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Syllabus (Analog and Digital Electronics)

ANALOG ELECTRONICS :

UNIT-I (Chapter - 1)

Special Diodes : LED, Varactor diode, Photo diode, Schottky diode, Tunnel diode; Their characteristics and applications.

Transistors as a switch.

UNIT-II (Chapters - 2, 3)

Frequency Response : Amplifier transfer function, Low and high frequency response of common emitter and common source amplifiers.

Feedback : General feedback structure; Properties of negative feedback; Series-series, Series-shunt, Shunt-series and shunt-shunt feedback amplifiers.

UNIT-III (Chapter - 4)

Basic principle of sinusoidal oscillator, R-C phase shift and Wein bridge oscillators, Tuned osciliators- Collpits and Hartley; Crystal oscillator.

DIGITAL ELECTRONICS :

UNIT-IV (Chapters - 5, 6, 7, 8)

Combinational Logic Circuits: Multiplexers/Demultiplexures, Encoders/Decoders.

Sequential Logic Circuits: Latches, Flip-flops- S-R, T, D, J-K.

Shift Registers: Basic principle, Serial and parallel data transfer, Shift left/right registers, Universal shift register.

Counters: Mode N counters, Ripple counters, Synchronous counters, Ring/Johnson counters.

UNIT-V (Chapters - 9, 10, 11)

OP-AMP Applications - Astable and monostable multivibrators, Schmitt trigger, IC-555 Timer, A/D and D/A converters.

Voltage Regulators: Series, Shunt and switching regulators, Op-amp based configurations.

Memories: Introduction to ROM, RAM; Sequential Memory, Memory organization.

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11

Memories

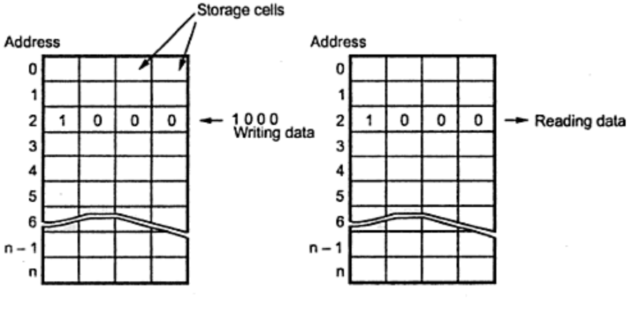
11.1 Introduction

We have seen registers, which are a type of storage devices; in fact, a register devices used to store large amount of digital data.

Memories are made up of registers. Each register in the memory is one storage location. Each location is identified by an **address**. The number of storage locations can vary from a few in some memories to hundreds of thousand in others. Each location can accommodate one or more bits. Generally, the total number of bits that a memory can store is its **capacity**. Most of the types the capacity is specified interms of bytes (group of eight-bits).

Each register consists of storage elements (flip-flops or capacitors in semiconductor memories and magnetic domain in magnetic storage), each of which stores one-bit of data. A storage element is called a **cell**.

The data stored in a memory by a process called **writing** and are retrieved from the memory by a process called **reading**. Fig. 11.1 illustrates in a very simplified way the concept of write, read, address and storage capacity for a generalized memory.



(a) Write operation

(b) Read operation

Fig. 11.1

As shown in the Fig. 11.1 a memory unit stores binary information in groups of bits called **words**. A word in memory is an entity of bits that moves in and out of storage as a unit. A word having group of 8-bits is called a **byte**. Most computer memories use words that are multiples of eight-bits in length. Thus, a 16-bit word contains two bytes, and a 32-bit word is made of 4 bytes.

The communication between a memory and its environment is achieved through data lines, address selection lines, and control lines that specify the direction of transfer. The Fig. 11.2 shows the block diagram of memory unit. The n data lines provide the information to be stored in memory and the k address lines specify the particular word chosen among the many available. The two control inputs specify the direction transfer.

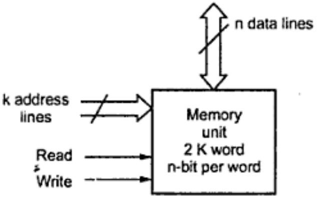

n data lines
k address lines
Memory unit
2 K word
n-bit per word
Read
Write

Fig. 11.2 Block diagram of memory unit

11.2 Classification of Memories

Fig 11.3 shows the classification of semiconductor memories.

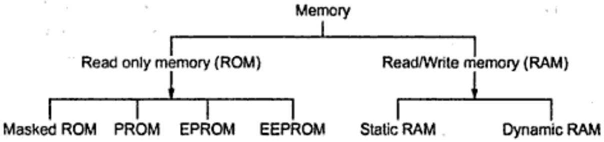

Memory
Read only memory (ROM)
Read/Write memory (RAM)
Masked ROM
PROM
EPROM
EEPROM
Static RAM
Dynamic RAM

Fig. 11.3 Classification of semiconductor memories

11.3 RAM Organization

Unlike ROM (Read Only Memory), we can read from or write into the RAM, so it is often called read/write memory. The numerical and character data that are to be processed by the computer change frequently. These data must be stored in type of memory from which they can be read by the microprocessor, modified through processing and written back for storage. For this reason they are stored in RAM instead of ROM. But it is a volatile memory i.e. it cannot hold data when power is turned off.

RAM memory cells are organized in the form of an array, in which each cell is capable of storing one-bit of information. The Fig. 11.4 shows the row and the column organization of a 8192-bit memory chip.

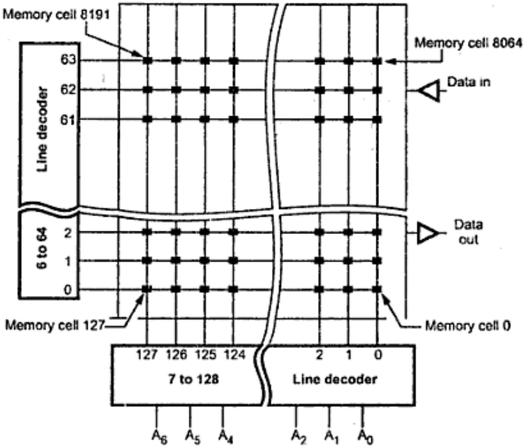


Fig. 11.4 Row and column organization for 8192-bit static RAM

The chip has 13 address lines. The first seven address lines are connected to the column decoder to indicate one of the 128 columns. The remaining 6 address lines are connected to the row decoder to indicate one of 64 rows. Where the decoded row and column cross, they select the desired individual memory cell. Simple arithmetic shows that there are $64 \times 128 = 8192$, crossings. Therefore, this memory has 8192 memory cells.

The Fig. 11.5 shows the organization of 16×8 (16 words of 8-bit each) memory. Here, the organization is shown with detail connections of address lines, data lines and control lines. The data input and the data output of each sense/write circuit are connected to a single bidirectional data line that can be connected to the data bus of a computer. Two control lines, R/$\overline{\text{W}}$ and $\overline{\text{CS}}$, are provided in addition to address and data lines. The R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$) input specifies the required operation and the $\overline{\text{CS}}$ input selects a given chip in a multichip memory system.

Nowadays the memory chips with much larger number of memory cells than the examples shown in Fig. 11.5 are commercially available. We have used small examples to avoid the complexity of figure. The larger memory has same organization that we have discussed. But the only difference is the number of data and address lines used in the memory organization. For example, a 8 Mbit chip may have a 1 M × 8 organization, in which 20 address and 8 data input/output lines are used.

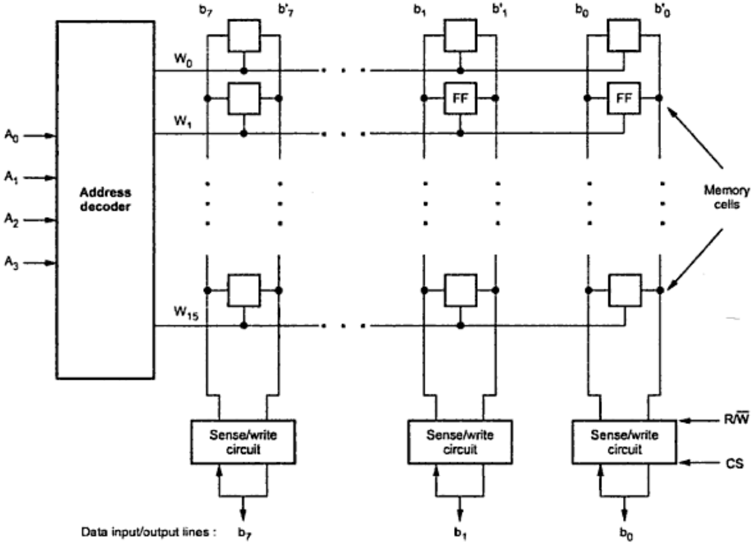

b7
b'7
b1
b'1
b0
b'0
W0
W1
W15
A0
A1
A2
A3
Address decoder
FF
FF
Memory cells
Sense/write circuit
Sense/write circuit
Sense/write circuit
R/W̄
CS
Data input/output lines :
b7
b1
b0

Fig. 11.5 Organization of bit cells in a memory chip

11.3.1 Read and Write Operation

- Steps to perform memory read operation are as follows :
  1. Apply the binary address of the desired word to the address lines.
  2. Activate the read input i.e. make $R/\overline{W}$ line high.
- Steps to perform memory write operation are as follows :
  1. Apply the binary address of the desired word to the address lines.
  2. Apply the data bits that is to be stored in the memory to the data lines.
  3. Activate the write input, i.e. make $R/\overline{W}$ line Low.

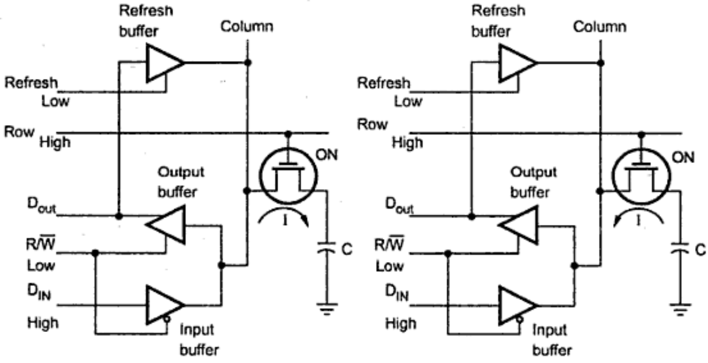
There are two types of RAMs.

- Static RAM
- Dynamic RAM

disabled by controlling $R/\overline{W}$ line. When $R/\overline{W}$ line is LOW, input buffer is enabled and output buffer is disabled. When $R/\overline{W}$ line is HIGH, input buffer is disabled and output buffer is enabled. With this basic information let us see the read, write and refresh operations.

11.3.3.1 Write Operation

To enable write operation $R/\overline{W}$ line is made LOW which enables input buffer and disables output buffers, as shown in the Fig. 11.10 (a). To write a 1 into the cell, the D_{IN} line is HIGH and the transistor is turned ON by a HIGH on the ROW line. This allows the capacitor to charge to a positive voltage. When 0 is to be stored, a LOW is applied to the D_{IN} line. The capacitor remains uncharged, or if it is storing a 1, it discharges as indicated in Fig. 11.10 (b). When the ROW line is made LOW, the transistor turns off and disconnects the capacitor from the data line, thus storing the charge (either 1 or 0) on the capacitor.


Refresh buffer
Column
Refresh Low
Row High
ON
Output buffer
D_{out}
$R/\overline{W}$ Low
D_{IN} High
I
C
Input buffer
Refresh buffer
Column
Refresh Low
Row High
ON
Output buffer
D_{out}
$R/\overline{W}$ Low
D_{IN} High
I
C
Input buffer

(a) Writing a 1 into the memory cell **(b) Writing a 0 into the memory cell**

Fig. 11.10

11.3.3.2 Read Operation

To read data from the cell, the $R/\overline{W}$ line is made HIGH, which enables output buffer and disables input buffer. Then ROW line is made HIGH. It turns transistor ON and connects the capacitor to the D_{OUT} line through output buffer. This is illustrated in Fig. 11.10 (c).

11.3.4 Comparison between SRAM and DRAM

Sr. No	Static RAM	Dynamic RAM
1.	Static RAM contains less memory cells per unit area.	Dynamic RAM contains more memory cells as compared to static RAM per unit area.
2.	Its access time is less hence faster memories	Its access time is greater than static RAMs.
3.	Static RAM consists of number of Flip-flops. Each flip-flop stores one-bit.	Dynamic RAM stores the data as a charge on the capacitor. It consists of MOSFET and the capacitor for each cell.
4.	Refreshing circuitry is not required.	Refreshing circuitry is required to maintain the charge on the capacitors after every few milliseconds. Extra hardware is required to control refreshing. This makes system design complicated.
5.	Cost is more.	Cost is less.

In above discussion we have seen memory organization for ROM and static RAM. In this organization, data is organized as a single bit data word. However, in most memory ICs the data is organized as eight-bit data word. In these ICs eight memory cells are connected in parallel and enabled at a time to read or write eight-bit data word. The eight memory cells connected in parallel forms a register and memory is nothing but an array of registers.

11.3.5 Memory Cycles and Timing Waveforms

Let us study read and write memory cycle with their timing parameters.

Read Cycle

Fig. 11.11 shows the read cycle for static RAM. The timing diagram is drawn on the basis of different timing parameters. These are as follows :

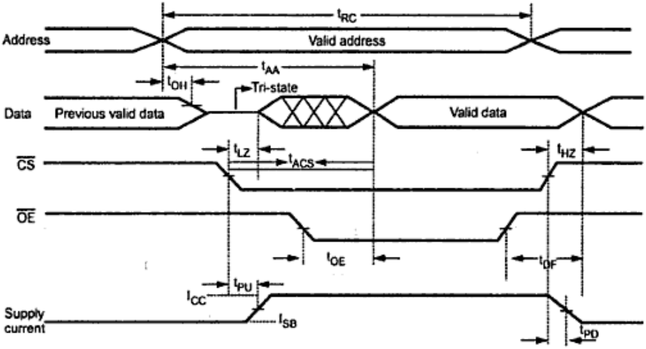


Fig. 11.11 Read cycle timing waveforms

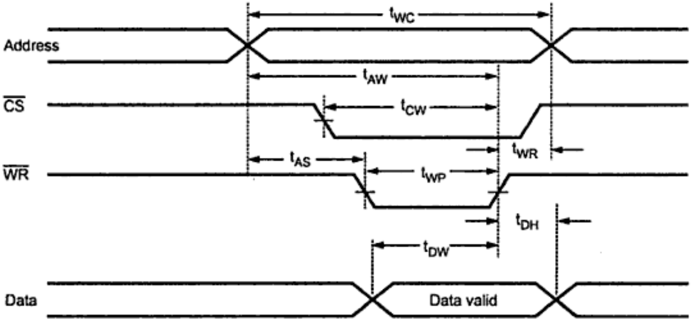


Fig. 11.12 Write cycle timing waveforms

Write Cycle

Fig. 11.12 shows the write cycle for static RAM. The timing diagram is drawn on the basis of different timing parameters. These are as follows :

1. t_{WC} : Write Cycle Time

It is the minimum time for which an address must be held stable on the address bus, in write cycle.

2. t_{AW} : Address Valid to End of Write

It is the time at which address must be applied on the address bus before $\overline{WR}$ goes high.

3. t_{WR} : Write Recovery Time

It is the time for which address will remain on address bus after $\overline{WR}$ goes high.

4. t_{AS} : Address Setup Time

When address is applied, it is the time after which $\overline{WR}$ can be made low.

5. t_{CW} : Chip Selection to the End of Write

It is the time at which the $\overline{CE}$ must be made low to select the device before $\overline{WR}$ goes high.

6. t_{WP} : Write Pulse Width

It is the time for which $\overline{WR}$ goes low.

7. t_{DW} : Data Valid to the End of Write

It is the minimum time for which data must be valid on the data bus before $\overline{WR}$ goes high.

8. t_{DH} : Data Hold Time

It is the time for which data must be held valid after $\overline{WR}$ goes high.

11.4 Memory Decoding

We have seen that in the organization of memory, there is a need for decoding circuit to select the memory word specified by the input address. In this section we study the operation of the decoder. As shown in the Fig. 11.13 there are 16 words of 8-bits each. A memory with 16 words needs four address lines. The four address inputs go through a 4 × 16 decoder to select one of the sixteen words. The decoder is enabled with a memory enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory select at 1, one of the sixteen words is selected, dictated by the value in the four address lines. Once a word has been selected, the read/write input determines the operation. During write operation, the data available in the input lines are transferred into the eight memory cells of the selected word. The memory cells that are not selected are disabled and their previous binary values remain unchanged.

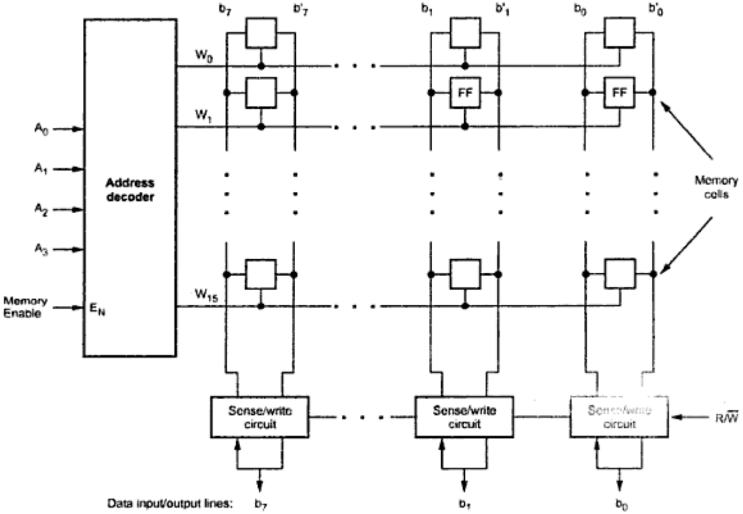

b_7
b'_7
b_1
b'_1
b_0
b'_0
W_0
W_1
W_{15}
FF
FF
A_0
A_1
A_2
A_3
Address decoder
Memory Enable
E_N
Memory cells
Sense/write circuit
Sense/write circuit
Sense/write circuit
$R/\overline{W}$
Data input/output lines:
b_7
b_1
b_0

Fig. 11.13 Organization of bit cells in a memory chip

11.5 Memory Expansion

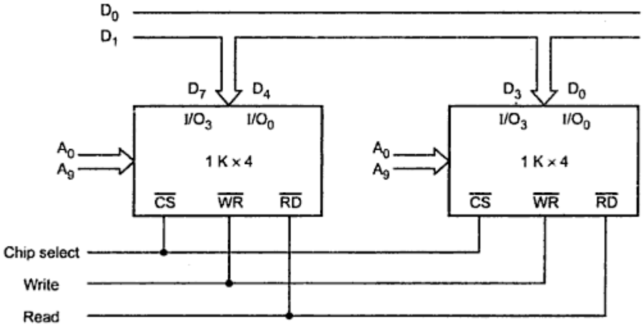
The memory expansion can be achieved in two ways : By expanding word size and by expanding memory capacity.

11.5.1 Expanding Word Size

It is possible to expand word size of memory by connecting two or more ICs together. The word size of memory IC can be increased by connecting two memory ICs in such a way that their data bus is in series and address bus in parallel. Both memory ICs are selected simultaneously by common chip select signal to access entire expanded word at a time. The example 11.1 illustrates method of word expansion.

➠ **Example 11.1 :** *Design 1 K × 8 RAM using two 1 K × 4 ICs.*

Solution :



D_0
D_1
D_7
D_4
I/O_3
I/O_0
1 K × 4
A_0
A_9
$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
D_3
D_0
I/O_3
I/O_0
1 K × 4
A_0
A_9
$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
Chip select
Write
Read

Fig. 11.15

11.5.2 Expanding Memory Capacity

The memory capacity can be increased by connecting two or more memory ICs in parallel. This means that the address, data and control lines are connected in parallel to all memory ICs. Each IC is selected by the separate chip select signal generated by the address decoder. This is illustrated by the following example.

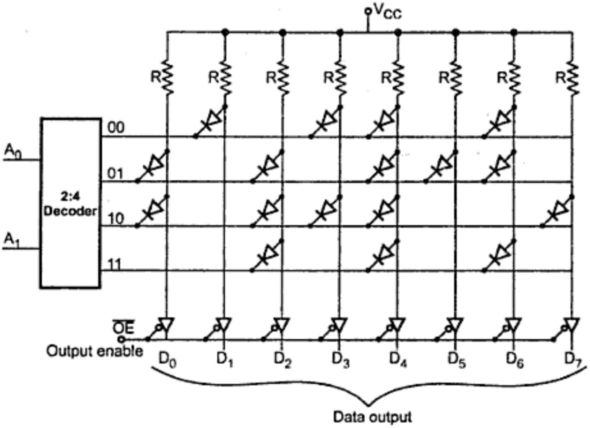


Fig. 11.17 Simple four byte diode ROM

Address in binary	Binary data								Data in hex
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
00	1	0	1	0	0	1	0	1	A5
01	0	1	0	1	0	0	0	1	51
10	0	1	0	0	0	1	1	0	46
11	1	1	0	1	0	1	0	1	D5

Table 11.1 Contents of ROM

Nowadays ROMs use MOS technology instead of diode. Fig. 11.18 shows four nibble (half-byte) ROM using MOS transistors. Here, diodes and pull up resistors are replaced by MOS transistors. The address on the address lines (A_0 and A_1) is decoded by 2 : 4 decoder. Decoder selects one of the four rows making it logic 0. The inverter connected at the output of decoder inverts the state of selected row (i.e. logic 1). Therefore, each output data line goes to logic 0 if a gate of MOS transistor is connected to row select lines. When gate of the MOS transistor is connected to the selected row, MOS transistor is turned on. This pulls the corresponding column data line to logic 0.

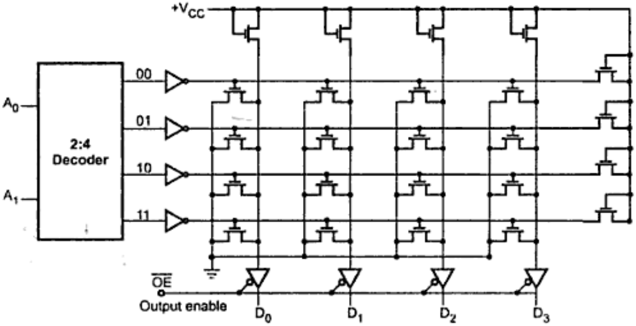


Fig. 11.18 Simple four half-byte ROM

In integrated circuits, a thin metallized layer connects the gates of some transistors to the row select lines. The gate connections of MOS transistors depend on the data to be stored in the ROM. Therefore, according to the user truth table, manufacturer can deposit thin layer of metal to connect gates of the transistors. Once the pattern/mask is decided, it is possible to make thousands of such ROMs. Such ROMs are called **Mask programmed ROMs.** Masked ROMs are used in microprocessor based toys, TV games, home computers and other such high volume consumer products.

11.6.1 PROM (Programmable Read Only Memory)

PROMs are programmed by user. To provide the programming facility, each address select and data line intersection has its own fused MOSFET or transistor. When the fuse is intact, the memory cell is configured as a logic 1 and when fuse is blown (open circuit), the memory cell is logical 0. Logical 0s are programmed by selecting the appropriate select line and then driving the vertical data line with a pulse of high current. The Fig. 11.19 shows a PROM fused MOSFET memory cell.

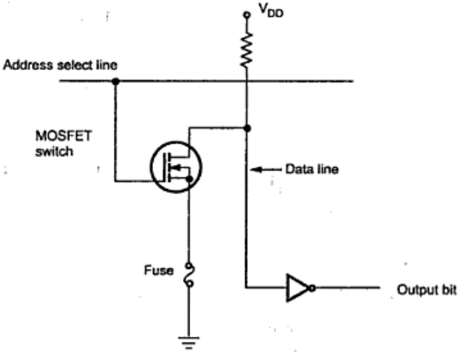


Fig. 11.19 Single fused PROM cell

Fig. 11.20 shows four byte PROM. It has diodes in every bit position; therefore, the output is initially all 0s. Each diode, however has a fusible link in series with it. By addressing bit and applying proper current pulse at the corresponding output, we can blow out the fuse, storing logic 1 at that bit position. The fuse uses material like nichrome and polycrystalline. For blowing the fuse it is necessary to pass around 20 to 50 mA of current for period 5 to 20 μs. The blowing of fuses according to the truth table is called programming of ROM. The user can program PROMs with special PROM programmer. The PROM programmer selectively burns the fuses according to the bit pattern to be stored. This process is also known as burning of PROM. The PROMs are one time programmable. Once programmed, the information stored is permanent.

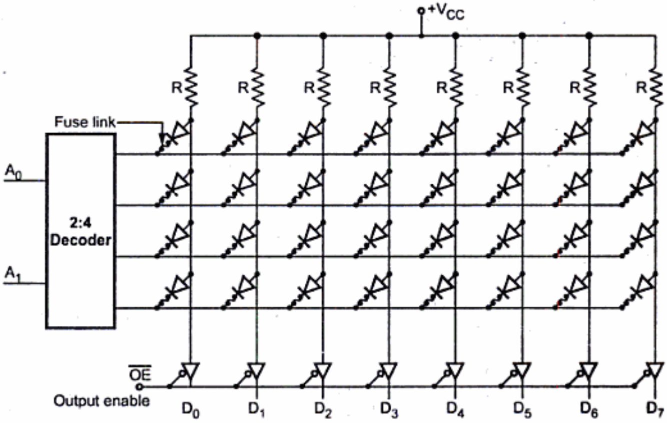


Fig. 11.20 Four byte PROM

11.6.2 EPROM (Erasable Programmable Read Only Memory)

Erasable programmable ROMs use MOS circuitry. They store 1s and 0s as a packet of charge in a buried layer of the IC chip. EPROMs can be programmed by the user with a special EPROM programmer. The important point is that we can erase the stored data in the EPROMs by exposing the chip to ultraviolet light through its quartz window for 15 to 20 minutes, as shown in the Fig. 11.21.

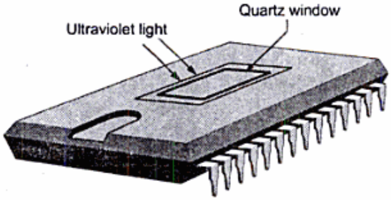


Fig. 11.21 EPROM

It is not possible to erase selective information, when erased the entire information is lost. The chip can be reprogrammed. This memory is ideally suitable for product development, experimental projects and college laboratories, since this chip can be reused many times, over.

EPROM Programming :

When erased each cell in the EPROM contains 1. Data is introduced by selectively programming 0s into the desired bit locations. Although only 0s will be programmed, both 1s and 0s can be presented in the data.

During programming address and data are applied to address and data pins of the EPROM. When the address and data are stable, program pulse is applied to the program input of the EPROM. The program pulse duration is around 50 ms and its amplitude depends on EPROM IC. It is typically 11.5 V to 25 V. In EPROM, it is possible to program any location at any time - either individually, sequentially or at random.

11.6.3 EEPROM (Electrically Erasable Programmable Read Only Memory) /EAPROM (Electrically Alterable Programmable Read Only Memory)

Electrically erasable programmable ROMs also use MOS circuitry very similar to that of EPROM. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. The insulating layer is made very thin (< 200 Å). Therefore, a voltage as low as 20 to 25 V can be used to move charges across the thin barrier in either direction for programming or erasing. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals. The EEPROM memory also has a special chip erase mode by which entire chip can be erased in 10 ms. This time is quite small as compared to time required to erase EPROM and it can be erased and reprogrammed with device right in the circuit. However, EEPROMs are most expensive and the least dense ROMs.

11.7 Sequential Memory : Magnetic Tape

Magnetic tape is one of the most popular storage medium for large data that are sequentially accessed and processed. The tape is formed by depositing magnetic film on a very thin and 1/2 inch or 1/4 inch wide plastic tape. Usually, iron oxide is used as a magnetizing material. The tape ribbon itself is stored in reels similar to the tape used on a tape recorder except that it is of high quality and more durable. Like audio tape, computer tape can be erased and reused indefinitely. Old data on a tape are automatically erased as new data are recorded in the same area.

The information is recorded on the tape with the help of read/write head. It magnetizes or nonmagnetizes tiny invisible spots (representing 1's and 0's) on the iron oxide side of the tape, as shown in the Fig. 11.22.

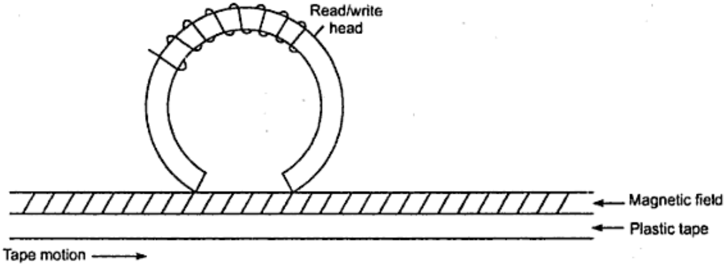

Read/write head
Magnetic field
Plastic tape
Tape motion

Fig. 11.22 Magnetic recording with read/write head

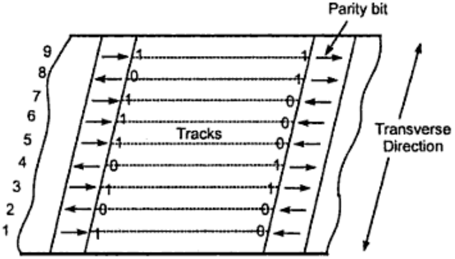

Parity bit
9
8
7
6
5
4
3
2
1
1
0
1
1
1
0
1
0
1
1
1
0
0
0
1
1
0
0
Tracks
Transverse Direction

Fig. 11.23 Magnetic recorded tape

Usually, seven or nine bits (corresponding to one character) are recorded in parallel across the width of the tape, perpendicular to the direction of motion. A separate read/write head is provided for each bit position on the tape, so that all bits of characters can be read or written in parallel. One of the character bit is used as a parity bit. This is illustrated in Fig. 11.23.

Data on the tape are organized in the form of *records* separated by gaps, as shown in the Fig. 11.24. A set of related records constitutes a *file*. A *file mark* is used to identify the beginning of the file. The file mark is a special single or multiple character record, usually preceded by a gap longer than the interrecord gap. The record following the file mark

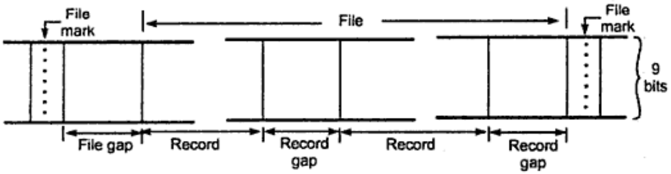

File mark
File
File mark
9 bits
File gap
Record
Record gap
Record
Record gap

Fig. 11.24 Organization of data on magnetic tape

1. BCD Decade (8421) Counter :

The B input must be externally connected to the Q_A output and A input receives the incoming count and a BCD count sequence is produced.

2. Symmetrical Bi-quinary Divide-by-Ten Counter :

The Q_D output must be externally connected to the A input. The input count is then applied to the B input and a divide-by-ten square wave is obtained at output Q_A.

3. Divide-by-Two and Divide-by-Five Counter :

No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (A as the input and Q_A as the output). The B input is used to obtain binary divide-by-five operation at the Q_D output.

Table 8.8 shows function tables and Fig. 8.49 shows logic diagram for IC 7490.

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Table 8.8 (a) BCD count sequences (Note 1)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L

Clock	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Table 8.9

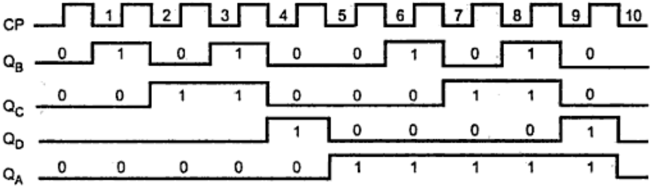


Fig. 8.56 Waveforms

Example 8.29 : *Design a mod-25 counter using IC 7490.*

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-25 counter, the counter is reset as soon as it becomes 0010 0101. The diagram is shown in Fig. 8.57.

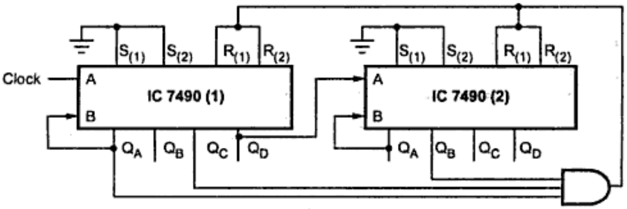

$S_{(1)}$
$S_{(2)}$
$R_{(1)}$
$R_{(2)}$
Clock
A
B
IC 7490 (1)
Q_A
Q_B
Q_C
Q_D
$S_{(1)}$
$S_{(2)}$
$R_{(1)}$
$R_{(2)}$
A
B
IC 7490 (2)
Q_A
Q_B
Q_C
Q_D

Fig. 8.57

1

Special Diodes

1.1 Introduction

A general purpose diode has one p-n junction. But number of other types of diodes having one or more than one p-n junctions are available. Such diodes have different characteristics, different methods of construction and special areas of application. These diodes are called **special diodes**. Some of such special diodes are photodiode, tunnel diode, light emitting diode, Schottky diode etc. The details about the construction, characteristics and applications of such special diodes are discussed in this chapter.

1.2 Light Emitting Diode (LED)

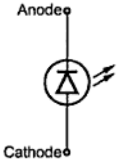


Fig. 1.1 Symbol of LED

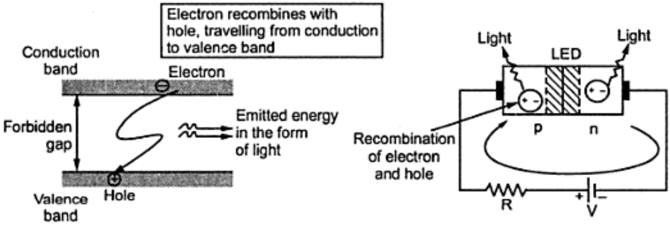
The LED is an optical diode, which emits light when forward biased. The Fig. 1.1 shows the symbol of LED which is similar to p-n junction diode apart from the two arrows indicating that the device emits the light energy.

1.2.1 Basic Operation

Whenever a p-n junction is forward biased, the electrons cross the p-n junction from the n-type semiconductor material and recombine with the holes in the p-type semiconductor material. The free electrons are in the conduction band while the holes are present in the valence band. Thus the free electrons are at higher energy level with respect to the holes. When a free electron recombines with hole, it falls from conduction band to a valence band. Thus the energy level associated with it changes from higher value to lower value. The energy corresponding to the difference between higher level and lower level is released by an electron while travelling from the conduction band to the valence band. In normal diodes, this energy released is in the form of heat. But LED is made up some special material which release this energy in the form of **photons** which emit the light energy. Hence such diodes are called light emitting diodes.

This process is called **electroluminescence**.

The Fig. 1.2 shows the basic principle of this process. The energy released in the form of light depends on the energy corresponding to the forbbiden gap. This determines the wavelength of the emitted light. The wavelength determines the colour of the light and also determines whether the light is visible or invisible (infrared). The various impurities are added during the doping process to control the wavelength and colour of the emitted light. For normal silicon diode, the forbidden energy gap is 1.1 eV and wavelength of the emitted light energy corresponds to that of infrared light spectrum hence in normal diodes the light is not visible. The infrared light is not visible.


Electron recombines with hole, travelling from conduction to valence band
Conduction band
Electron
Forbidden gap
Emitted energy in the form of light
Valence band
Hole
Light
LED
Light
Recombination of electron and hole
p
n
R
V

(a) Process of electroluminescence (b) LED forward biased

Fig. 1.2 Operation of LED

1.2.2 Materials and Colours

The LEDs use mixtures of Gallium (Ga), Arsenic (As) and Phosphorous (P).

The colour of emitted light is decided by its wavelength which depends on forbidden energy gap. This gap is different for different mixtures. Hence different mixtures give the different colours.

No.	Mixture used	Symbol	Colour
1.	Gallium arsenide	GaAs	Infrared, Invisible
2.	Gallium phosphide	GaP	Red or green
3.	Gallium arsenide phosphide	GaAsP	Red or yellow

1.2.3 Construction of LED

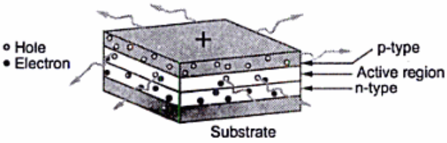
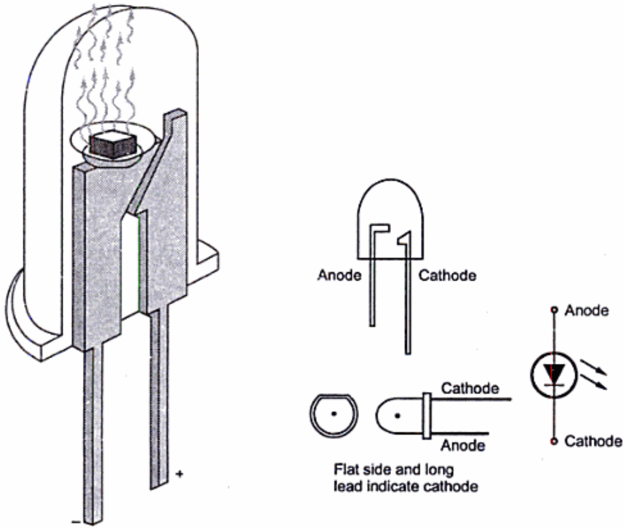

+
o Hole
• Electron
p-type
Active region
n-type
Substrate

Fig. 1.3 LED construction

One of the methods used for the LED construction is to deposite three semiconductor layers on the substrate as shown in the Fig. 1.3. In between p type and n type, there exists an active region. This active region emits light, when an electron and hole recombine. When the diode is forward biased, holes from p type and electrons from n type, both get driven into the active region. And when recombine, the light is emitted.

In this particular structure, the LED emit light all the way around the layered structure. Thus the basic layered structure is placed in a tiny reflective cup so that the light from the active layer will be reflected towards the desired exit direction. This is shown in the Fig. 1.4 (a) while the symbol of LED indicating identification of anode and cathode is shown in the Fig. 1.4 (b).


+
–
Anode
Cathode
Cathode
Anode
Flat side and long lead indicate cathode
Anode
Cathode

(a) Cup type construction

(b) Anode-cathode indication

Fig. 1.4

1.2.4 Biasing of LED

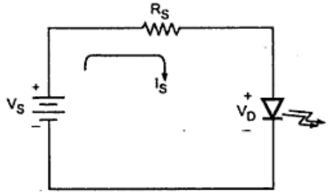


Fig. 1.5 LED circuit

Consider a source connected to LED and a resistor as shown in the Fig. 1.5.

The outward arrows associated with a diode indicate that it is LED.

The resistor R_s is the current limiting resistor. Due to this resistor, the current through the circuit is limited and prevented from exceeding the maximum current rating of the diode.

Let V_S = Supply voltage

V_D = Drop across LED

Applying KVL to the circuit we can write,

$$V_S = I_S R_S + V_D$$

$$I_S = \frac{V_S - V_D}{R_S}$$

When forward biased, the voltage drop across conducting LED is about 2 to 3 V which is considerably greater than that across a normal silicon or germanium diode. The current range of commercially available LEDs is 10 to 80 mA. Unless and otherwise specified, while analyzing the LED circuits, the drop across LED is considered as $V_D = 2$ V.

The reverse breakdown voltage of LED is much less than the normal diode, which is about 3 V to 10 V.

1.2.5 Spectral Output Curves for LED

The visibility of the light is decided from its **wavelength (λ)**. The graph of output light of LED against the wavelength λ gives the various curves called spectral output curves for LEDs. These are shown in the Fig. 1.6.

It can be seen that wavelength is expressed in nm (nanometres). The normalized output for visible light shows peak at 460 nm for blue, at 540 nm for green, at 590 nm for yellow and at 660 nm for red. The infrared invisible light output shows a peak at 940 nm.

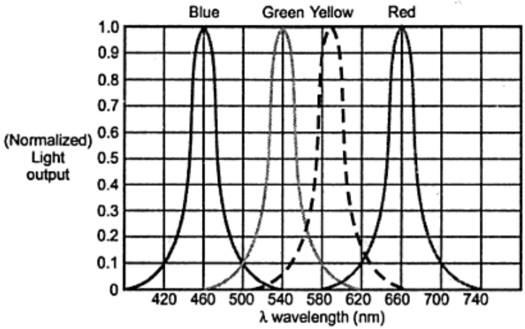


Fig. 1.6 Spectral output curves for visible light

1.2.6 Radiation Pattern of LED

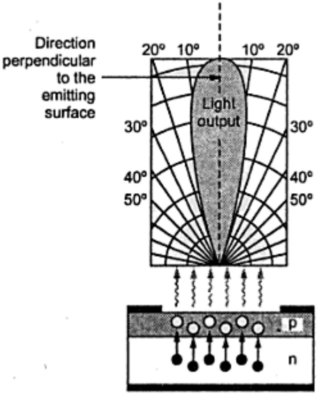

Direction perpendicular to the emitting surface
20°
10°
10°
20°
30°
30°
40°
40°
50°
50°
Light output
p
n

Fig. 1.7 Radiation pattern of a typical LED

LED is a directional light source. It emits the light in a particular way which has a typical radiation pattern. Maximum emitted power is perpendicular to the emitting surface. The Fig. 1.7 shows a radiation pattern for a typical LED, which shows that most of the energy is emitted within 20° of the direction of maximum light.

Some LEDs use plastic lenses to spread the light for a greater angle to increase the visibility. The coloured lenses are also used to enhance the colour.

1.2.7 Output Characteristics of LED

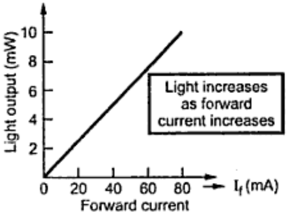


Fig. 1.8 LED output characteristic

The amount of power output translated into light is directly proportional to the forward current I_f. More the forward current I_f, the greater is the output light. The graph of forward current and output light in mW is shown in the Fig. 1 8. This is called **output characteristics** for LED.

When forward biased, the voltage drop across conducting LED is about 2 to 3 V which is considerably greater than that across a normal silicon or germanium diode. The current range of commercially available LEDs is 10 to 80 mA. Unless and otherwise specified, while analyzing the LED circuits, the drop across LED is considered as $V_D = 2$ V.

The reverse breakdown voltage of LED is much less than the normal diode, which is about 3 V to 10 V.

1.2.8 Data Sheet Information of LED

The two important parameters related to LED characteristics are,

i) Radiant intensity : The LED output power per steradian is called axial radiant intensity. The symbol for radiant intensity is I_e. The steradian (sr) is the unit of solid angle. The unit of radiant intensity is W/sr or mW/sr.

ii) Irradiance : The power per unit area at a given distance from the LED source is called irradiance. It is denoted as H and expressed in W/cm^2 or mW/cm^2. Mathematically irradiance can be calculated as,

$$H = \frac{I_e}{d^2}$$

Where I_e = Radiant intensity

d = Distance from LED source in cm

The electrical characteristics, maximum ratings and optical characteristics of a typical MLED81 are given in the following tables.

Maximum ratings :

Rating	Symbol	Value	Unit
Reverse voltage	V_R	5	volts
Forward current-continuous	I_F	100	mA
Forward current-peak pulse	I_F	1	A
Total power dissipation at $T_A = 25\,°C$ Derate above 25 °C	P_D	100 2.2	mW mW/°C
Ambient operating temperature range	T_A	– 30 to +70	°C
Storage temperature	T_{stg}	– 30 to + 80	°C
Lead soldering temperature, 5 seconds max, 1/16 inch from case	–	260	°C

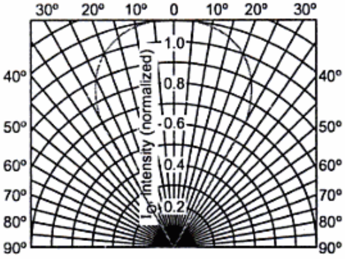
Electrical characteristics ($T_A = 25\,°C$ unless otherwise noted) :

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse leakage current ($V_R = 3$ V)	I_R	–	10	–	nA
Reverse leakage current ($V_R = 5$ V)	I_R	–	1	10	µA
Forward voltage ($I_F = 100$ mA)	V_F	–	1.35	1.7	V
Temperature coefficient of forward voltage	ΔV_F	–	– 1.6	–	mV/°K
Capacitance (f = 1 MHz)	C	–	25	–	pF

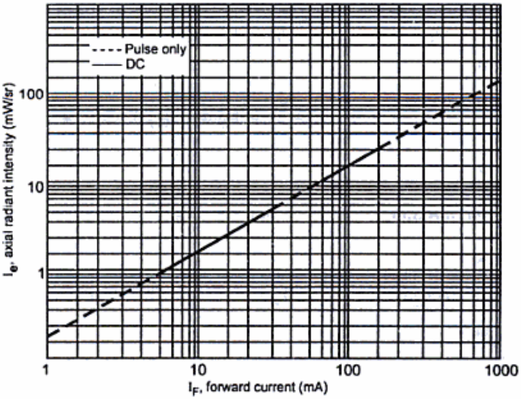
Optical characteristics ($T_A = 25\,°C$ unless otherwise noted) :

Characteristic	Symbol	Min	Typ	Max	Unit
Peak wavelength ($I_F = 100$ mA)	λ_p	–	940	–	nm
Spectral half-power bandwidth	$\Delta\lambda$	–	50	–	nm
Total power output ($I_F = 100$ mA)	ϕ e	–	16	–	mW
Temperature coefficient of total power output	$\Delta\phi$ e	–	– 0.25	–	%/K
Axial radiant intensity ($I_F = 100$ mA)	I_e	10	15	–	mW/sr
Temperature coefficient of axial radiant intensity	ΔI_e	–	– 0.25	–	%/K
Power half-angle	φ	–	± 30	–	°

Similarly the data sheet includes some graphical characteristics. The Fig. 1.9 shows spatial radiation pattern and intensity versus forward current graphs for MLED 81.



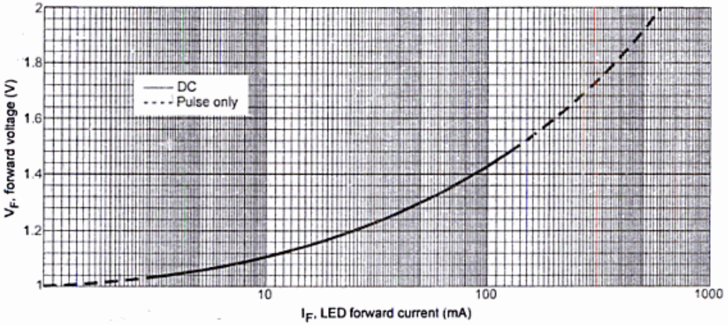
(a) Spatial radiation pattern



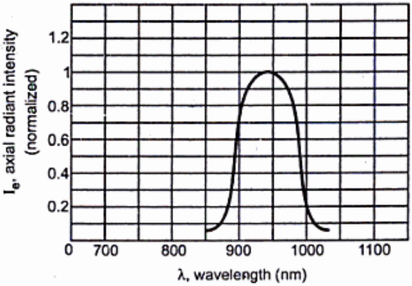
(b) Intensity versus forward current

Fig. 1.9 MLED 81 data sheet graphs

The Fig. 1.10 shows other two graphs for MLED 81 available in its datasheet.



(a) LED forward voltage versus forward current



(b) Relative spectral emission

Fig. 1.10 MLED 81 data sheet graphs

It can be seen for this device that at 30° on the either side of the maximum orientation, the output power reduces to about 60% of the maximum.

1.2.9 Advantages of LED

The various advantages of LED are,

1. LEDs are small in size, and hence can be regarded as point source of light. Because of their small size, several thousand LEDs can be packed in one sq. metre area.

2. The brightness of light emitted by LED depends on the current flowing through LED. Hence the brightness of light can be smoothly controlled by varying the current. This makes possible to operate LED displays under different ambient lighting conditions.
3. LEDs are fast operating devices. They can be turned on and off in time less than 1 microsecond.
4. The LEDs are light in weight.
5. The LEDs are available in various colours.
6. The LEDs have long life.
7. The LEDs are cheap and readily available.
8. The LEDs are easy to interface with various other electronic circuits.
9. Some LEDs radiate infrared light which is invisible but still useful in some applications like burglar alarm systems.
10. LEDs are useful for the applications which are subjected to frequent on-off cycling. The fluorescent lamps burn out more quickly when cycled.
11. LEDs can be easily dimmed using pulse width modulation or by controlling the forward current.
12. LEDs are shock resistant and difficult to damage due to external shocks.
13. LEDs do not contain toxic material like mercury which is used in fluorescent lamps.

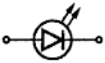
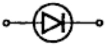
1.2.10 Disadvantages of LED

The various disadvantages of LED are,

1. It draws considerable current requiring frequent replacement of battery in low power battery operated devices.
2. Luminous efficiency of LEDs is low which is about 1.5 lumen/watt.
3. The characteristics are affected by temperature.
4. Need large power for the operation compared to normal p-n junction diode.

1.2.11 Comparison of LED and P-N Junction Diode

Sr. No.	LED	P-N junction diode
1.	It emits light, when forward biased.	It does not emit light.
2.	It uses materials like gallium, arsenide phosphide and gallium phosphide.	It uses materials like silicon and germanium.
3.	The drop across forward biased LED is about 2 V.	The drop across forward biased diode is about 0.7 V, much less than that of LED.

4.	Reverse breakdown voltage is low, about 3 V to 10 V.	Reverse breakdown voltage is high, about 50 V and more.
5.	Needs large power for the operation.	Needs less power for the operation.
6.	Draws considerable current from battery.	Draws less current.
7.	Symbol is 	Symbol is 
8.	The applications are optocouplers, seven segment displays, alpha numeric displays.	The applications are rectifiers, clippers, clampers, voltage multipliers and many other electronic circuits.

1.2.12 Applications of LED

Due to the advantages like low voltage, long life, cheap, reliable, fast on-off switching etc., the LEDs are used in many applications. The various applications of LED are,

1. All kinds of visual displays i.e. seven segment displays and alpha numeric displays. Such displays are commonly used in the watches and calculators.
2. In the optical devices such as optocouplers.
3. As on-off indicator in various types of electronic circuits.
4. Some LEDs radiate infrared light which is invisible. But such LEDs are useful in remote controls and applications like burglar alarm.

➠ **Example 1.1 :** *What is the current through LED used in a circuit shown in the Fig. 1.11.*

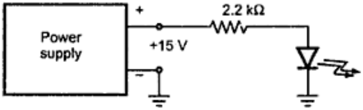


Fig. 1.11

Solution : Assume the drop across the LED as 2 V.

$$\therefore \quad V_D = 2\text{ V}$$

From Fig. 1.11, $R_S = 2.2\text{ k}\Omega$ and $V_S = 15\text{ V}$

$$\therefore \quad I_S = \frac{V_S - V_D}{R_S} = \frac{15-2}{2.2\times10^3} = \mathbf{5.91\ mA}$$

1.3 Seven Segment Display

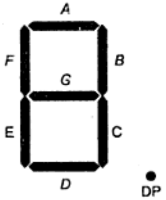


Fig. 1.12 Seven segment indicator

A display consisting of seven LEDs arranged in seven segments is called seven segment display. It is shown in the Fig. 1.12. The seven LEDs are arranged in a rectangular fashion and are labeled A through G. Each LED is called a **segment** because it forms a part of the digit being displayed. An additional LED is used for the indication of a decimal point (DP).

By forward biasing different LEDs we can display the digits 0 through 9. For example, to display a zero, the LEDs A, B, C, D, E and F are forward biased. To light up a 5, we need to forward bias segments A, F, G, C, D. Thus in a seven segment display depending upon the digit to be displayed, the particular set of LEDs is forward biased. The various digits from 0 to 9 which can be displayed using seven segment display are shown in the Fig. 1.13.

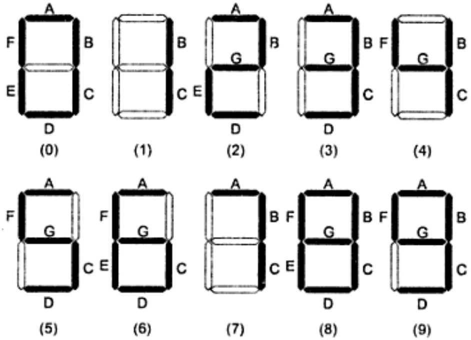


Fig. 1.13 Various digits displayed with 7 segment display

A seven segment display can also display the capital letters A, C, E and F and also small letters b and d. Microprocessor kits often use such seven segment displays.

1.3.1 Types of Seven Segment Display

The two types of seven segment display are available called,

1) Common anode type 2) Common cathode type

Common anode type

In this type, all anodes of LEDs are connected together and common point is connected to + V_{CC} which is positive supply voltage. A current limiting resistor is required to be connected between each LED and ground. The connection is shown in the Fig. 1.14.

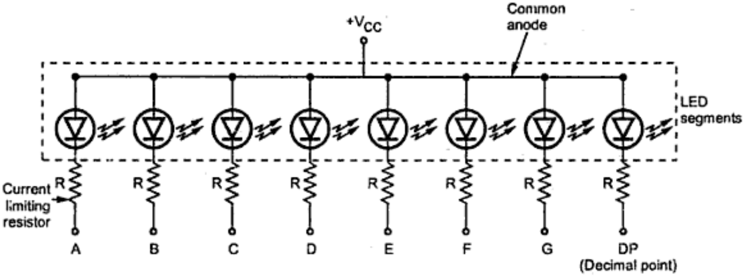

+V_{CC}
Common anode
LED segments
Current limiting resistor
R
R
R
R
R
R
R
R
A
B
C
D
E
F
G
DP
(Decimal point)

Fig. 1.14 Common anode type

Common cathode type

In this type, all cathodes of LEDs are connected together and common point is connected to the ground. A current limiting resistor is connected between each LED and the supply + V_{CC}. The anodes of the respective segments are to be connected to + V_{CC} for the required operation of LEDs. The connection of common cathode type display is shown in the Fig. 1.15.

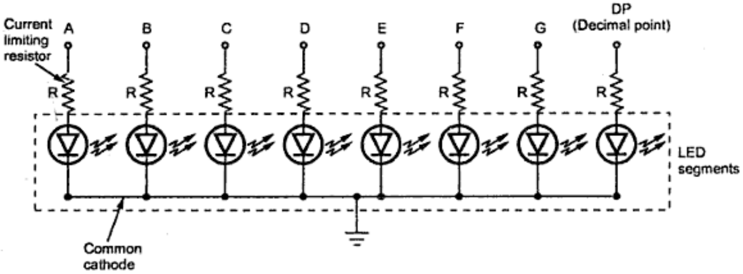
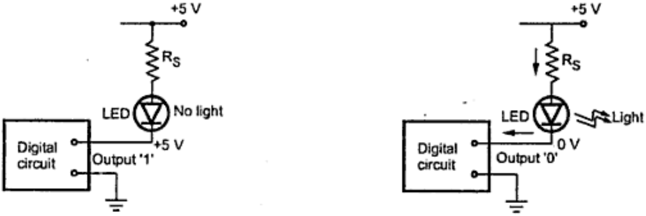

Current limiting resistor
A
B
C
D
E
F
G
DP
(Decimal point)
R
R
R
R
R
R
R
R
LED segments
Common cathode

Fig. 1.15 Common cathode type

1.3.2 LED Driver Circuit

The output of a digital circuit is logical i.e. either '0' or '1'. The '0' means low while '1' means high. In the high state the output voltage is nearly 5 V while in low state, it is almost 0 V. If LED is to be driven by such digital circuit, it can be connected as shown in the Fig. 1.16. When output of digital circuit is high, both ends of LED are at 5 V and it can not be forward biased hence will not give light. While when output of digital circuit is low, then high current will flow through LED as it becomes forward biased, and it will give light.


+5 V
R_S
LED
No light
Digital circuit
+5 V
Output '1'
+5 V
R_S
LED
Light
Digital circuit
0 V
Output '0'

(a) TTL output high **(b) TTL output low**

Fig. 1.16

In practice seven segment displays are used at the output of digital integrated circuits, the output of which is in binary coded decimal form (BCD). Such output has only four lines and it cannot drive seven segments of the display directly. In such a case a driver

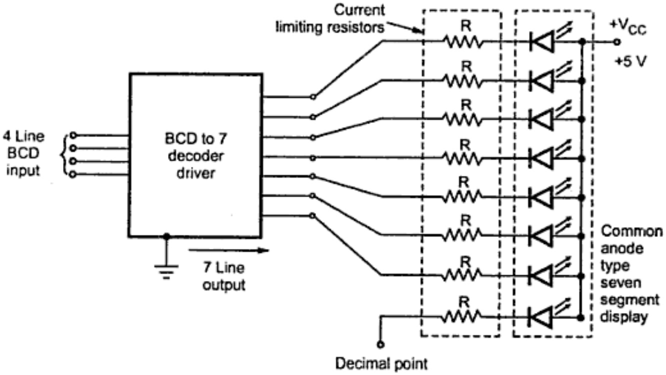

Current limiting resistors
R
+V_CC
+5 V
4 Line BCD input
BCD to 7 decoder driver
7 Line output
Common anode type seven segment display
Decimal point

Fig. 1.17 Typical 7-segment LED display with its driver

circuit is used which is a BCD to 7 segment decoder. It converts 4 BCD lines into 7 lines. A typical LED seven segment display with its driver circuit is shown in the Fig. 1.17. The common anode type display is used.

Notice that, an additional LED corresponding to the decimal point is also provided in the seven segment display, which again has a current limiting series resistance. Here a positive voltage is applied to the common anode. Therefore selected LEDs are illuminated by making their respective cathodes low (0 V).

1.4 Varactor Diode

In a normal diode, the depletion region exists between p-region and n-region as shown in the Fig. 1.18.

The p-region and n-region act like the plates of capacitor while the depletion region acts like dielectric. Thus there exists a capacitance at the p-n junction called **transition capacitance, space charge capacitance, barrier capacitance** or **depletion region capacitance.** It is denoted as C_T.

Mathematically it is given by the expression,

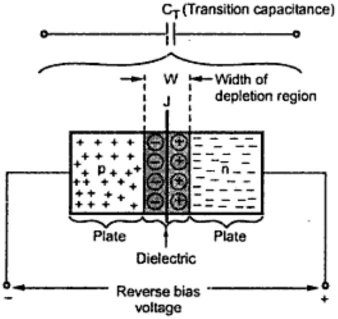


Fig. 1.18

$$\boxed{C_T = \frac{\varepsilon A}{W}}$$

where ε = Permittivity of semiconductor

A = Area of cross section

W = Width of depletion region

As the reverse biased applied to the diode increases, the width of the depletion region (W) increases. Thus the transition capacitance C_T decreases. In short, the capacitance can be controlled by the applied voltage. The variation of C_T with respect to the applied reverse bias voltage is shown in the Fig. 1.19.

As reverse voltage is negative, graph is shown in the second quadrant. For a particular diode shown, C_T varies from 80 pF to less than 5 pF as V_R changes from 2V to 15 V.

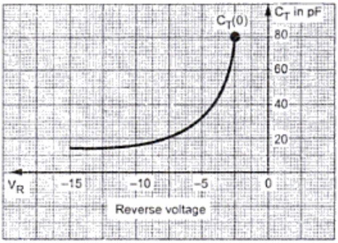
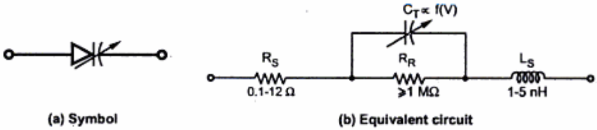


Fig. 1.19

In practice, special type of diodes are manufactured which shows the transition capacitance property more predominantly as compared to the normal diodes. Such diodes are called **varactor diodes, varicap , VVC** (voltage variable capacitance), or **tuning diodes.**

1.4.1 Symbol and Equivalent Circuit

The Fig. 1.20 (a) shows the symbol of varactor diode while the Fig. 1.20 (b) shows the first approximation for its equivalent circuit in the reverse bias region.



(a) Symbol (b) Equivalent circuit

Fig. 1.20 Varactor diode

The R_R is the reverse resistance which is very large while R_S is the geometric resistance of diode which is very small. The inductance L_S indicates that there is a high frequency limit associated with the use of varactor diodes.

1.4.2 Expression for Transition Capacitance

For a varactor diode, the transition capacitance in terms of applied reverse bias voltage is given by,

$$\boxed{C_T = \frac{K}{(V_J + V_R)^n}}$$

where K = Constant depends on semiconductor material and construction technique

V_J = Junction potential

V_R = Magnitude of reverse bias voltage

$n = \frac{1}{2}$ for the alloy junctions

$= \frac{1}{3}$ for the diffused junctions

At the zero bias condition the capacitance is C(0). Interms of C(0), the transition capacitance is given by,

$$\boxed{C_T = \frac{C(0)}{\left[1+\left|\frac{V_R}{V_J}\right|\right]^n}}$$

1.4.3 Effect of Temperature

The varactor diodes have positive temperature coefficient i.e. C_T value increases by small amount as the temperature increases.

1.4.4 Data Sheet Information of Varactor Diode

The data sheet of a varactor diode consists of the maximum ratings and its electrical characteristics. The table 1.1 shows the range of nominal diode capacitance C_T from 6.8 pF to 47 pF, for series of 1N5139 - 1N5148 varactor diodes, measured at V_R = 4 V d.c.

Device type	C_T V_R = 4V, f = 1 MHz pF			Q value V_R = 4 V d.c. f = 50 MHz	T_R Tuning ratio C_4/C_{60} f = 1 MHz	
	Min	Typ	Max	Min	Min	Typ
1N 5139	6.1	6.8	7.5	350	2.7	2.9
1N 5140	9.0	10	11	300	2.8	3.0
1N 5141	10.8	12	13.2	300	2.8	3.0
1N 5142	13.5	15	16.5	250	2.8	3.0
1N 5143	16.2	18	19.8	250	2.8	3.0
1N 5144	19.8	22	24.2	200	3.2	3.4
1N 5145	24.3	27	29.7	200	3.2	3.4
1N 5146	29.7	33	36.3	200	3.2	3.4
1N 5147	36.1	39	42.9	200	3.2	3.4
1N 5148	42.3	47	51.7	200	3.2	3.4

Table 1.1

Capacitance tolerance range : The capacitance values are based on 10% tolerance range. For example, varactor diode 1N 5144 shows a variation in C_T from 19.8 pF to 24.2 pF, at V_R = 4 V d.c. So it can show any value between 19.8 pF and 24.2 pF at V_R = 4 V d.c.

Tuning Ratio : This is also called **capacitance ratio** as it is a ratio of the varactor diode capacitance at a minimum reverse voltage to the maximum reverse voltage. This ratio is not related to the tolerance range. For example, if C_T of 1N5148 diode at V_R = 4V (min) is divided by C_T of 1N 5148 diode at V_R = 60 V(max), the ratio gives value as 3.4, called tuning ratio. This is indicated as C_4/C_{60} in the table 1.1.Thus C_T at V_R = 4V is 3.2 times higher than the C_T at V_R = 60 V.

Now C_4 = 47 pF at V_R = 4V for 1N 5148 varactor diode, and its tuning ratio (TR) is 3.2.

$$\therefore \quad TR = \frac{C_4}{C_{60}} = 3.2 = \frac{47\text{pF}}{C_{60}}$$

$$\therefore \quad C_{60} = 14.6875 \text{ pF}$$

So C_T values from 14.6875 pF to 47 pF for this diode, as V_R is changed from 60V to 4V. This gives flexibility to select the diode in the various tuning circuits. The tuning ratio depends on abruptness of the p-n junction. Many hyper-abrupt varactor diodes give TR value, ranging between 10 to 15.

Quality factor (Q) : The quality factor of a reactive element either capacitor or inductor is the ratio of energy stored and returned by the element to the energy dissipated in the device resistance. It is also called **figure of merit.** Thus Q = 300 means capacity of an element to store and return the energy is 300 times more than the energy lost in its resistance. Thus higher Q values is desirable. For varactor diodes, the Q value increases with increase in reverse voltage.

Temperature coefficient (TC) : This indicates dependence of C_T on temperature. Varactor diodes have positive TC i.e. C_T value increases by a small amount as the temperature increases. While the quality factor has negative temperature coefficient i.e. Q decreases with increase in temperature.

The table 1.2 gives maximum ratings for 1N 5139 - 1N 5148 varactor diodes.

Rating	Symbol	Value	Unit
Reverse voltage	V_R	60	Volts
Forward current	I_F	250	mA
RF power input*	P_{in}	5.0	watts
Device dissipation at T_A = 25°C	P_D	400	mW
Derate above 25°C		2.67	mW/°C

Device dissipation at T_C = 25°C	P_C	2.0	watts
Derate above 25°C		13.3	mW/°C
Junction temperature	T_J	+ 175	°C
Storage temperature range	T_{stg}	– 65 to + 200	°C

Table 1.2 Maximum rating (T_C = 25 °C unless otherwise noted)

* The RF power input rating assumes that an adequate heatsink is provided.

The Table 1.5 gives the electrical characteristics for 1N 5139 - 1N 5148 varactor diodes.

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse breakdown voltage (I_R = 10 µA dc)	$V_{(BR)\ R}$	60	70	-	V dc
Reverse voltage leakage current (V_R = 55 V dc T_A = 25°C)	I_R	-	-	0.02	µA dc
(V_R = 55 V dc, T_A = 150°C)		-	-	20	
Series inductance (f = 250 MHz)	L_S	-	5.0	-	nH
Case capacitance (f = 1.0 MHz)	C_C	-	0.25	-	pF
Diode capacitance temperature coefficient (V_R = 4.0 V dc. f = 1.0 MHz)	TC_C	-	200	300	ppm/°C

Table 1.3 Electrical characteristics (T_A = 25 °C unless otherwise noted)

1.4.5 Applications

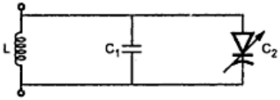


Fig. 1.21 Use of varactor diode in LC tuned circuit

The main application of varactor diodes is LC tuned circuits.

Fig. 1.21 shows how varactor diode can be connected in a LC tuned circuits. The resonance frequency for a parallel LC tuned circuit is given by,

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

As varactor diode is connected in parallel, the resultant capacitance becomes $C_1 + C_2$.

Hence the resonance frequency becomes,

$$f_r = \frac{1}{2\pi\sqrt{L(C_1 + C_2)}}$$

where C_2 is transistion capacitance of varactor diode. The value of C_2 can be changed by controlling the voltage applied to the circuit. Hence circuit can be tuned by changing voltage applied at a resonance frequency, this is called **electrical tuning.**

The various other applications of varactor diodes are,

1. Tuned circuits
2. FM modulators
3. Automatic frequency control devices
4. Adjustable bandpass filters
5. Parametric amplifiers
6. Television receivers

➡ **Example 1.2 :** *Determine the transition capacitance of a diffused junction varactor diode at a reverse bias voltage of 4.2 V if C(0) = 80 pF and junction potential of 0.7 V. Also calculate constant K for diode.*

Solution : The transition capacitance is given by,

$$C_T = \frac{C(0)}{\left[1+\left|\frac{V_R}{V_J}\right|\right]^n}$$

Now $$C(0) = 80\text{ pF}, n = \frac{1}{3} \text{ as diffused junction}$$

$$V_R = 4.2\text{ V}, V_J = 0.7\text{ V}$$

$$\therefore \quad C_T = \frac{80\times 10^{-12}}{\left[1+\left|\frac{4.2}{0.7}\right|\right]^{1/3}} = \mathbf{41.82\ pF}$$

The transition capacitance is also given by,

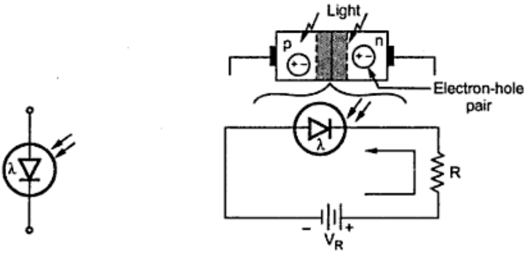
$$C_T = \frac{K}{[V_R + V_J]^n}$$

$$\therefore \quad 41.82\times 10^{-12} = \frac{K}{[4.2+0.7]^{1/3}}$$

$$\mathbf{K = 71.03\times 10^{-12}}$$

1.5 Photodiode

The photodiode is a semiconductor p-n junction device whose region of operation is limited to the reverse biased region. The Fig. 1.22 (a) shows the symbol of photodiode while the Fig. 1.22 (b) shows the working principle of photodiode.



(a) Symbol (b) Principle of operation

Fig. 1.22 Photodiode

The photodiode is connected in reverse biased condition. The depletion region width is large. Under normal condition, it carries small reverse current due to minority charge carriers. When light is incident through glass window on the p-n junction, photons in the light bombard the p-n junction and some energy is imparted to the valence electrons. Due to this, valence electrons are dislodged from the covalent bonds and become free electrons. Thus more electron-hole pairs are generated. Thus total number of minority charge carriers increases and hence the reverse current increases. This is the basic principle of operation of photodiode.

1.5.1 Photodiode Characteristics

The photodiode is designed such that it is sensitive to the light.

When there is no light, the reverse biased photodiode carries a current which is very small and called **dark current**. It is denoted as I_λ. It is purely due to thermally generated minority carriers. When light is allowed to fall on a p-n junction through a small window, photons transfer energy to valence electrons to make them free. Hence reverse current increases. It is proportional to the light intensity. The Fig. 1.23 shows the photodiode characteristics. The Fig. 1.23 (a) shows the relation between reverse current and light intensity while the Fig. 1.23 (b) shows relation between reverse voltage and reverse current at different light intensities. It can be seen that reverse current is **not dependent** on reverse voltage and totally depends on light intensity.

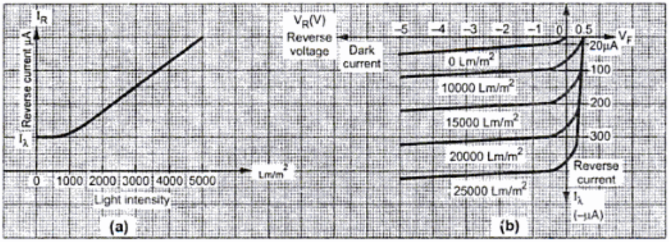


Fig. 1.23 Photodiode characteristics

1.5.2 Use of Photodiode as Variable Resistance Device

Consider a typical photodiode with dark current $I_\lambda = 20\ \mu A$ at $V_R = -2V$

$$\therefore \text{ Dark resistance } = \frac{V_R}{I_\lambda} = \frac{2}{20\mu A} = 100\ k\Omega$$

If now photodiode is illuminated with 25000 Lm/m^2 (Lumens per square metres) then current changes to 350 μA at same reverse voltage.

$$\therefore \text{ Illuminated resistance } = \frac{2}{350\mu A} = 5.714\ k\Omega$$

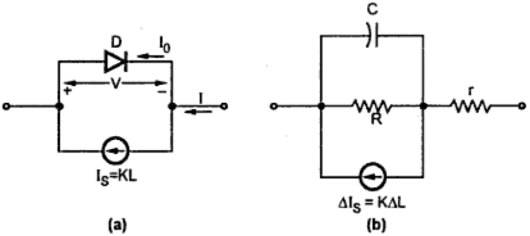
This shows that the photodiode can be used as a **variable resistance device** controlled by light intensity. It is also called **photoconductive device**. The response of photodiode is very fast hence change in resistance from high to low or otherwise is also very fast. Hence it can be used in variety of applications.

1.5.3 Why to be used in Reverse Biased ?

The reverse current without light in diode is in the range of μA. The change in this current due to the light is also in the range of μA. Thus such a change can be significantly observed in the reverse current. If the photodiode is forward biased, the current flowing through it is in mA. The applied forward biased voltage takes the control of the current instead of the light. The change in forward current due to light is negligible and can not be noticed. The resistance of forward biased diode is not affected by the light. Hence to have significant effect of light on the current and to operate photodiode as a variable resistance device, it is always connected in reverse biased condition.

1.5.4 Small Signal Model of Photodiode

The Fig. 1.24 shows the small signal model for photodiode. In Fig. 1.24 (a) a photodiode is represented by an ideal junction diode in parallel with a current source which is proportional to the light intensity. The model in the Fig. 1.24 (b) assumes that the



(a) (b)

Fig. 1.24 Small signal models for photodiode

diode is heavily reversed biased, and hence that the diode may be replaced by its reverse resistance R. This model also includes the effect of barrier capacitance C and the ohmic resistance r. The typical values for barrier capacitance, reverse resistance and ohmic resistance are of the order of

$$C \approx 10 \text{ pF}, \qquad R \approx 50 \text{ M}\Omega, \qquad r \approx 100\ \Omega$$

In both the figures, the symbol L represents light flux in lumens, and K is a proportionality constant in the range 10 to 50 mA/lumen.

1.5.5 Sensitivity with Position of Illumination

We know that the current in a reverse biased semiconductor photodiode depends upon the diffusion of minority carriers to the junction. If the radiation is focused into a small spot far away from the junction, the injected minority carriers may recombine before diffusing to the junction. This results in a much smaller current. On the other hand, if the radiation is focused from near the junction more current will result. Therefore, we can say that the photocurrent is a function of the distance from the junction at which the light spot is focused. This is illustrated in the graph shown in the Fig. 1.25.

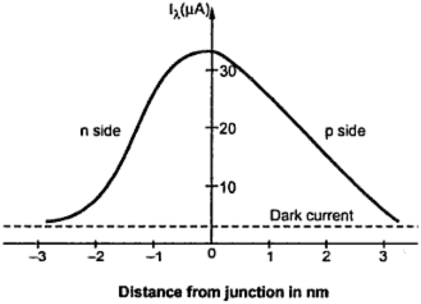


Fig. 1.25 Sensitivity of photodiode as a function of position of illumination

1.5.6 Photodiode as a Voltage Cell

When the photodiode is illuminated without any biasing, there is increase in the number of holes in the p-side and the number of electrons in the n-side. Due to this, minority carriers are swept across the junction. We know that, the barrier potential is negative on the p-side and positive on the n-side. This barrier potential tends to reduce because of the flow of minority carriers. When an external circuit is connected across the diode terminals, the minority carriers will return to the original side via the external circuit. The electrons which crossed the junction from p to n will now flow out through the n terminal and into the p-terminal. This means that the device is behaving as a voltage cell with the n-side being the negative terminal and the p-side the positive terminal. Thus, the photodiode is a **photovoltaic** device as well as a **photoconductive** device.

1.5.7 Advantages

The advantages of photodiode are,

1. Can be used as variable resistance device.
2. Highly sensitive to the light.
3. The speed of operation is very high. The switching of current and hence the resistance value from high to low or otherwise is very fast.

1.5.8 Disadvantages

The various disadvantages of photodiode are,

1. The dark current I_λ is temperature dependent.
2. The overall photodiode characteristics are temperature dependent hence have poor temperature stability.
3. The current and change in current is in the range of μA which may not be sufficient to drive other circuits. Hence amplification is necessary.

1.5.9 Photodiode Applications

The two commonly used systems using photodiode are alarm system and a counting system.

The Fig. 1.26 shows a photodiode employed in an alarm system.

The reverse current I_λ continues to flow as long as light beam is incident on the photodiode. When the light is interrupted, the current I_λ drops to the dark current level. This initiates the alarm system sounding the alarm.

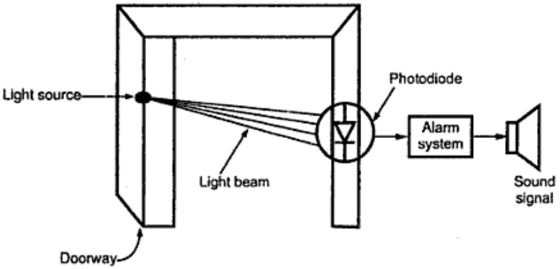

Light source
Photodiode
Alarm system
Light beam
Sound signal
Doorway

Fig. 1.26 Photodiode in an alarm system

The Fig. 1.27 shows a photodiode used to count the items on a conveyor belt. As each item passes, the light beam is broken. Thus reverse current I_λ drops to the dark current level. This activates the counting mechanism and the counter is increased by one.

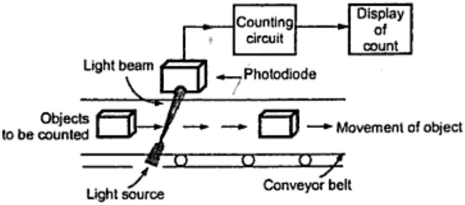

Counting circuit
Display of count
Light beam
Photodiode
Objects to be counted
Movement of object
Light source
Conveyor belt

Fig. 1.27 Photodiode in the counter operation

1.5.10 Photodiode Control Circuit

The Fig. 1.28 shows the typical photodiode control circuit. When there is no light incident on the photodiode, the current through the photodiode is negligible, dark current.

Part of this current is a current through R_2. Such a small current through R_2 keeps the voltage drop across R_2 low, making transistor and relay 'OFF'. When light is incident on the photodiode the current through diode and hence the current through R_2 is sufficient to forward bias both the junctions, making transistor and relay 'ON'.

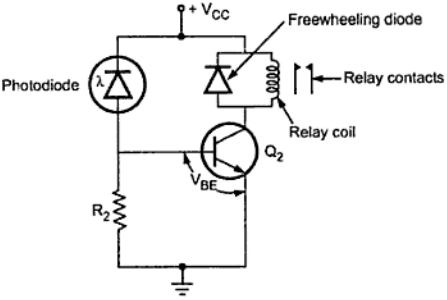


Fig. 1.28 Photodiode control circuit

1.6 Schottky Diode

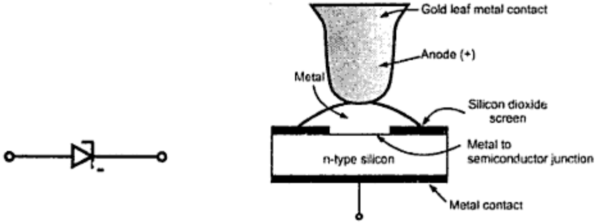
At low frequencies the conventional diode can be easily turn off by changing its bias from forward to reverse. But at very high frequencies conventional diode shows a tendency to store the charge and there is noticeable current in reverse half cycle. During forward biased it is not possible for all the carriers in depletion region to recombine. Some carriers exist in depletion region which are not recombined. Now if the diode is suddenly reverse biased, the carriers existing in depletion region can flow in the reverse direction for some time. But for large life time of these carriers, longer is the flow of current in reverse half cycle. Hence there is a limitation on the frequency range for which a conventional diode can be used.

The time taken by a diode to turn off from its forward biased state is called reverse recovery time. For frequencies upto 10 MHz it is very small but above 10 MHz it is large and puts a limit on the use of conventional diode in such high frequency applications.

The diodes which are specially manufactured to solve this problem of fast switching are called Schottky diodes. Its construction is different than the conventional p-n junction diode. It consists of a metal to semiconductor junction as shown in the Fig. 1.29 (b). These diodes are also called **Schottky barrier diodes, surface barrier diodes** or **hot carrier diodes**. The symbol for the Schottky diode is shown in the Fig. 1.29 (a).

Usually n-type silicon is used as a semiconductor. Different metals, such as molybdenum, platinum, chrome or tungsten are used with different construction techniques to get different set of characteristics such as increased frequency range, lower forward bias etc.

In both the materials metal as well as n-type semiconductor the electrons are the majority carriers. In the metal, the minority carriers (holes) are very less in number. When the contact is made between the two materials, the electrons from the n-type



(a) Symbol (b) Construction

Fig. 1.29 Schottky diode

semiconductor material immediately flow into the adjoining metal. This is because the kinetic energy level of the majority carriers i.e. electrons in the n region is higher than the electrons in the metal. Hence a heavy flow of majority carriers is established from n region to the metal. Due to high kinetic energy the injected carriers are called **hot carriers**.

In conventional diode, the minority carriers get injected into adjoining region while in Schottky diode, majority carriers get injected into metal.

Key Point *Thus in a conventional diode the conduction is due to minority and majority carriers while in Schottky diode the conduction is totally by majority carriers.*

The heavy flow of electrons into the metal creates a region near the junction surface, depleted of carriers in the silicon material. This is similar to depletion region in a conventional diode. The additional carriers in the metal establish a negative wall in the metal at the boundary between the two materials. This results in further current. So there exists a carrier free region and a negative wall at the surface of the metal.

1.6.1 Characteristics of Schottky Diode

Due to the minority carrier free region, Schottky diode cannot store the charge. Hence due to lack of charge storage, it can switch off very fast than a conventional diode. It can be easily switched off for the frequencies above 300 MHz. The barrier at the junction for a Schottky diode is less than that of normal p-n junction diode, in both forward and reverse bias region. The barrier potential and breakdown voltage in forward bias and reverse bias region respectively are also less than p-n junction diode. The barrier potential of Schottky diode is 0.25 V as compared to 0.7 V for normal diode. The Fig. 1.30 shows the comparison of characteristics of Schottky diode and a conventional p-n junction diode.

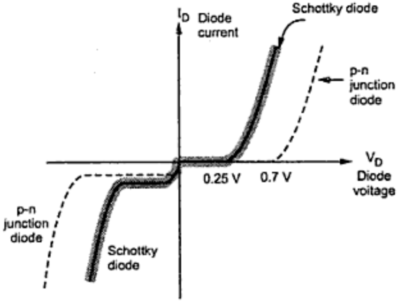
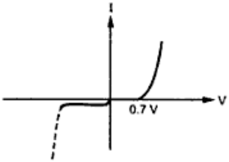
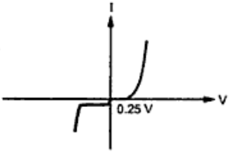


Fig. 1.30 Comparison of characteristics

1.6.2 Applications

Due to fast switching characteristics, the Schottky diodes are very useful for high frequency applications such as digital computers, high speed TTL, radar systems, mixers, detectors in communication equipments and analog to digital converters.

1.6.3 Comparison between Schottky Diode and Conventional Diode

Parameter	p-n junction diode	Schottky diode
Junction	Semiconductor to semiconductor	Semiconductor to metal
Carriers	Minority and majority	Only majority
Reverse recovery time	More	Less
Barrier potential	More about 0.7 V	Less about 0.25 V
Breakdown voltage	More	Less
Switching speed	Less	High
PIV rating	More	Less
Frequency range	Upto 10 MHz	Very high more than 300 MHz
Characteristics		

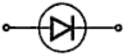
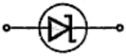
Symbol		
Application	Mainly rectifiers and low frequency devices	High frequency devices digital computers, radar systems, Schottky TTL logics, mixers etc.

Table 1.4

1.6.4 Specifications of Schottky Diode

The specifications and typical values for the small signal Schottky BAT 49 are given below. The device is having low turn on voltage and fast switching.

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		80	V
I_F	Forward continuous current*	$T_a = 70°C$	500	mA
I_{FRM}	Repetitive peak forward current*	$t_p = 1s$ $\delta \leq 0.5$	3	A
I_{FSM}	Surge non repetitive forward current*	$t_p \leq 10$ ms	10	A
T_{stg} T_j	Storage and junction temperature range		– 65 to 150 – 65 to 125	°C °C

Table 1.5 Absolute ratings (limiting values)

Electrical characteristics

a) Static characteristics

Symbcl	Test conditions	Min.	Typ.	Max.	Unit
I_R **	$T_j = 25°C$ $V_R = 80$ V			200	μA
V_F **	$T_j = 25°C$ $I_F = 10$ mA			0.32	V
	$T_j = 25°C$ $I_F = 100$ mA			0.42	
	$T_j = 25°C$ $I_F = 1$ A			1	

b) Dynamic characteristics

Symbol	Test conditions	Min.	Typ.	lax.	Unit
C	$T_j = 25°C$ f = 1 MHz $V_R = 0$ V		120		pF
	$V_R = 5$ V		35		pF

* On finite heat sink with 4 mm lead length.

** Pulse test $t_p \le 300 \mu s$, $\delta < 2\%$

1.7 Tunnel Diode

A normal p-n junction has an impurity concentration of about 1 part in 10^8. This much amount of doping has the depletion layer width of about 5 microns i.e. 5×10^{-4}cm. The diodes in which the concentration of impurity atoms is greatly increased upto 1 part in 10^3, to get completely changed characteristics, are called as Tunnel diodes. These diodes are first introduced by Leo Esaki in 1958.

Due to the heavy doping the depletion region gets reduced considerably, of the order of 10^{-6}cm i.e. about 1/100 the width of depletion region in normal p-n junction diode. Due to the thin depletion region, an electron penetrates through the barrier. This is called as tunneling and hence such high impurity density p-n junction devices are called as tunnel diodes. Many carriers in tunnel diodes penetrate the barrier at velocities far more than the velocities available in the conventional diodes, at low forward bias voltages. Due to such effect, it shows a negative resistance region in its volt-ampere characteristics. This negative resistance region is the most important feature of a tunnel diode.

1.7.1 Characteristics of a Tunnel Diode

The Fig. 1.31 shows the volt-ampere characteristics of a tunnel diode.

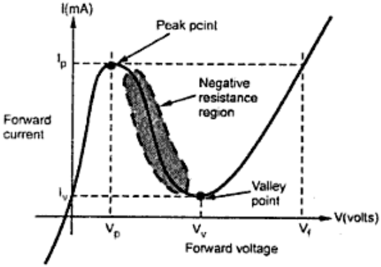


Fig. 1.31 Characteristics of tunnel diode

For small forward voltages (upto 50 mV for germanium) the resistance remains small, of the order of 5 Ω and current increases. The current attains a peak value I_p corresponding to the voltage V_p which is about 600 mV. The I_p can vary from few micro amperes to several hundred amperes.

At the peak point, the slope dI/dV of the characteristics becomes zero. If now the forward voltage is increased further, beyond V_P, then the current starts decreasing rather than increasing. Thus the dynamic conductance dI/dV becomes negative. Hence the dynamic resistance dV/dI is negative and it shows negative resistance characteristics. This negative resistance continues till a voltage V_v called as **valley voltage**.

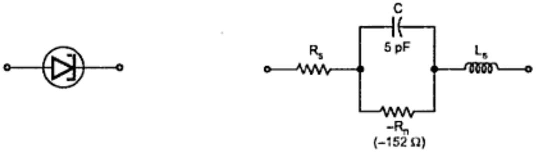
At the valley voltage V_v, the current is I_v and slope dI/dV becomes again zero.

After V_v, if the voltage is increased, the current again increases. Thus resistance again becomes positive and remains positive thereafter.

At the socalled peak forward voltage V_f, the current again reaches the value equal to **peak current I_p**.

The value of current between I_p and I_v can be obtained with three different voltage values. For the value of current between I_p and I_v, the characteristics is triple values. This multivalued feature makes the tunnel diode useful in the pulse and digital circuits.

The circuit symbol of a tunnel diode is shown in the Fig. 1.32 (a) while its equivalent circuit in the negative resistance region is shown in the Fig. 1.32 (b).



(a) Symbol

(b) Equivalent circuit in negative resistance region

Fig. 1.32 Tunnel diode

The negative resistance $-R_n$ has a minimum at the point of inflection between I_p and I_v. The series resistance R_s is due to ohmic contact resistance. The series inductance L_s depends upon the lead length and the geometry of the diode package. The junction capacitance C depends upon the bias represents the junction diffusion capacitance and is usually measured at the valley point.

1.7.2 Construction

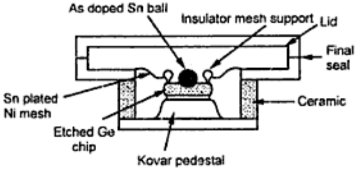


Fig. 1.33 Construction of tunnel diode

The most common commercially available tunnel diodes are made from the germanium or gallium arsenide. The basic construction of an advanced design tunnel diode is shown in the Fig. 1.33.

1.7.3 Load Line for Tunnel Diode

Consider a circuit as shown in the Fig. 1.34. The supply voltage is V and R is the load resistance.

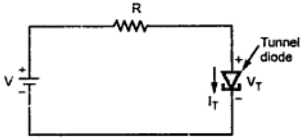


Fig. 1.34

The drop across the tunnel diode is V_T. Applying KVL,

$$V = I_T R + V_T$$

$$\therefore \quad I_T = -\frac{1}{R} V_T + \frac{V}{R} \qquad \dots (1)$$

So when $I_T = 0$, $V_T = V$ while when $V_T = 0$, $I_T = \frac{V}{R}$. Using these two points a load line can be obtained on V-I characteristics of tunnel diode as shown in the Fig. 1.35.

The load line intersects the characteristics at the three points A, B and C. The load line position and the slope is completely dependent on the network elements and tunnel diode characteristics.

The points A and C are stable operating points as located in positive resistance region of characteristics. While point B is in the negative resistance region and hence unstable operating point.

An important point regarding stable points A and C is that if there is slight change in the network conditions there will not be any change in the circuit behaviour and position of Q point for the circuit. If supply voltage increases then point C will move up on the

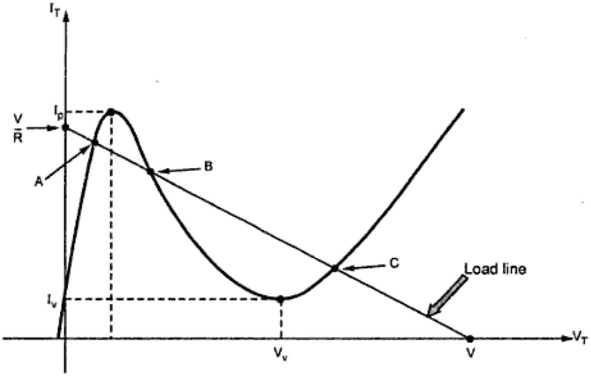


Fig. 1.35 Load line for tunnel diode circuit

curve as voltage across diode V_T will increase. When voltage decreases to original value, point C will regain its original position back.

But if operating point is defined at point B in the unstable region and if supply voltage slightly increases then correspondingly V_T increases but I_T decreases due to negative resistance characteristics. This further reduces V_T and process continues till point shifts into stable region at point C. If supply voltage slightly decreases, point B moves up to achieve stable point A.

Thus point B can be defined as an operating point using load line concept but in practice it will get stabilized at the locations A or C.

This concept is used in a negative resistance oscillator using a tunnel diode.

1.7.4 Negative Resistance Oscillator using Tunnel Diode

The Fig. 1.36 shows a negative resistance oscillator using tunnel diode.

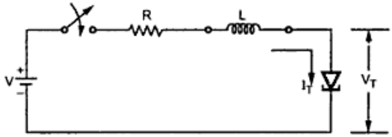


Fig. 1.36 Negative resistance oscillator using tunnel diode

The network elements are so designed to obtain the operating Q point at position 'O' as shown in the Fig. 1.37. This is the intersection point of load line with Tunnel diode characteristics. The design is such that the load line intersects the characteristics only at one point which is the Q point. A stable operating point is not at all defined.

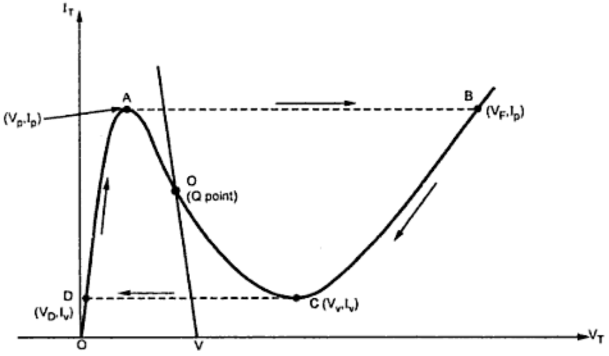


Fig. 1.37

Initially when switch is closed, the supply voltage starts increasing and at $V=V_p$, the current attains maximum value I_p. Now for $V>V_p$, according to the characteristics current must decrease.

But $$V = I_T R + I_T (-R_T) \qquad \text{... (2)}$$

As tunnel diode is operating with Q point in negative resistance region hence R_T is taken negative.

$\therefore$ $$V = I_T (R - R_T) \qquad \text{... (3)}$$

Hence I_T is decreasing and $R-R_T$ is also decreasing. But V is increasing beyond V_p. This is contradictory according to equations (3). Hence diode operating point switches from A to B, in that region where current can increase as voltage increases. But at point B, $V = V_F$ which is greater than V. To achieve this, the polarity of the transient voltage across the coil must reverse and current starts decreasing from B to C. Energy stored in the inductor while current has reached I_p, starts decreasing.

This decrease in current continues till the point of operation shifts to point C where current is I_v while voltage is V_v. Now this voltage is still more than V and hereafter current starts increasing again. But as inductor is discharging, current must decrease as voltage decreases. Hence it is not possible in practice to increase the current after point C but the point of operation shifts from point C to D where voltage is V_D and current is I_v.

This is a stable region where current can further decrease rather than increasing. But from point D onwards, tunnel current can again increase to I_P. Thus the process repeats on its own again and again, never settling at an operating point defined in an unstable region of characteristics. The result is the oscillator circuit with the help of a fixed supply and negative resistance characteristics of a Tunnel diode.

The voltage and current waveforms are shown in the Fig. 1.38 (a) and (b).

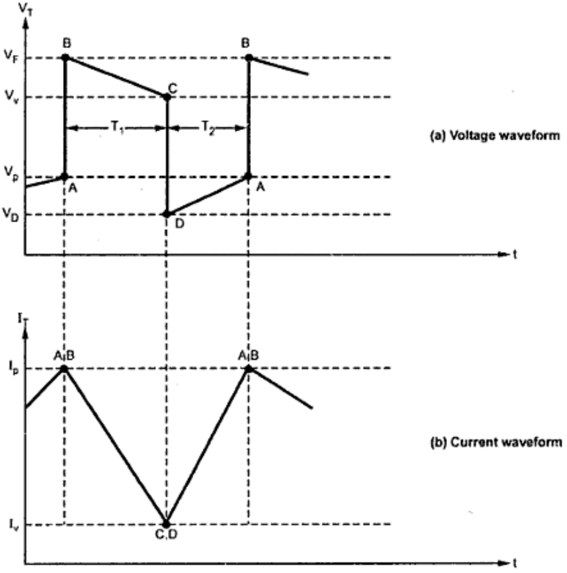


Fig. 1.38 Waveforms of negative resistance oscillator

Thus the square type waveform can be obtained using tunnel diode. The oscillator waveforms are not necessarily exactly symmetrical i.e. $T_1 \neq T_2$. This is because portions DA and BC are not identical.

Expression of Time Period T

Let R_1 = Tunnel diode resistance of the portion passing through origin.

R_2 = Tunnel diode resistance of the second positive resistance region.

then $R_T = R + R_2$ while $R'_T = R + R_1$ and R = load or circuit resistance.

The linear piecewise approximation of tunnel diode is shown in the Fig. 1.39.

Now $$V_Y = V' - V = V'_v - V - I_v R_2 \quad \ldots (4)$$

Then the time T_1 is given by,

$$T_1 = \frac{L}{R_T} \ln\left[\frac{V_Y + I_p R_T}{V_Y + I_v R_T}\right] \quad \ldots (5)$$

While the time T_2 is given by,

$$T_2 = \frac{L}{R'_T} \ln\left[\frac{V - I_v R'_T}{V - I_p R'_T}\right] \quad \ldots (6)$$

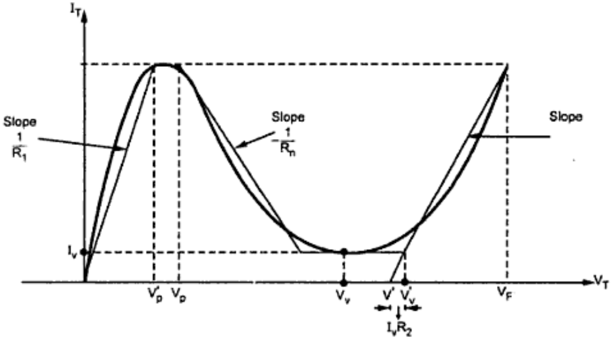


Fig. 1.39

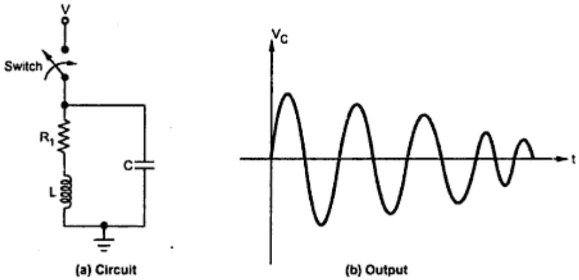
The total period is given by,

$$T = T_1 + T_2$$

while $$f = \frac{1}{T} = \text{frequency of oscillations}$$

1.7.5 Sinusoidal Oscillator using Tunnel Diode

The Fig. 1.40 (a) shows a tank circuit and a switch. The closing of the switch will result in a sinusoidal voltage that will decrease in amplitude with time. Thus it will produce damped output as shown in the Fig. 1.40 (b). The damping of the oscillator output is due to the dissipative characteristics of the resistive elements in the tank circuit.

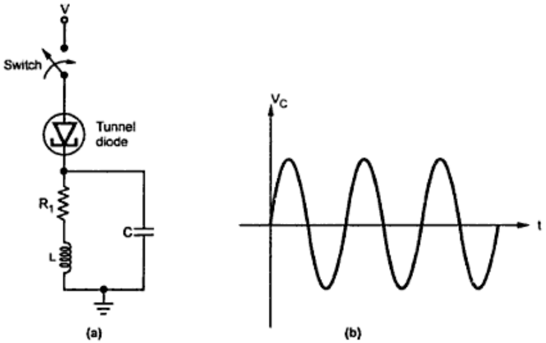


(a) Circuit (b) Output

Fig. 1.40 Oscillator

The dissipative characteristics of the resistance must be compensated to produce pure sinusoidal output.

A tunnel diode can be placed in series with the tank circuit as shown in the Fig. 1.41 (a). It must be operated in its negative resistance region. This will compensate the resistive characteristics of the tank circuit to produce the undamped purely sinusoidal response as shown in the Fig. 1.41 (b).



(a) (b)

Fig. 1.41 Sinusoidal oscillator with tunnel diode

1.7.6 Advantages of Tunnel Diode

The advantages of a tunnel diode are :

1. Environmental immunity i.e. the peak point (V_p, I_p) is not a sensitive function of temperature.
2. Low cost.
3. Simplicity i.e. a tunnel diode can be used along with a d.c. supply and few passive elements to obtain various application circuits.
4. Low noise.
5. High speed i.e. the tunneling takes place at the speed of light hence the switching times of the order of a nanosecond are easily obtained and switching times as low as 50 psec also can be obtained.
6. Low power consumption.

The only disadvantage of this diode are its low output voltage swing and it is a two terminal device. Hence there is no isolation between input and output. Hence transistor is used alongwith a tunnel diode for frequencies below 1 GHz.

1.7.7 Other Applications of Tunnel Diode

The various other applications of tunnel diode are,

1. As a high speed switch.
2. In pulse and digital circuits.
3. In negative resistance and high frequency (microwave) oscillator.
4. In switching networks.
5. In timing and computer logic circuitry.
6. Design of pulse generators and amplifiers.

1.7.8 Comparison of Tunnel Diode and Conventional Diode

The comparison of tunnel diode and conventional p-n junction diode is given below.

Sr. No.	Tunnel diode	Conventional p-n junction diode
1.	Impurity concentration is high about 1 part in 10^3 atoms.	Impurity concentration is low about 1 part in 10^8 atoms.
2.	Depletion region width is about 5 microns, which is 1/ 100th the width of typical p-n junction diode.	The width of depletion region is high compared to the tunnel diode.
3.	The carrier velocities are very high at low forward bias, hence can punch through the depletion region.	The carrier velocities are low at low forward bias, hence can not penetrate the depletion region.

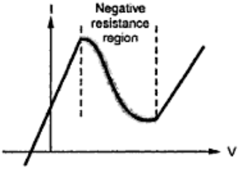
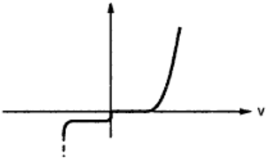
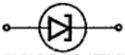
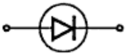
4.	The V-I characteristics shows the negative resistance region.	The V-I characteristics does not show the negative resistance region.
5.	The V-I characteristics is,  	The V-I characteristics is, 
6.	The materials used for construction are germanium or gallium arsenide.	The silicon is most popularly used.
7.	The symbol is, 	The symbol is, 
8.	The switching time is very low of the order of nano to picoseconds.	The switching time is high.
9.	Used for high frequency oscillators, high speed applications such as computers, pulse and digital circuits and switching networks.	Used in rectifiers and other general purpose applications.

Table 1.6

1.7.9 Specifications of Tunnel Diode

The important specifications and typical values for a tunnel diode are,

Specifications	Typical values
Forward current (I_F)	About 5 mA
Reverse current (I_R)	About 10 mA
Peak current (I_p)	About 1 mA
Peak voltage $\left(V_p\right)$	About 65 mV
Valley current $\left(I_V\right)$	About 0.1 mA
Valley voltage $\left(V_V\right)$	About 350 mV
Capacitor	5 to 10 pF

Table 1.7 Specifications of tunnel diode

1.8 Transistor as a Switch

Transistors are widely used in digital logic circuits and switching applications. In these applications, the voltage levels periodically alternate between a "Low" and a "High" voltage, such as 0 V and +5 V.

In switching applications, the transistor operates either in cut off region or saturation region. It is connected in common emitter configuration as shown in the Fig. 1.42.

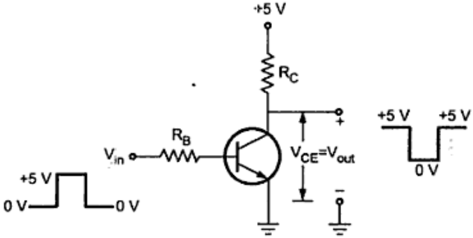
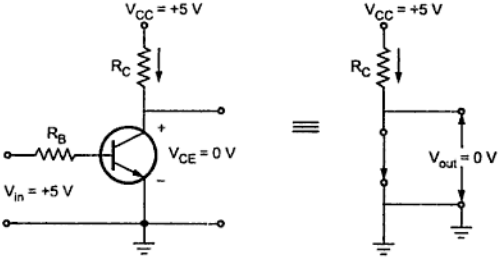


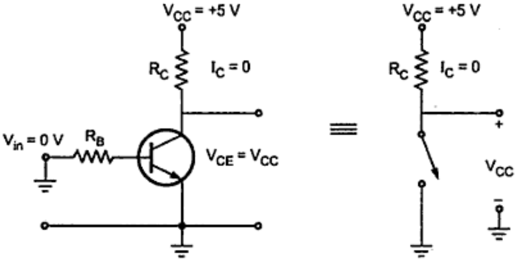
Fig. 1.42 Transistor as a switch

In this circuit, when input is HIGH, base current flows and it is greater than $\frac{I_c}{\beta}$, hence transistor is operated in saturation. In saturation condition, voltage between collector and emitter, $V_{CE(sat)}$ is typically 0.2 V to 0.3 V and hence transistor acts as closed switch. This is illustrated in Fig. 1.43.



Transistor saturated Fig. 1.43 Switch ON (Close)

When input is LOW, base current and collector current is zero and hence transistor is operated in cut off. In cut off V_{CE} = V_{CC} and transistor acts as open switch. This is illustrated in Fig. 1.44.


VCC = +5 V
RC
IC = 0
Vin = 0 V
RB
VCE = VCC
≡
VCC = +5 V
RC
IC = 0
+
VCC
−

Transistor cut off **Fig. 1.44** **Switch OFF (Open)**

Transistor Switching Times

When a transistor is used as a switch, it is usually made to operate alternately in the cutoff condition and in the saturation condition.

The switching speed of the transistor is an important quantity when transistor is used as a switch. Let us see Fig. 1.45. When the base input current is applied, the transistor does not switch on immediately. This is because of the junction capacitance and the transition time of electrons across the junctions. The time between the application of the input pulse and the commencement of collector current flow is termed as **delay time** t_d, and the time required for I_C to reach 90 % of its maximum level from 10 % level is called the **rise time** t_r. Thus the turn-on time t_{ON} is the addition of t_r and t_d ($t_{ON} = t_d + t_r$).

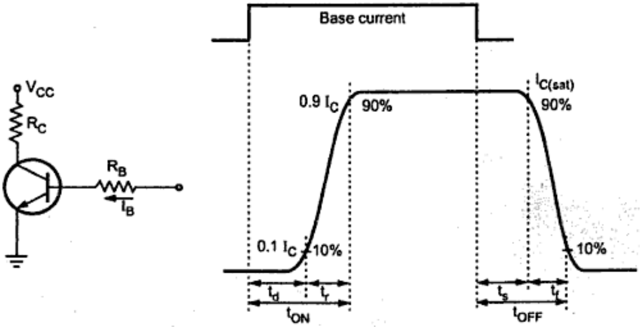

VCC
RC
RB
IB
Base current
0.9 IC
90%
IC(sat)
90%
0.1 IC
10%
10%
td
tr
tON
ts
tf
tOFF

Fig. 1.45 Transistor turn-ON and turn-OFF times

Similarly when input current I_B is switched OFF, I_C does not go to zero level immediately. It goes to zero level after turn off time, which is the sum of **storage time t_s** and **fall time t_f** as shown in the Fig. 1.45. The fall time is specified as the time required for I_C to go from 90 % to 10 % of its maximum level.

Delay Time

It is the time that elapses the application of the input pulse and current to rise to 10 percent of it maximum (saturation) value $I_{C\ sat} \approx V_{CC}/R_C$. The delay time exists due to following reasons.

- When the driving signal is applied to the transistor input, a nonzero time is required to charge up the emitter junction transition capacitance so that the transistor may be brought from cut off to the active region.
- Even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a time interval is required before these carriers can cross the base region to the collector junction and be recorded as collector current.
- Finally some time is required for the collector current to rise to 10 percent of its maximum.

Rise Time and Fall Time

The time required for I_C to reach 90% of its maximum level from 10% level is called the **rise time** (t_r), and time required for I_C to go from 90% to 10% of its maximum level is called **fall time** (t_f). The rise time and the fall time are due to the fact that, if a base current step is used to saturate the transistor or return it from saturation to cutoff, the transistor collector current must traverse the active region. The collector current increases or decreases along an exponential curve whose time constant is τ_r. It is given by

$$\tau_r = h_{FE}(C_C R_C + 1/\omega_T)$$

where C_C is the collector transition capacitance and ω_T is the radian frequency at which the current gain is unity.

Storage Time

When transistor is in saturation, it has excess minority carries stored in the base. The transistor cannot respond until this saturation excess charge has been removed. Due to this there is a finite time elapses between the transition of the input wavefrom and the time when collector current has dropped to 90 percent of I_C(sat) and it is referred to as **storage time** (t_s)

Review Questions

1. *What is LED ? Which material is used for LED ?*
2. *Explain the basic operating principle of LED.*
3. *Explain the construction of LED in brief.*
4. *State the advantages and disadvantages of LED.*
5. *Compare LED and normal p-n junction diode.*
6. *Sketch the output characteristics of LED and comment on it.*
7. *Why LEDs are preferred in displays ?*
8. *If a LED is forward biased for a supply of 10 V with a series resistance of 680 Ω, calculate the LED current.* **(Ans. : 11.8 mA)**
9. *Draw and explain the radiation pattern of a LED.*
10. *Define the following for LED :*
    a) Radiant intensity b) Irradiance
11. *Explain seven segment configuration of LEDs to display a number code.*
12. *Explain two types of seven segment display.*
13. *Draw the display of number 1 using seven segment display and explain the working of seven segment display.*
14. *What is varactor diode ? Explain.*
15. *How capacitance of diode vary with the reverse voltage ?*
16. *Draw the symbol and equivalent circuit of a varactor diode.*
17. *State the expression for transition capacitance of a varactor diode, giving the meaning of each symbol in it.*
18. *Explain the use of varactor diode in tuned circuit. State other applications of varactor diode.*
19. *Explain the characteristics of a photodiode.*
20. *Explain in brief, any two applications of photodiode.*
21. *Explain the small signal model of a photodiode.*
22. *Draw and explain, photodiode control circuit.*
23. *Explain the use of photodiode as a voltage cell.*
24. *Why photodiode is used in reverse biased condition ?*
25. *State the advantages and disadvantages of a photodiode.*
26. *Explain the construction of Schottky diode.*
27. *Draw and explain the characteristics of Schottky diode.*
28. *Compare Schottkey diode and conventional p-n junction diode.*

29. *Draw and explain the characteristics of tunnel diode.*
30. *Derive the equation for a load line of tunnel diode and explain its significance.*
31. *Explain the working of negative resistance oscillator using tunnel diode.*
32. *State the advantages of tunnel diode.*
33. *Compare tunnel diode and conventional p-n junction diode.*
34. *Write a note on transistor as a switch.*
35. *Define delay time, storage time, rise time and fall time with respect to transistor.*

❑❑❑

2

Frequency Response

2.1 Introduction

Let us consider an audio frequency amplifier which operates over audio frequency range extending from 20 Hz to 20 kHz. The audio frequency amplifiers are used in everyday life. For example, they are used in radio receivers, to address large public meeting, annual social gathering of college, for various announcements to be made for passengers on railway platforms, etc.

Over the range of frequencies at which it is to be used, an amplifier should ideally provide the same amplification for all frequencies.. The degree to which this is done is usually indicated by a curve, known as **frequency response curve** of the amplifier. This curve is a plot of the voltage gain of an amplifier against the frequency of input signal. A typical frequency response of an RC coupled amplifier is illustrated in Fig. 2.1.

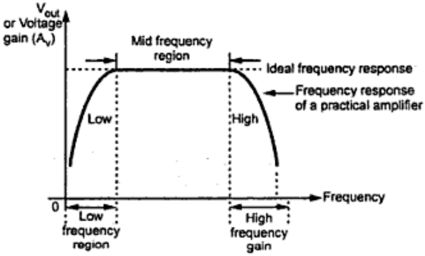


Fig. 2.1 A typical frequency response of an amplifier

To plot this curve, input voltage to the amplifier is kept constant and frequency of input signal is continuously varied. The output voltage at each frequency of input signal is noted; and the gain of the amplifier is calculated. The output voltage or the voltage gain of the amplifier is then plotted against frequency. For an A.F. amplifier, the frequency range of interest is quite large, from 20 Hz to 20 kHz. Hence to show clearly the voltage gain over such a wide frequency range, the frequency of input signal is plotted on x-axis using log scale (instead of usual linear scale). However the output voltage or voltage gain of the amplifier is plotted on y-axis with linear scale.

It is seen from the frequency response curve of an audio frequency amplifier that the gain of the amplifier remains fairly constant in the mid-frequency range, while the gain varies with frequency in low and high frequency regions of the curve. The frequency response is nearly ideal over a wide range of mid-frequency. Only at low and high frequency ends, the gain deviates from ideal characteristics. The decrease in voltage gain with frequency is called **roll-off.**

2.1.1 Definition of Cut-off Frequencies and Bandwidth

To indicate how constant an amplifiers's gain is with frequency variation, we may specify the range of frequencies over which the gain does not deviate more than 70.7 % of the maximum gain at some reference mid-frequency. This is shown in Fig. 2.2 where these two frequencies are indicated by f_1 and f_2 are called the **lower cut-off** and **upper cut-off** frequencies, respectively.

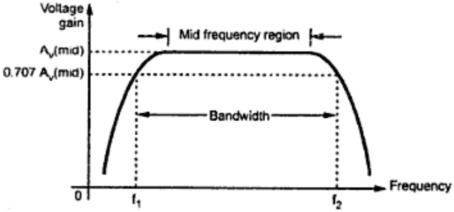


Fig. 2.2 Frequency response, half power frequencies and bandwidth of an RC coupled amplifier

Bandwidth of the amplifier is defined as the difference between f_2 and f_1; i.e. Bandwidth of the amplifier = $f_2 - f_1$. The frequency f_2 lies in high frequency region, while the frequency f_1 lies in low frequency region. These two frequencies are also referred to as half-power frequencies since gain or output voltage drops to 70.7 % of maximum value and this represents a power level of one-half the power at the reference frequency in mid-frequency region. Although this drop from maximum value to 70.7 % may seem to be large drop, the change is not easily noticeable to the listener, so that an amplifier may be considered to have a flat response from f_1 to f_2.

➡ **Example 2.1 :** *The voltage amplifier has voltage gain = 200 at cut-off frequencies. Find the maximum voltage gain.*

Solution : We know that maximum voltage gain of voltage amplifier is given as

$\therefore$ Maximum voltage gain = Gain at cut-off $\times \sqrt{2} = 200 \times \sqrt{2} =$ **282.84**

2.1.2 The Decibel Unit

The use of decibles to express gain. The basic for the decibel unit origins from the logarithmic response of the human ear to the intensity of sound. The decibel is a logarithmic measurement of the ratio of one power to another or one voltage to another. Usually, the voltage gain of the amplifier is represented in decibels (dBs). It is given by,

$$\text{Voltage gain in dB} = 20 \log A_v$$

The power gain in decibels is given by

$$\text{Power gain in dB} = 10 \log A_p$$

When A_v is greater than one, the dB gain is positive and when A_v is less than one, the dB gain is negative. The positive and negative signs of dB gain indicate the amplification and attenuation, respectively.

In amplifiers, a certain value of gain is assigned with 0 dB reference. This does not mean that the actual voltage gain is 1 (which is 0 dB), it means that the reference gain, no matter what its actual value, is used as a reference with which to compare other values of gain.

We have seen that the amplifiers exhibit a maximum gain over mid frequency range and a reduced gain at frequencies below and above this range. Usually, the maximum gain called the mid frequency range gain is assigned a 0 dB value. Any value of gain below mid frequency range can be referred to 0 dB and expressed as a negative dB value. For example, assume that mid frequency gain of a certain amplifeir is 100, then

$$\text{Voltage gain in dB} = 20 \log 100 = 20 \times 2 = 40 \text{ dB}$$

$$\text{At } f_1 \text{ and } f_2 \qquad A_v = \frac{100}{\sqrt{2}} = 70.7$$

$$\therefore \quad \text{Voltage gain in dB at } f_1 = \text{voltage gain in dB at } f_2 = 20 \log 70.7$$

$$= 37 \text{ dB}$$

Now if we assign maximum gain (40 dB) as a 0 dB then gain at f_1 and f_2 becomes − 3 dB (40 − 37), as shown in the Fig. 2.3.

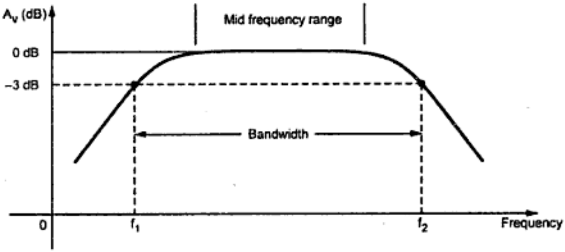


Fig. 2.3 Normalized voltage gain versus frequency curve

It shows that the voltage gain at f_1 and f_2 is less than 3 dB of the maximum voltage gain. Due to this, frequencies f_1 and f_2 are also called **3 dB frequencies.**

At f_1 and f_2 power gain drops by 3 dB (power gain dB = 10 log (0.5) = − 3 dB). For all frequencies within the bandwidth (BW = $f_2 - f_1$), amplifier power gain is at least half of the maximum power gain. Thus this bandwidth is also referred to as **3 dB bandwidth.**

2.1.3 Significance of Octaves and Decades

The octaves and decades are the measures of change in frequency. A ten times change in frequency is called a **decade.** On the other hand, an **octave** corresponds to a doubling or halving of the frequency. For example, an increase in frequency from 100 Hz to 200 Hz is an octave. Likewise, a decrease in frequency from 100 kHz to 50 kHz is also an octave.

At lower and higher frequencies the decrease in the gain of amplifiers is often indicated in terms of dB/decades or dB/octaves. If the attenuation in the gain is 20 dB for each decade, then it is indicated by line having slope of 20 dB/decade. This is illustrated in Fig. 2.4. A rate of − 20 dB/decade is approximately equivalent to − 6 dB/octave, a rate of − 40 dB/decade is approximately equivalent to − 12 dB/octave, and so on.

If the frequency is reduced to one hundredth of f_c (i.e. from f_c to 0.01 f_c), the drop in the voltage gain is − 40 dB. In each decade the voltage gain drops by − 20 dB.

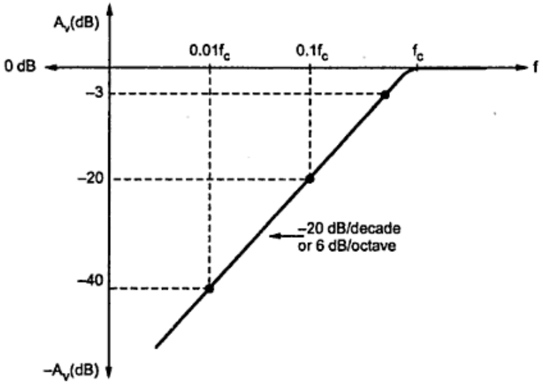


Fig. 2.4 Frequency response showing significance of decade and octave

2.1.4 Midband Gain

We define the midband of an amplifier as the band of frequencies between 10 f_1 and 0.1 f_2. As shown in the Fig. 2.3, in the midband, the voltage gain of the amplifier is approximately maximum. It is designated as midband gain or A_{mid}.

Although an amplifier normally operates in the midband, there are times when we want to know what the voltage gain is outside of the midband. The voltage gain of the amplifier outside the midband is approximately given as

$$A = \frac{A_{mid}}{\sqrt{1+(f_1/f)^2}\sqrt{1+(f/f_2)^2}}$$

In the midband, $f_1/f \approx 0$ and $f/f_2 \approx 0$. Therefore,

Midband : $A = A_{mid}$

Below the midband, $f/f_2 \approx 0$. As a result, the equation becomes

Below Midband : $$A = \frac{A_{mid}}{\sqrt{1+(f_1/f)^2}}$$

Above Midband, $f_1/f \approx 0$. As a result, the equation becomes

Above Midband : $$A = \frac{A_{mid}}{\sqrt{1+(f/f_2)^2}}$$

Example 2.2 : *For an amplifier, midband gain = 100 and lower cut-off frequency is 1 kHz. Find the gain of an amplifier at frequency = 20 Hz.*

Solution : We know that,

Below midband : $$A = \frac{A_{mid}}{\sqrt{1+(f_1/f)^2}}$$

$$\therefore \quad A = \frac{100}{\sqrt{1+\left(\frac{1000}{20}\right)^2}} = 2$$

Example 2.3 : *For an amplifier, 3-dB gain is 200 and higher cut-off frequency is 20 kHz. Find the gain of an amplifier at frequency = 100 kHz.*

Solution :

We know that $$A_{mid} = 3 \text{ dB gain} \times \sqrt{2} = 200 \times \sqrt{2} = 282.84$$

and

Above midband : $$A = \frac{A_{mid}}{\sqrt{1+(f/f_2)^2}}$$

$$\therefore \quad A = \frac{282.84}{\sqrt{1+\left(\frac{100\times 10^3}{20\times 10^3}\right)^2}} = 115.47$$

2.2 Effect of Various Capacitors on Frequency Response

2.2.1 Effect of Coupling Capacitors

Recall that the reactance of a capacitor is $X_C = 1/2\pi f_C$. At medium and high frequencies, the factor f makes X_C very small, so that all coupling capacitors behave as short circuits. At low frequencies, X_C increases. This increase in X_C drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequencies decrease, the capacitor reactances increase and circuit gain continues to fall, reducing the output voltage.

2.2.2 Effect of Bypass Capacitors

At lower frequencies, the bypass capacitor C_E is not a short. So, the emitter is not at ac ground. X_C in parallel with R_E (R_s in case of FET) creates an impedance. The signal voltage drops across this impedance reducing the circuit gain. This is illustrated in Fig. 2.5.

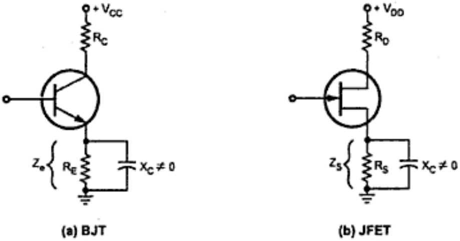


Fig. 2.5 At low frequencies emitter (source in case of JFET) is not at ac ground

2.2.3 Effect of Internal Transistor Capacitances

At high frequencies, the coupling and bypass capacitors act as short circuit and do not affect the amplifier frequency response. However, at high frequencies, the internal capacitances, commonly known as junction capacitances do come into play, reducing the circuit gain.

Fig. 2.6 shows the junction capacitances for both a BJT and a JFET. In case of the BJT, C_{be} is the base emitter junction capacitance and C_{bc} is the base collector junction capacitance. In case of JFET, C_{gs} is the internal capacitance between gate and source and C_{gd} is the internal capacitance between gate and drain.

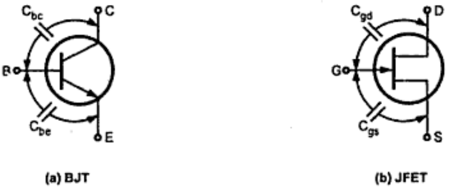


Fig. 2.6 Internal transistor capacitances

At higher frequencies, the reactances of the junction capacitances are low. As frequency increases, the reactances of junction capacitances fall. When these reactances become small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

2.2.4 Miller Theorem

For the analysis purpose, in transistor amplifiers, it is necessary to split the capacitance between input (base or gate) and the output (collector or drain). This can be achieved using Miller's theorem, as shown in the Fig. 2.7. In the Fig. A_v represents absolute voltage gain of the amplifier at midrange frequencies and C represents either C_{bc} (in case of BJT) or C_{gd} (in case of FET).

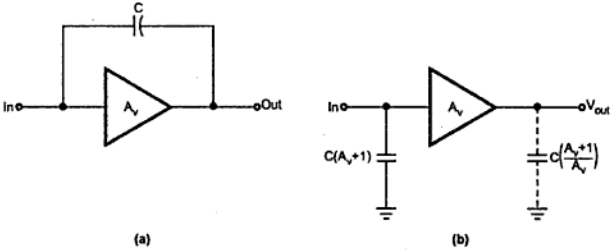


Fig. 2.7 Spliting of capacitor using Miller's theorem

2.3 Low Frequency Response of Common Emitter Amplifier

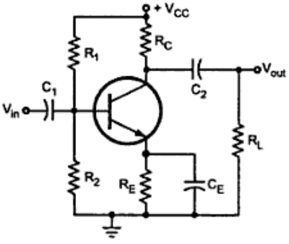


Fig. 2.8 Typical RC coupled common emitter amplifier

Let us consider a typical common emitter amplifier as shown in Fig. 2.8.

The amplifier shown in Fig. 2.9 has three RC networks that affect its gain as the frequency is reduced below midrange. These are :

1) RC network formed by the input coupling capacitor C_1 and the input impedance of the amplifier.
2) RC network formed by the output coupling capacitor C_2, the resistance looking in at the collector, and the load resistance.
3) RC network formed by the emitter bypass capacitor C_E and the resistance looking in at the emitter.

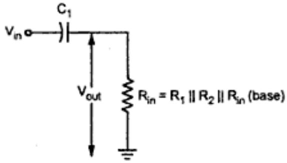


Fig. 2.9

Input RC Network

Fig. 2.9 shows input RC network formed by C_1 and the input impedance of the amplifier. Note that V_{out} shown in the Fig. 2.10 is the output voltage of the network.

Applying voltage divider theorem we can write

$$V_{out} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} \right) V_{in}$$

We know that a critical point in the amplifier response is generally accepted to occur when the output voltage is 70.7 percent of the input ($V_{out} = 0.707\ V_{in}$) . Thus we can write, at critical point

$$\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = 0.707 = \frac{1}{\sqrt{2}}$$

$\therefore$ At this condition $R_{in} = X_{C1}$.

At this condition the overall gain is reduced due to the attenuation provided by the input RC network. The reduction in overall gain is given by

$$A_v = 20 \log \left(\frac{V_{out}}{V_{in}} \right) = 20 \log (0.707) = -3 \text{ dB}$$

The frequency f_c at this condition is called lower critical frequency and is given by

$$f_c = \frac{1}{2 \pi R_{in} C_1}$$

where $R_{in} = R_1 || R_2 || h_{ie}$

$$\therefore \quad f_c = \frac{1}{2 \pi (R_1 || R_2 || h_{ie}) C_1}$$

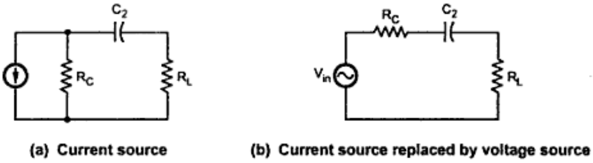
If the resistance of input source is taken into account the above equation becomes

$$f_c = \frac{1}{2 \pi (R_s + R_{in}) C_1}$$

The phase angle in an input RC circuit is expressed as $\theta = \tan^{-1} \left(\frac{X_{C1}}{R_{in}} \right)$.

Output RC Network

Fig. 2.10 shows output RC network formed by C_2, resistance looking in at the collector and the load resistance.



(a) Current source (b) Current source replaced by voltage source

Fig. 2.10

The critical frequency for this RC network is given by,

$$f_c = \frac{1}{2\pi(R_C + R_L)C_2}$$

The phase angle in the output RC circuit is expressed as $\theta = \tan^{-1}\left(\frac{X_{C2}}{R_C + R_L}\right)$.

Bypass Network

Fig. 2.11 (b) shows RC network formed by the emitter bypass capacitor C_E and the resistance looking in at the emitter.

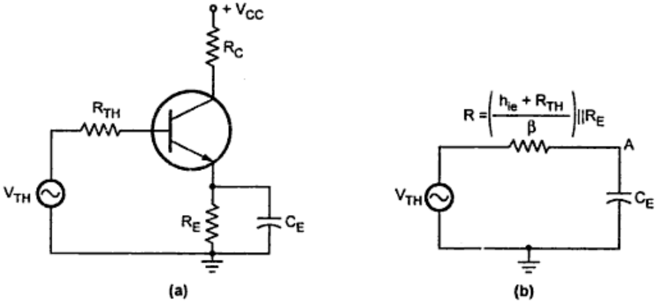


Fig. 2.11 Bypass RC network

Here, $\frac{h_{ie} + R_{TH}}{\beta}$ is the resistance looking in at the emitter. It is derived as follows

$$R = \frac{V_e}{I_e} + \frac{h_{ie}}{\beta} \cong \frac{V_b}{\beta I_b} + \frac{h_{ie}}{\beta}$$

$$= \frac{I_b R_{TH}}{\beta I_b} + \frac{h_{ie}}{\beta} = \frac{R_{TH} + h_{ie}}{\beta}$$

where $R_{TH} = R_1 || R_2 || R_s$. It is the thevenin's equivalent resistance looking from the base of the transistor towards the input as shown in the Fig. 2.11 (a).

The critical frequency for the bypass network is

$$f_c = \frac{1}{2\pi R C_E}$$

or

$$f_c = \frac{1}{2\pi\left[\left(\frac{h_{ie} + R_{TH}}{\beta}\right) || R_E\right] C_E}$$

We have seen that each network has a critical frequency. It is not necessary that all these frequencies should be equal. The network which has higher critical frequency than other two networks is called dominant network. The dominant network determines the frequency at which the overall gain of the amplifier begin to drop at –20 dB/decade. This is illustrated in the following example.

➡ **Example 2.4 :** *Determine the low frequency response of the amplifier circuit shown in Fig. 2.12.*

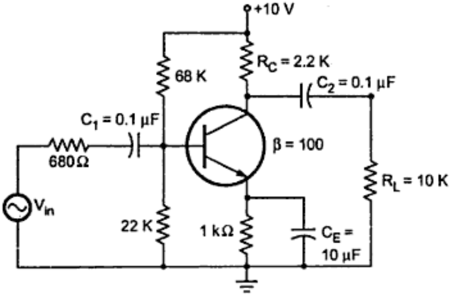


Fig. 2.12

Solution : It is necessary to analyze each network to determine the critical frequency of the amplifier

a) Input RC network

$$f_c\,(\text{input}) = \frac{1}{2\pi[R_s + (R_1 \,||\, R_2 \,||\, h_{ie})]C_1}$$

$$= \frac{1}{2\pi[680 + (68\,\text{K} \,||\, 22\,\text{K} \,||\, 1.1\,\text{K})] \times 0.1 \times 10^{-6}}$$

$$= \frac{1}{2\pi[680 + 1031.7] \times 0.1 \times 10^{-6}} = \mathbf{929.8\ Hz}$$

b) Output RC network

$$f_{c\,(\text{output})} = \frac{1}{2\pi(R_C + R_L)\,C_2} = \frac{1}{2\pi(2.2\,\text{K} + 10\,\text{K}) \times 0.1 \times 10^{-6}}$$

$$= \mathbf{130.45\ Hz}$$

c) Bypass RC network

$$f_{c\,(\text{bypass})} = \frac{1}{2\pi\left[\left(\frac{R_{TH} + h_{ie}}{\beta}\right) || R_E\right] C_E}$$

$$R_{TH} = R_1 \,||\, R_2 \,||\, R_s = 68\text{K} \,||\, 22\text{K} \,||\, 680 = 653.28\ \Omega$$

$$f_{c\,(\text{bypass})} = \frac{1}{2\pi\left[\left(\frac{653.28 + 1100}{100}\right) || 1\,\text{K}\right] \times 10 \times 10^{-6}}$$

$$= \frac{1}{2\pi(17.23) \times 10 \times 10^{-6}} = \mathbf{923.7\ Hz}$$

We have calculated all the three critical frequencies :

a) f_c (input) = 929.8 Hz b) f_c (output) = 130.45 Hz c) f_c (bypass) = 923.7 Hz

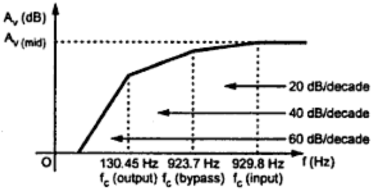


Fig. 2.13 Low frequency response of the amplifier

The above analysis shows that the input network produces the dominant lower critical frequency. Fig. 2.13 shows low frequency response of the given amplifier.

2.4 Low Frequency Response of Common Source Amplifier

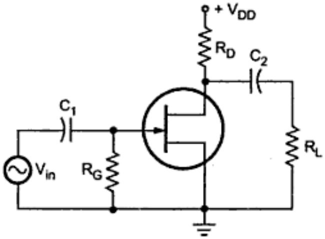


Fig. 2.14 Typical RC coupled common source amplifier

Let us consider a typical common source amplifier as shown in Fig. 2.14.

The amplifier shown in Fig. 2.14 has two RC networks that affect its gain as the frequency is reduced below midrange. These are :

1) RC network formed by the input coupling capacitor C_1 and the input impedance and
2) RC network formed by the output coupling capacitor and the output impedance looking in at the drain.

Input RC Network

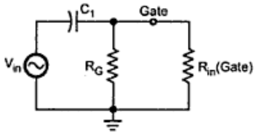


Fig. 2.15 Input RC network

Fig. 2.15 shows the input RC network formed by C_1 and the input impedance of the amplifier.

The lower critical frequency of this network can be given as

$$f_c = \frac{1}{2\pi R_{in} C_1}$$

where $R_{in} = R_G \parallel R_{in\,(gate)}$

The value of $R_{in\,(gate)}$ can be determined from the data sheet as follows :

$$R_{in\,(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

where I_{GSS} is the gate reverse current.

The phase shift in the low frequency input RC circuit is $\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)$.

Output RC Network

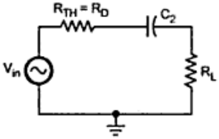


Fig. 2.16 Output RC network

Fig. 2.16 shows the output RC network formed by C_2 and the output impedance looking in at the drain.

The lower critical frequency for this network can be given as

$$f_c = \frac{1}{2\pi(R_D + R_L) C_2}$$

The FET amplifier circuit shown in Fig. 2.14 has two critical frequencies for two networks, and network having higher critical frequency is called **dominant network.**

The phase shift in low frequency output RC circuit is $\theta = \tan^{-1}\left(\frac{X_{C2}}{R_D + R_L}\right)$.

➡ **Example 2.5 :** *Determine the low frequency response of the amplifier circuit shown in Fig. 2.17.*

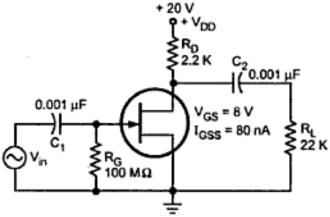


Fig. 2.17

Solution : It is necessary to analyze each network to determine the critical frequency of the amplifier

a) Input RC Network

$$f_c = \frac{1}{2\pi R_{in}\, C_1}$$

where $$R_{in} = R_G \,||\, R_{in\,(gate)} = R_G \,||\left|\frac{V_{GS}}{I_{GSS}}\right|$$

$$= 100\ \text{M}\Omega \,||\, \frac{8}{80 \times 10^{-9}} = 100\ \text{M}\Omega\ ||\ 100\ \text{M}\Omega = \mathbf{50\ M\Omega}$$

$$\therefore \quad f_c = \frac{1}{2\pi \times 50 \times 10^6 \times 0.001 \times 10^{-6}} = \mathbf{3.18\ Hz}$$

b) Output RC Network

$$f_c = \frac{1}{2\pi(R_D + R_L)C_2} = \frac{1}{2\pi(2.2\,\text{K} + 22\,\text{K})\,1 \times 10^{-6}} = \mathbf{6.577\ Hz}$$

We have calculated two critical frequencies

a) f_c (input) = 3.18 Hz

b) f_c (output) = 6.577 Hz

The above analysis shows that the output network produces dominant lower critical frequency. Fig. 2.18 shows the frequency response of the given amplifier.

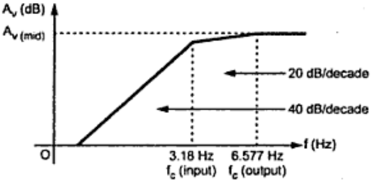


Fig. 2.18 Low frequency response of the FET amplifier

2.5 High Frequency Response of Common Emitter Amplifier

Let us consider a typical common emitter amplifier as shown in Fig. 2.19.

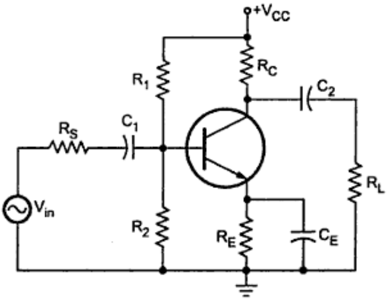


Fig. 2.19 Typical RC coupled common emitter amplifier

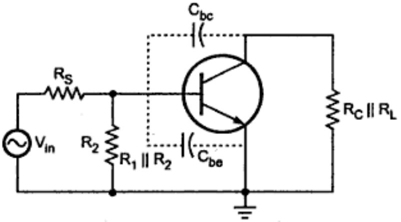


Fig. 2.20 High frequency equivalent circuit

As mentioned earlier, at high frequencies, the coupling and bypass capacitors act as a short circuit and do not affect the amplifier frequency response. However, at higher frequencies the internal capacitances do come into play. Fig. 2.20 shows the high frequency equivalent circuit for the given amplifier circuit.

Using Miller theorem this high frequency equivalent circuit can be further simplified as follows.

The internal capacitance C_{bc} can be splitted into $C_{in\,(miller)}$ and $C_{out\,(miller)}$ as shown in the Fig. 2.21.

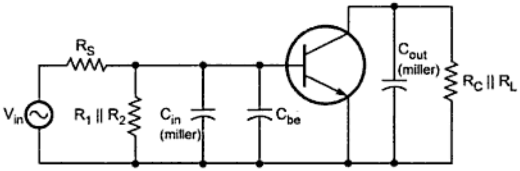


Fig. 2.21 Simplified high frequency equivalent circuit

where $$C_{in\,(miller)} = C_{bc}\,(A_v + 1)$$

and $$C_{out\,(miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right) \approx C_{bc}$$

Fig. 2.21 shows that there are two RC networks which affect the high frequency response of the amplifier. These are :

1) Input RC Network and

2) Output RC Network

Input RC Network

Fig. 2.22 shows input RC network.

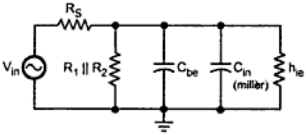


Fig. 2.22 Input RC network

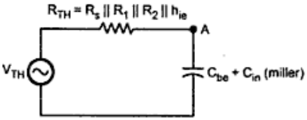

$R_{TH} = R_s \| R_1 \| R_2 \| h_{ie}$
A
V_{TH}
$C_{be} + C_{in}$ (miller)

Fig. 2.23 Reduces input RC network

This network is further reduced as shown in the Fig. 2.23. At high frequencies capacitive reactance becomes smaller. If we apply voltage divider theorem, voltage at point A in Fig. 2.23 reduces as capacitive reactance reduces with increase in frequency above midrange. This reduces the signal voltage applied to the base, reducing the circuit gain and hence the output voltage.

The critical frequency can be calculated at condition capacitive reactance is equal to the resistance, i.e. $X_{C1} = R_s \| R_1 \| R_2 \| h_{ie}$.

It is given as,

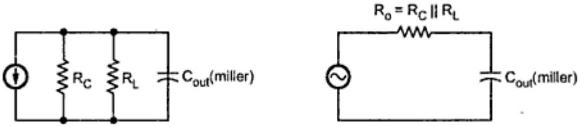
$$f_c\,(\text{input}) = \frac{1}{2\pi(R_s \parallel R_1 \parallel R_2 \parallel h_{ie})\,C_T}$$

where $C_T = C_{bc} + C_{in\,(\text{Miller})}$

The phase shift in high frequency input RC circuit is $\theta = \tan^{-1}\left(\frac{R_s \parallel R_1 \parallel R_2 \parallel h_{ie}}{X_{C_T}}\right)$

Output RC Network

Fig. 2.24 shows the output RC network.



R_C
R_L
C_{out}(miller)
$R_o = R_C \parallel R_L$
C_{out}(miller)

(a) Output network with current source **(b) Output network with voltage source**

Fig. 2.24

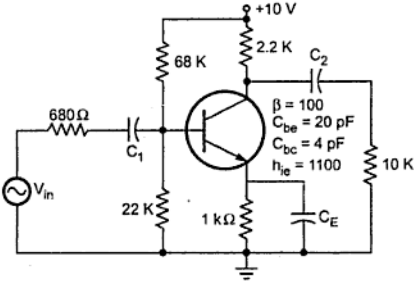
The critical frequency can be given as

$$f_c\,(\text{output}) = \frac{1}{2\pi R_o\, C_{out\,(\text{miller})}} \approx \frac{1}{2\pi(R_C \parallel R_L)\,C_{bc}}$$

We have seen that both the networks have critical frequencies. It is not necessary that these frequencies should be equal. The network which has lower critical frequency than other network is called **dominant network.**

The phase shift in high frequency output RC network is $\theta = \tan^{-1}\left(\frac{R_o}{X_{C\,out\,(\text{Miller})}}\right)$.

Example 2.6 *Determine the high frequency response of the amplifier circuit shown in Fig. 2.25.*



+10 V
68 K
2.2 K
C_2
680 Ω
C_1
β = 100
C_{be} = 20 pF
C_{bc} = 4 pF
h_{ie} = 1100
10 K
V_{in}
22 K
1 kΩ
C_E

Fig. 2.25

Solution : Before calculating critical frequencies it is necessary to calculate mid frequency gain of the given amplifier circuit. This is required to calculate $C_{in\ (miller)}$ and $C_{out\ (miller)}$.

$$A_v = \frac{-h_{fe} R_o}{R_i}$$

where $$R_i = h_{ie} \| R_1 \| R_2$$

and $$R_o = R_C \| R_L$$

$$\therefore \quad A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} \| R_1 \| R_2} = \frac{-100\,(2.2\text{ K} \| 10\text{ K})}{1100 \| 68\text{ K} \| 22\text{ K}}$$

$$= \frac{-100\,(1.8\text{ K})}{1.032\text{ K}} = -174.4$$

Negative sign indicates 180° phase shift between input and output.

$$C_{in\ (miller)} = C_{bc}\,(A_v + 1) = 4\text{ pF}\,(174.4 + 1) = 0.7016\text{ nF}$$

$$C_{out\ (miller)} = \frac{C_{bc}\,(A_v + 1)}{(A_v)} = \frac{4\text{ pF}(174.4+1)}{(174.4)} = 4\text{ pF}$$

We now analyze input and output network for critical frequency.

$$f_c\text{ (input)} = \frac{1}{2\pi(R_s \| R_1 \| R_2 \| h_{ie})(C_{bc} + C_{in\ (miller)})}$$

$$= \frac{1}{2\pi(680 \| 68\text{ K}) \| 22\text{ K} \| 1100)(20\text{ pF} + 0.7016\text{ nF})}$$

$$= \frac{1}{2\pi(410)(0.7216 \times 10^{-9})} = 537947\text{ Hz} = \mathbf{537.947\ kHz}$$

$$f_c\text{ (output)} = \frac{1}{2\pi(R_C \| R_L)\,C_{out\ (miller)}} = \frac{1}{2\pi(2.2\text{ K} \| 10\text{ K}) \times 4\text{ pF}}$$

$$= \mathbf{22.1\ MHz}$$

We have calculated both the critical frequencies :

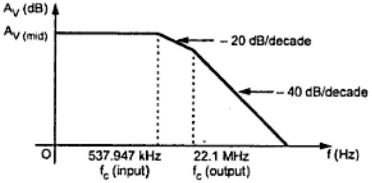


Fig. 2.26 High frequency response of the amplifier

a) f_c (input) = **537.947 kHz**

b) f_c (output) = **22.1 MHz**

The above analysis shows that the input network produces the dominant higher critical frequency. Fig. 2.26 shows high frequency response of the given amplifier.

2.6 High Frequency Response of Common Source Amplifier

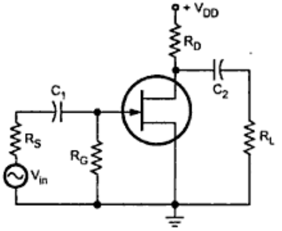


Fig. 2.27 Typical RC coupled common source amplifier

Let us consider a typical common source amplifier as shown in Fig. 2.27.

Fig. 2.28 shows the high frequency equivalent circuit for the given amplifier circuit. It shows that at high frequencies coupling and bypass capacitors act as short circuits and do not affect the amplifier high frequency response. The equivalent circuit shows internal capacitances which affect the high frequency response.

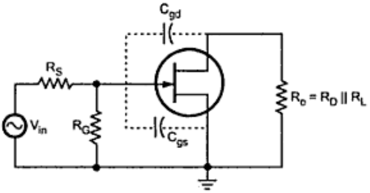


Fig. 2.28 High frequency equivalent circuit

Using Miller theorem this high frequency equivalent circuit can be further simplified as follows :

The internal capacitance C_{gd} can be splitted into $C_{in\ (miller)}$ and $C_{out\ (miller)}$ as shown in the Fig. 2.29.

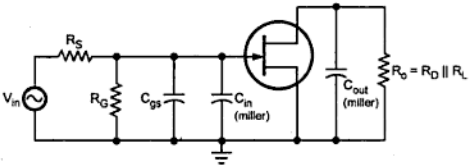


Fig. 2.29 Simplified high frequency equivalent circuit

where
$$C_{in\,(miller)} = C_{gd}\,(A_v + 1)$$
$$C_{out\,(miller)} = C_{gd}\,\frac{(A_v + 1)}{(A_v)}$$

FET data sheets do not directly provide values for C_{gs} and C_{gd} . The data sheet normally provides values for input capacitance, C_{iss} and the reverse transfer capacitance C_{rss}. From C_{iss} and C_{rss} the values for C_{gd} and C_{gs} can be calculated as follows :

$$C_{gd} = C_{rss}$$
$$C_{gs} = C_{iss} - C_{rss}$$

Fig. 2.29 shows that there are two RC networks which affect the high frequency response of the amplifier. These are :

1) Input RC network and

2) Output RC network

Input RC Network

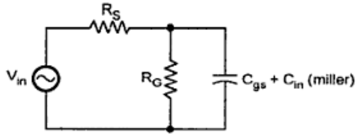


Fig. 2.30 Input RC network

Fig. 2.30 shows input RC network.

This network is further reduced as shown in the Fig. 2.31, since $R_s << R_G$.

The critical frequency for the reduced input RC network is given as

$$f_{c\,(input)} = \frac{1}{2\pi R_s C_T}$$

$$\text{or } f_c = \frac{1}{2\pi R_s\ [C_{gs} + C_{in\,(miller)}]}$$

The phase shift in high frequency input RC network is $\theta = \tan^{-1}\left(\frac{R_s}{X_{C_T}}\right)$.

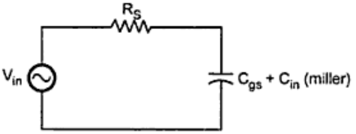
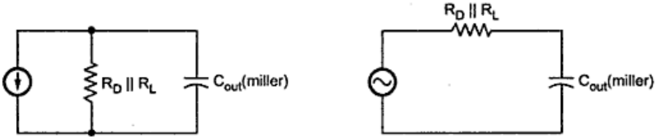


Fig. 2.31 Reduced input RC network

Output RC Network

Fig. 2.32 shows output RC network.



$R_D \| R_L$
C_{out}(miller)
$R_D \| R_L$
C_{out}(miller)

(a) Output network with current source **(b) Output network with voltage source**

Fig. 2.32

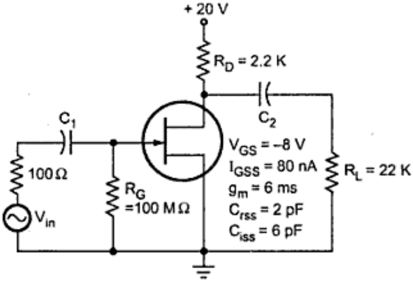
The critical frequency for the above circuit is given as

$$f_c = \frac{1}{2\pi R_o \, C_{out\,(miller)}} = \frac{1}{2\pi(R_D \,\|\, R_L)\, C_{out\,(miller)}}$$

We have seen that both the networks have critical frequencies. It is not necessary that these frequencies should be equal. The network which has lower critical frequency than other network is called dominant network.

The phase shift in high frequency output RC network is $\theta = \tan^{-1}\left(\frac{R_o}{X_{C\,out\,(Miller)}}\right)$.

➠ **Example 2.7 :** *Determine the high frequency response of the amplifier circuit shown in Fig. 2.33.*



+ 20 V
R_D = 2.2 K
C_1
C_2
100 Ω
V_{in}
R_G =100 MΩ
V_{GS} = –8 V
I_{GSS} = 80 nA
g_m = 6 ms
C_{rss} = 2 pF
C_{iss} = 6 pF
R_L = 22 K

Fig. 2.33

Solution : Before calculating critical frequencies it is necessary to calculate mid frequency gain of the given amplifier circuit. This is required to calculate $C_{in\,(miller)}$ and $C_{out\,(miller)}$.

$$A_v = -g_m R_D$$

Here, R_D should be replaced by $R_D \| R_L$.

$$\therefore \quad A_v = -g_m (R_D \| R_L) = -6\text{ mS}(2.2\text{ K} \| 22\text{ K})$$

$$= -6\text{ mS }(2\text{ K}) = -12$$

$$C_{in\,(miller)} = C_{gd}(A_v + 1) = C_{rss}(A_v + 1) = 2\text{ pF }(12 + 1) = 26\text{ pF}$$

$$C_{out\,(miller)} = \frac{C_{gd}(A_v + 1)}{(A_v)} = \frac{C_{rss}(A_v + 1)}{(A_v)} = \frac{2\text{ pF}(12+1)}{12}$$

$$= 2.166\text{ pF}$$

$$C_{gs} = C_{iss} - C_{rss} = 4\text{ pF}$$

We now analyze input and output network for critical frequency

$$f_{c\,(input)} = \frac{1}{2\pi R_s C_T}$$

$$= \frac{1}{2\pi R_s \times [C_{gs} + C_{in\,(miller)}]}$$

$$= \frac{1}{2\pi \times 100 \times [4\text{ pF} + 26\text{ pF}]}$$

$$= \frac{1}{2\pi \times 100 \times [30\text{ pF}]} = 53\text{ MHz}$$

$$f_c\text{ (output)} = \frac{1}{2\pi(R_D \| R_L) \times C_{out\,(miller)}} = \frac{1}{2\pi(2.2\text{ K} \| 22\text{ K}) \times 2.166\text{ pF}}$$

$$= 36.74\text{ MHz}$$

We have calculated both the critical frequencies :

a) f_c (input) = 53 MHz b) f_c (output) = 36.74 MHz.

The above analysis shows that the output network produces the dominant higher critical frequency. High frequency response of the given amplifier is shown in Fig. 2.34.

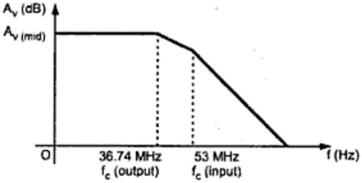


Fig. 2.34 High frequency response of the amplifier

Review Questions

1. *What do you understand by frequency response of the amplifier ? How is it plotted ?*
2. *What do you mean by bandwidth of the amplifier ?*
3. *Explain the usefulness of decibel unit.*
4. *Explain the significance of octaves and decades.*
5. *Give the expressions for voltage gain of the amplifier below and above midband.*
6. *What is the effect of coupling capacitors on the bandwidth of the amplifier?*
7. *What is the effect of bypass capacitors on the bandwidth of the amplifier?*
8. *What is the effect of internal transistor capacitances on the bandwidth of the amplifier ?*
9. *For the circuit shown in Fig. 2.35 determine the low frequency response.*

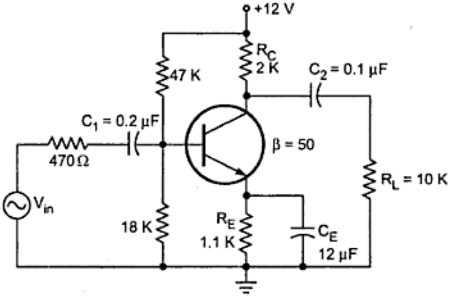

+12 V
47 K
R_C
2 K
$C_2 = 0.1\ \mu F$
$C_1 = 0.2\ \mu F$
470Ω
$\beta = 50$
$R_L = 10$ K
V_{in}
18 K
R_E
1.1 K
C_E
12 μF

Fig. 2.35

10. *Determine the low frequency response of the amplifier circuit shown in Fig. 2.36.*

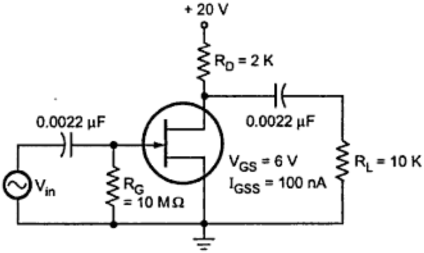
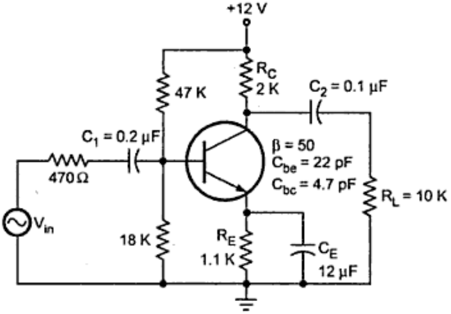

+ 20 V
$R_D = 2$ K
0.0022 μF
0.0022 μF
$V_{GS} = 6$ V
$I_{GSS} = 100$ nA
$R_L = 10$ K
V_{in}
R_G
= 10 MΩ

Fig. 2.36

11. Draw the high frequency equivalent circuit for the typical RC coupled commom emitter amplifier.

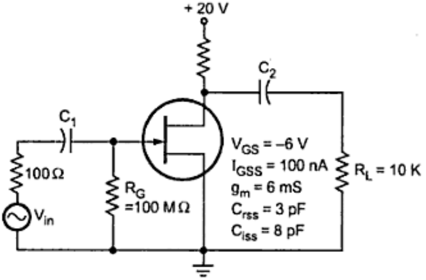
12. Determine the high frequency response of the amplifier circuit shown in Fig. 2.37.



+12 V
R_C
2 K
47 K
C_2 = 0.1 μF
C_1 = 0.2 μF
470 Ω
β = 50
C_be = 22 pF
C_bc = 4.7 pF
R_L = 10 K
V_in
18 K
R_E
1.1 K
C_E
12 μF

Fig. 2.37

13. Determine the high frequency response of the amplifier circuit shown in Fig. 2.38.



+ 20 V
C_2
C_1
100 Ω
V_in
R_G
=100 MΩ
V_GS = –6 V
I_GSS = 100 nA
g_m = 6 mS
C_rss = 3 pF
C_iss = 8 pF
R_L = 10 K

Fig. 2.38

14. Why the gain of the amplifier decreases in the low frequency and high frequency range ?

❑❑❑

3

Feedback Amplifiers

3.1 Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are in out of phase, the feedback is called **negative feedback**. Use of positive feedback results in oscillations and hence not used in amplifiers.

In this chapter, we introduce the concept of feedback and show how to modify the characteristics of an amplifier by combining a portion or part of the output signal with the input signal.

3.2 Classification of Amplifiers

Before proceeding with the concepts of feedback, it is useful to understand the classification of amplifiers based on the magnitudes of the input and output impedances of an amplifier relative to the source and load impedances, respectively. The amplifiers can be classified into four broad categories : voltage, current, transconductance and transresistance amplifiers.

3.2.1 Voltage Amplifier

Fig. 3.1 shows a Thevenin's equivalent circuit of an amplifier.

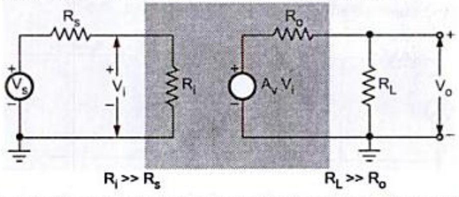


Fig. 3.1 Thevenin's equivalent circuits of a voltage amplifier

If the amplifier input resistance R_i is large compared with the source resistance R_s then $V_i \approx V_s$. If the external load resistance R_L is large compared with the output resistance R_o of the amplifier, then $V_o \approx A_v V_i \approx A_v V_s$. Such amplifier circuit provides a voltage output proportional to the voltage input and the proportionality factor does not depend on the magnitudes of the source and load resistances. Hence, this amplifier is called **voltage amplifier**. An ideal voltage amplifier must have infinite input resistance R_i and zero output resistance R_o. For practical voltage amplifier we must have $R_i >> R_s$ and $R_L >> R_o$.

3.2.2 Current Amplifier

Fig. 3.2 shows Norton's equivalent circuit of a current amplifier. If amplifier input resistance $R_i \rightarrow 0$, then $I_i \approx I_s$. If amplifier output resistance $R_o \rightarrow \infty$, then $I_L = A_i I_i$. Such amplifier provides a current output proportional to the signal current and the proportionality factor is independent of source and load resistances. This amplifier is called **current amplifier**. An ideal current amplifier must have zero input resistance R_i and infinite output resistance R_o. For practical current amplifier we must have $R_i << R_s$ and $R_o >> R_L$.

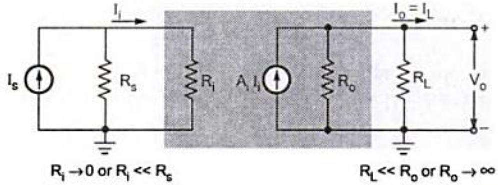

I_i
$I_o = I_L$
I_s
R_s
R_i
$A_i I_i$
R_o
R_L
V_o
+
−
$R_i \rightarrow 0$ or $R_i << R_s$
$R_L << R_o$ or $R_o \rightarrow \infty$

Fig. 3.2 Norton's equivalent circuits of a current amplifier

3.2.3 Transconductance Amplifier

Fig. 3.3 shows a transconductance amplifier with a Thevenin's equivalent in its input circuit and Norton's equivalent in its output circuit. In this amplifier, an output current is proportional to the input signal voltage and the proportionality factor is independent of the magnitudes of the source and load resistances. Ideally, this amplifier must have an infinite input resistance R_i and infinite output resistance R_o. For practical transconductance amplifier we must have $R_i >> R_s$ and $R_o >> R_L$.

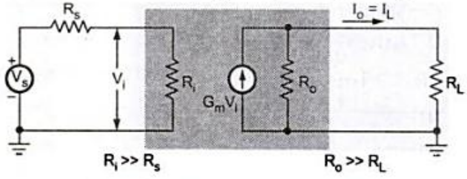


Fig. 3.3 Transconductance amplifier

3.2.4 Transresistance Amplifier

Fig. 3.4 shows a transresistance amplifier with a Norton's equivalent in its input circuit and a Thevenin's equivalent in its output circuit. In this amplifier an output voltage is proportional to the input signal current and the proportionality factor is independent on the source and load resistances. Ideally, this amplifier must have zero input resistance R_i and zero output resistance R_o. For practical transresistance amplifier we must have $R_i << R_s$ and $R_o << R_L$.

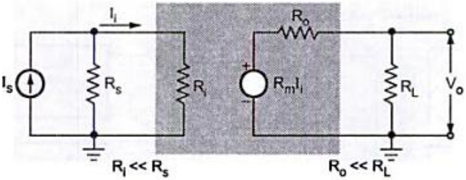

I_i
R_o
I_s
R_s
R_i
$R_m I_i$
R_L
V_o
$R_i << R_s$
$R_o << R_L$

Fig. 3.4

3.3 Feedback Concept

In the previous section we have seen four basic amplifier types and their ideal characteristics. In each one of these circuits we can sample the output voltage or current by means of a suitable sampling network and apply this signal to the input through a feedback two port network, as shown in the Fig. 3.5. At the input the feedback signal is combined with the input signal through a mixer network and is fed into the amplifier.

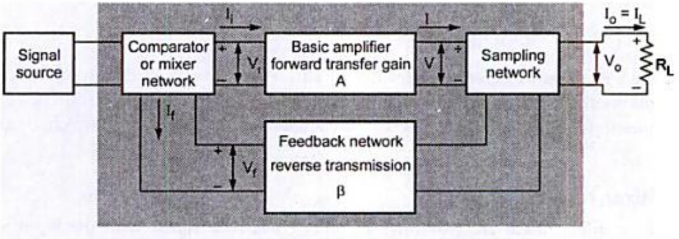

Signal source
Comparator or mixer network
I_i
V_i
Basic amplifier forward transfer gain A
I
V
Sampling network
$I_o = I_L$
V_o
R_L
I_f
V_f
Feedback network reverse transmission β

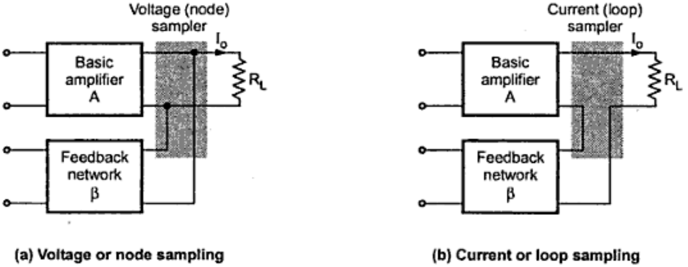
Fig. 3.5 Typical feedback connection around a basic amplifier

As shown in the Fig. 3.5 feedback connection has three networks :

- Sampling Network
- Feedback Network
- Mixer Network

3.3.1 Sampling Network

There are two ways to sample the output, according to the sampling parameter, either voltage or current. The output voltage is sampled by connecting the feedback network in shunt across the output, as shown in the Fig. 3.6 (a). This type of connection is referred to as **voltage or node sampling**. The output current is sampled by connecting the feedback network in series with the output as shown in the Fig. 3.6 (b). This type of connection is referred to as **current or loop sampling**.



(a) Voltage or node sampling (b) Current or loop sampling

Fig. 3.6

3.3.2 Feedback Network

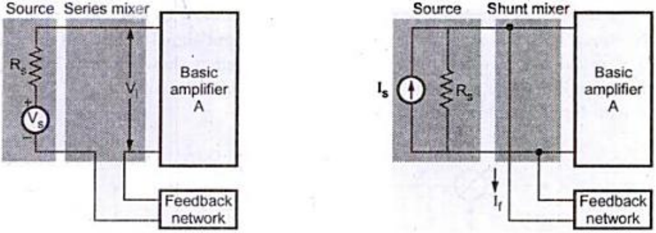
It may consists of resistors, capacitors and inductors. Most often it is simply a resistive configuration. It provides reduced portion of the output as feedback signal to the input mixer network. It is given as,

$$V_f = \beta V_o$$

where β is a **feedback factor** or **feedback ratio.** The symbol β used in feedback circuits represents feedback factor which always lies between 0 and 1. It is totally different from β symbol used to represent current gain in common emitter amplifier, which is greater than 1.

3.3.3 Mixer Network

Like sampling, there are two ways of mixing feedback signal with the input signal. These are : series input connection and shunt input connection. The Fig. 3.7 (a) and (b) show the simple and very common **series (loop)** input and **shunt (node)** input connections, respectively.


Source
Series mixer
R_s
V_s
V_i
Basic amplifier A
Feedback network
Source
Shunt mixer
I_s
R_s
I_f
Basic amplifier A
Feedback network

(a) Series mixing **(b) Shunt mixing**

Fig. 3.7

3.3.4 Transfer Ratio or Gain

In Fig. 3.5, the ratio of the output signal to the input signal of the basic amplifier is represented by the symbol A. The suffix of A given next, represents the different transfer ratios.

$$\frac{V}{V_i} = A_V = \text{Voltage gain} \quad \text{... (1)}$$

$$\frac{I}{I_I} = A_I = \text{Current gain} \quad \text{... (2)}$$

$$\frac{I}{V_I} = G_M = \text{Transconductance} \quad \text{... (3)}$$

$$\frac{V}{I_i} = R_M = \text{Transresistance} \quad \text{... (4)}$$

The four quantities A_V, A_I, G_M and R_M are referred to as a transfer gain of the basic amplifier without feedback and use of only symbol A represent any one of these quantities.

The transfer gain with feedback is represented by the symbol A_f. It is defined as the ratio of the output signal to the input signal of the amplifier configuration shown in Fig. 3.5. Hence A_f is used to represent any one of the following four ratios :

$$\frac{V_o}{V_s} = A_{Vf} = \text{Voltage gain with feedback} \quad \text{... (5)}$$

$$\frac{I_o}{I_s} = A_{If} = \text{Current gain with feedback} \quad \text{... (6)}$$

$$\frac{I_o}{V_s} = G_{Mf} = \text{Transconductance with feedback} \quad \text{... (7)}$$

$$\frac{V_o}{I_s} = R_{Mf} = \text{Transresistance with feedback} \quad \text{....(8)}$$

Fig. 3.8 shows the schematic representation of a feedback connection around a basic amplifier. Recall that, when part of output signal and input signal are in out of phase the feedback is called **negative feedback**. The schematic diagram shown in Fig. 3.8 represents negative feedback because the feedback signal is fed back to the input of the amplifier out of phase with input signal of the amplifier.

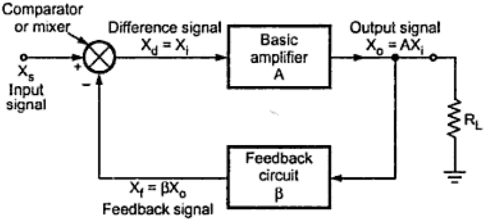

Comparator or mixer
Difference signal
$X_d = X_i$
Basic amplifier A
Output signal
$X_o = AX_i$
X_s
Input signal
+
−
R_L
Feedback circuit β
$X_f = \beta X_o$
Feedback signal

Fig. 3.8 Schematic representation of negative feedback amplifier

3.4 Ways of Introducing Negative Feedback in Amplifiers

The basic amplifier shown in Fig. 3.8 may be a voltage, current, transconductance, or transresistance amplifier. These can be connected in a feedback configuration as shown in the Fig. 3.9.

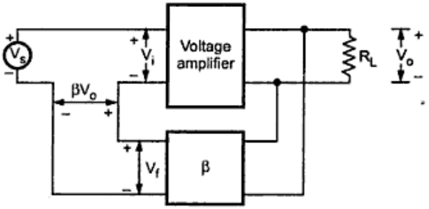

V_s
+
−
V_i
Voltage amplifier
R_L
V_o
βV_o
V_f
β

Fig. 3.9 (a) Voltage amplifier with voltage series feedback

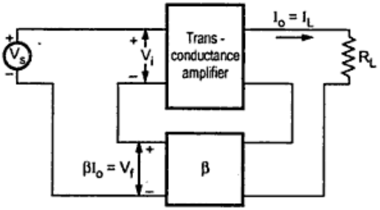

V_s
V_i
Trans - conductance amplifier
$I_o = I_L$
R_L
$\beta I_o = V_f$
β

Fig. 3.9 (b) Transconductance amplifier with current series feedback

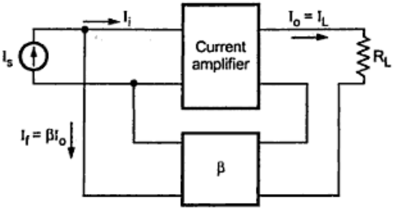

I_i
$I_o = I_L$
I_s
Current amplifier
R_L
$I_f = \beta I_o$
β

Fig. 3.9 (c) Current amplifier with current shunt feedback

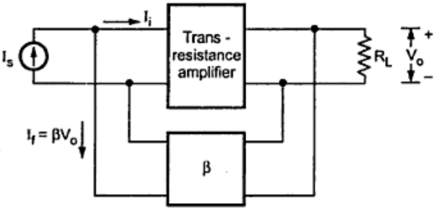

I_i
I_s
Trans - resistance amplifier
R_L
+
V_o
–
$I_f = \beta V_o$
β

Fig. 3.9 (d) Transresistance amplifier with voltage shunt feedback

3.5 Effect of Negative Feedback

3.5.1 Transfer Gain

We have seen, the symbol A is used to represent transfer gain of the basic amplifier without feedback and symbol A_f is used to represent transfer gain of the basic amplifier with feedback. These are given as,

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

where X_o = Output voltage or output current

X_i = Input voltage or input current

X_s = Source voltage or source current

As it is a negative feedback the relation between X_i and X_s is given as,

$$X_i = X_s + (-X_f)$$

where X_f = Feedback voltage or feedback current

$$\therefore \quad A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

Dividing by X_i to numerator and denominator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f)/X_i}$$

$$= \frac{A}{1 + X_f / X_i} \qquad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \qquad A_f = \frac{A}{1+\beta A} \qquad \because \quad \beta = \frac{X_f}{X_o} \qquad \dots (1)$$

where β is a feedback factor.

Looking at equation we can say that gain without feedback (A) is always greater than gain with feedback (A/(1 + βA)) and it decreases with increase in β i.e. increase in feedback factor.

For voltage amplifier, gain with negative feedback is given as,

$$A_{Vf} = \frac{A_V}{1 + A_V \beta} \qquad \dots (2)$$

where A_V = Open loop gain i.e. gain without feedback

β = Feedback factor

3.5.2 Stability of Gain

The transfer gain of the amplifier is not constant as it depends on the factors such as operating point, temperature etc. This lack of stability in amplifiers can be reduced by introducing negative feedback.

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Differentiating both sides with respect to A we get,

$$\frac{dA_f}{dA} = \frac{(1+\beta A)1 - \beta A}{(1+\beta A)^2}$$

$$= \frac{1}{(1+\beta A)^2}$$

$$\therefore \qquad dA_f = \frac{dA}{(1+\beta A)^2}$$

Dividing both sides by A_f we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+\beta A)^2} \times \frac{1}{A_f}$$

$$= \frac{dA}{(1+\beta A)^2} \times \frac{(1+\beta A)}{A_f} \qquad \text{since } A_f = \frac{A}{1+\beta A}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A}\frac{1}{(1+\beta A)} \qquad \text{... (3)}$$

where

$\frac{dA_f}{A_f}$ = Fractional change in amplification with feedback

$\frac{dA}{A}$ = Fractional change in amplification without feedback

Looking at equation (3) we can say that change in the gain with feedback is less than the change in gain without feedback by factor $(1+\beta A)$. The fractional change in amplification with feedback divided by the fractional change without feedback is called the **sensitivity of the transfer gain** $(1/(1+\beta A)$. The reciprocal of the sensitivity is called the **desensitivity D** $(1+\beta A)$.

Therefore, stability of the amplifier increases with increase in desensitivity.

If $\beta A >> 1$, then

$$A_f = \frac{A}{1+\beta A} = \frac{A}{\beta A}$$

$$= \frac{1}{\beta} \qquad \text{... (4)}$$

and the gain is dependant only on the feedback network.

Since A represents either A_V, G_M, A_I or R_M and A_f represents the corresponding transfer gains with feedback either A_{Vf}, G_{Mf}, A_{If} or R_{Mf} the equation signifies that :

- For voltage series feedback

$$A_{Vf} = \frac{1}{\beta} \qquad \text{Voltage gain is stabilized.} \qquad \text{... (5)}$$

- For current series feedback

$$G_{Mf} = \frac{1}{\beta} \qquad \text{Transconductance gain is stabilized.} \qquad \text{... (6)}$$

- For voltage shunt feedback

$$R_{Mf} = \frac{1}{\beta} \qquad \text{Transresistance gain is stabilized.} \qquad \text{... (7)}$$

- For current shunt feedback

$$A_{If} = \frac{1}{\beta} \quad \text{Current gain is stabilized.} \qquad \dots (8)$$

3.5.3 Frequency Response and Bandwidth

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Using this equation we can write,

$$A_{f\,mid} = \frac{A_{mid}}{1+\beta A_{mid}} \qquad \dots (9)$$

$$A_{f\,low} = \frac{A_{low}}{1+\beta A_{low}} \qquad \dots (10)$$

and

$$A_{f\,high} = \frac{A_{high}}{1+\beta A_{high}} \qquad \dots (11)$$

Now we analyze the effect of negative feedback on lower cut-off and upper cut-off frequency of the amplifier.

Lower cut-off frequency

We know that, the relation between gain at low frequency and gain at mid frequency, is given as,

$$\frac{A_{low}}{A_{mid}} = \frac{1}{1-j\left(\frac{f_L}{f}\right)} \quad \therefore \; A_{low} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)} \qquad \dots (12)$$

Substituting value of A_{low} in equation (10) we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}\right)} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)+A_{mid}\,\beta}$$

$$= \frac{A_{mid}}{(1+A_{mid}\beta)-j\left(\frac{f_L}{f}\right)}$$

Dividing numerator and denominator by $(1+A_{mid}\,\beta)$ we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1+A_{mid}\beta}}{1-j\left[\dfrac{\dfrac{f_L}{1+A_{mid}\beta}}{f}\right]}$$

$$= \frac{A_{f\,mid}}{1-j\left[\left(\dfrac{\dfrac{f_L}{1+A_{mid}\,\beta}}{f}\right)\right]} \qquad \because\ A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\,\beta}$$

$$\therefore \qquad \frac{A_{f\,low}}{A_{f\,mid}} = \frac{1}{1-j\left(\dfrac{f_{Lf}}{f}\right)} \qquad \text{...(13)}$$

where

Lower cut-off frequency with feedback = $f_{Lf} = \dfrac{f_L}{1+A_{mid}\,\beta}$. ... (14)

From equation (14), we can say that lower cut-off frequency with feedback is less than lower cut-off frequency without feedback by factor $(1+A_{mid}\,\beta)$. Therefore, by introducing negative feedback low frequency response of the amplifier is improved.

Upper Cut-off Frequency

We know that, the relation between gain at high frequency and gain at mid frequency is given as,

$$\frac{A_{high}}{A_{mid}} = \frac{1}{1-j\left(\dfrac{f}{f_H}\right)}$$

$$\therefore \qquad A_{high} = \frac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)} \qquad \text{... (15)}$$

Substituting value of A_{high} in equation (11) we get,

$$A_{f\,high} = \frac{\dfrac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)}\right)} = \frac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)+A_{mid}\beta}$$

Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\ high} = \frac{\dfrac{A_{mid}}{1+A_{mid}\,\beta}}{1 - j\left[\dfrac{f}{(1+A_{mid}\beta)\, f_H}\right]}$$

$$A_{f\ high} = \frac{A_{f\ mid}}{1 - j\left[\dfrac{f}{(1+A_{mid}\beta)\, f_H}\right]} \qquad \because\ A_{f\ mid} = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$= \frac{A_{f\ mid}}{1 - j\left(\dfrac{f}{f_{Hf}}\right)}$$

where upper cut-off frequency with feedback is given as,

$$f_{Hf} = (1 + A_{mid}\,\beta)\, f_H \qquad \text{... (16)}$$

From equation (16), we can say that upper cut-off frequency with feedback is greater than upper cut-off frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by introducing negative feedback high frequency response of the amplifier is improved.

Bandwidth

The bandwidth of the amplifier is given as,

$$BW = \text{Upper cut-off frequency} - \text{Lower cut-off frequency}$$

∴ Bandwidth of the amplifier with feedback is given as,

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\,\beta)\, f_H - \frac{f_L}{(1 + A_{mid}\,\beta)} \qquad \text{... (17)}$$

It is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 3.10.

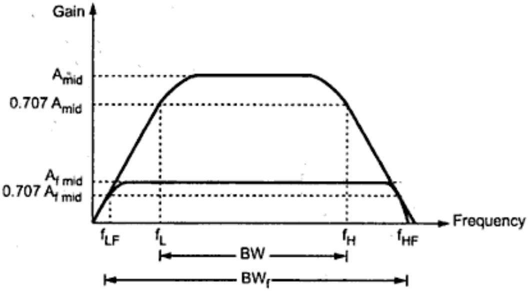


Fig. 3.10 Effect of negative feedback on gain and bandwidth

3.5.4 Frequency Distortion

From equation (8) we can say that if the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under such conditions frequency and phase distortion is substantially reduced.

If β is made up of reactive components, the reactances of these components will change with frequency, changing the β. As a result, gain will also change with frequency. This fact is used in tuned amplifiers. In tuned amplifiers, feedback network is designed such that at tuned frequency $\beta \to 0$ and at other frequencies $\beta \to \infty$. As a result, amplifier provides high gain for signal at tuned frequency and relatively reject all other frequencies.

3.5.5 Noise and Nonlinear Distortion

Signal feedback reduces the amount of noise signal and nonlinear distortion. The factor $(1+\beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. Thus, noise and nonlinear distortion also reduced by same factor as the gain.

3.5.6 Input and Output Resistances

Input resistance

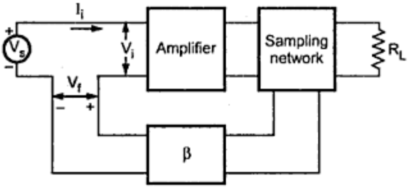


Fig. 3.11

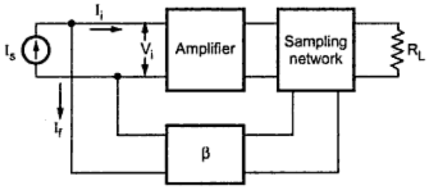


Fig. 3.12

If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), it increases the input resistance. Since the feedback voltage V_f opposes V_s, the input current I_i is less than it would be if V_f were absent, as shown in the Fig. 3.11.

Hence, the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback, for the circuit shown in Fig. 3.11.

On the other hand, if the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current), it decreases the input resistance. Since $I_s = I_i + I_f$, the current I_s drawn from the signal source is increased over what it would be if there were no feedback current, as shown in the Fig. 3.12.

Hence, the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in Fig. 3.12. Now we see the effect of negative feedback on input resistance in different topologies (ways) of introducing negative feedback and obtain R_{if} quantitatively.

Voltage series feedback

The voltage series feedback topology shown in Fig. 3.13 with amplifier is replaced by Thevenin's model. Here, A_v represents the open circuit voltage gain taking R_s into account. since throughout the discussion of feedback amplifiers we will consider R_s to be part of the amplifier and we will drop the subscript on the transfer gain and input resistance (A_v instead of A_{vs} and R_{if} instead of R_{ifs}).

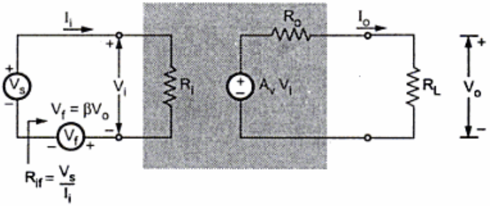


Fig. 3.13

Look at Fig. 3.13 the input resistance with feedback is given as,

$$R_{if} = \frac{V_s}{I_i} \qquad \dots (18)$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f$$

$$= I_i R_i + \beta V_o \qquad \dots (19)$$

The output voltage V_o is given as,

$$V_o = \frac{A_v V_i R_L}{R_o + R_L}$$

$$= A_V I_i R_i = A_V V_i \qquad \dots (20)$$

where $$A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}$$

Key Point: A_v *represents the open circuit voltage gain without feedback and* A_V *is the voltage gain without feedback taking the load* R_L *into account.*

Substituting value of V_o from equation (20) in equation (19) we get,

$$V_s = I_i R_i + \beta A_V I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i + \beta A_V R_i$$

$$\therefore \quad R_{if} = R_i (1 + \beta A_V) \qquad \dots (21)$$

Current series feedback

The current series feedback topology is shown in Fig. 3.14 with amplifier input circuit is represented by Thevenin's equivalent circuit and output circuit by Norton's equivalent circuit.

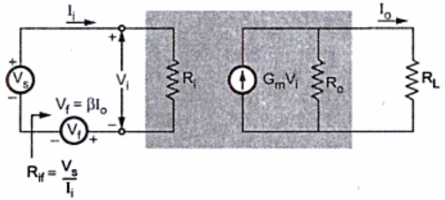


Fig. 3.14

Looking at Fig. 3.14 the input resistance with feedback is given as,

$$R_{if} = \frac{V_s}{I_i}$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f = I_i R_i + \beta I_o \qquad \dots (22)$$

The output current I_o is given as,

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \qquad \dots (23)$$

where $$G_M = \frac{I_o}{V_i}$$

$$G_M = \frac{G_m R_o}{R_o + R_L}$$

Key Point: *G_m represents the open circuit transconductance without feedback and G_M is the transconductance without feedback taking the load R_L into account.*

Substituting value of I_o from equation (23) into equation (22) we get,

$$V_s = I_i R_i + \beta G_M V_i$$

$$= I_i R_i + \beta G_M I_i R_i \quad \because V_i = I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i (1 + \beta G_M)$$

$$\therefore \quad R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta G_M) \qquad \dots (24)$$

Current shunt feedback

The current shunt feedback topology is shown in Fig. 3.15 with amplifier input and output circuit replaced by Norton's equivalent circuit

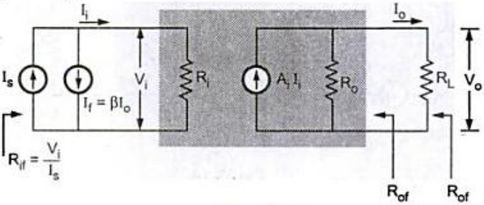


Fig. 3.15

Applying KCL to the input node we get,

$$I_s = I_i + I_f$$

$$= I_i + \beta I_o \qquad \dots (25)$$

The output current I_o is given as,

$$I_o = \frac{A_i I_i R_o}{R_o + R_L}$$

$$= A_I I_i \qquad \dots (26)$$

where $$A_I = \frac{A_i R_o}{R_o + R_L}$$

Key Point: A_i *represents the open circuit current gain without feedback and* A_I *is the current gain without feedback taking the load* R_L *into account.*

Substituting value of I_o from equation (26) into equation (25) we get,

$$I_s = I_i + \beta A_I I_i$$

$$= I_i (1 + \beta A_I)$$

The input resistance with feedback is given as,

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i\,(1+\beta\,A_I)}$$

$$= \frac{R_i}{(1+\beta A_I)} \qquad \because\ R_i = \frac{V_i}{I_i} \qquad \ldots (27)$$

Voltage shunt feedback

The voltage shunt feedback topology is shown in Fig. 3.16 with amplifier input circuit is represented by Norton's equivalent circuit and output circuit represented by Thevenin's equivalent.

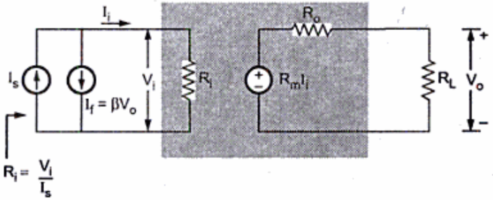


Fig. 3.16

Applying KCL at input node we get,

$$I_s = I_i + I_f$$

$$= I_i + \beta V_o \qquad \ldots (28)$$

The output voltage V_o is given as,

$$V_o = \frac{R_m\ I_i R_o}{R_o + R_L}$$

$$= R_M\ I_i \qquad \ldots (29)$$

where $$R_M = \frac{R_m R_o}{R_o + R_L}$$

Key Point: *R_m represents the open circuit transresistance without feedback and R_M is the transresistance without feedback taking the load* R_L *into account.*

Substituting value of V_o from equation (29) into equation (28) we get,

$$I_s = I_i + \beta\ R_M\ I_i$$

$$= I_i\ (1+\beta\ R_M)$$

The input resistance with feedback R_{if} is given as,

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i(1+\beta R_M)}$$

$$\therefore \qquad R_{if} = \frac{R_i}{(1+\beta R_M)} \qquad \because R_i = \frac{V_i}{I_i} \qquad \text{... (30)}$$

Output resistance

The negative feedback which samples the output voltage, regardless of how this output signal is returned to the input, tends to decrease the output resistance, as shown in the Fig. 3.17.

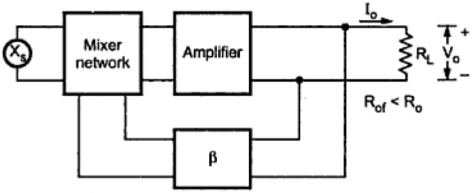


Fig. 3.17

On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 3.18.

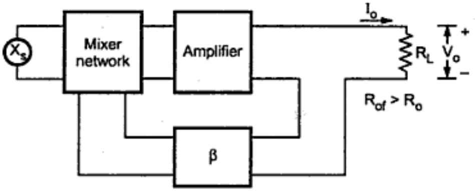


Fig. 3.18

Now, we see the effect of negative feedback on output resistance in different topologies (ways) of introducing negative feedback and obtain R_{of} quantitatively.

Voltage series feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.19.

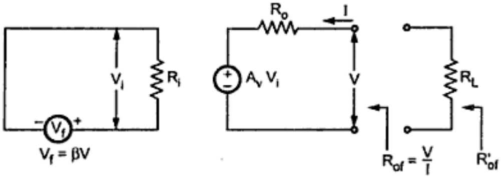


Fig. 3.19

Applying KVL to the output side we get,

$$A_v V_i + I R_o - V = 0$$

$$\therefore \qquad I = \frac{V - A_v V_i}{R_o} \qquad \dots (31)$$

The input voltage is given as,

$$V_i = -V_f = -\beta V \quad \because V_s = 0 \qquad \dots (32)$$

Substituting the V_i from equation (32) in equation (31) we get,

$$I = \frac{V + A_v \beta V}{R_o}$$

$$= \frac{V(1 + \beta A_v)}{R_o}$$

$$\therefore \qquad R_{of} = \frac{V}{I}$$

$$= \frac{R_o}{(1 + \beta A_v)} \qquad \dots (33)$$

Key Point: *Here* A_v *is the open loop voltage gain without taking* R_L *in account.*

$$R'_{of} = R_{of} \parallel R_L$$

$$= \frac{R_{of} \times R_L}{R_{of} + R_L} = \frac{\left(\frac{R_o}{1 + \beta A_v}\right) \times R_L}{\frac{R_o}{(1 + \beta A_v)} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L(1 + \beta A_v)} = \frac{R_o R_L}{R_o + R_L + \beta A_v R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\dfrac{R_o R_L}{R_o + R_L}}{1 + \dfrac{\beta A_v R_L}{R_o + R_L}}$$

$$= \frac{R'_o}{1+\beta A_v} \qquad \because \; R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_v = \frac{A_v R_L}{R_o + R_L} \qquad \ldots (34)$$

Key Point : *Here A_v is the open loop voltage gain taking R_L into account.*

Voltage shunt feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.20.

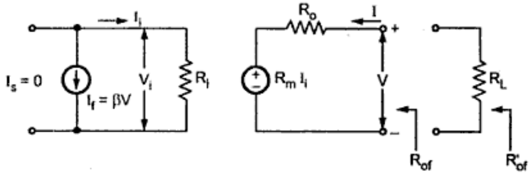


Fig. 3.20

Applying KVL to the output side we get,

$$R_m I_i + I R_o - V = 0$$

$$\therefore \qquad I = \frac{V - R_m I_i}{R_o} \qquad \ldots (35)$$

The input current is given as,

$$I_i = -I_f = -\beta V \qquad \ldots (36)$$

Substituting I_i from equation (36) in equation (35) we get,

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

$$\therefore \qquad R_{of} = \frac{V}{I}$$

$$= \frac{R_o}{1 + R_m \beta} \qquad \ldots (37)$$

Key Point: *Here. R_m is the open loop transresistance without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{\dfrac{R_o \times R_L}{1+R_m\,\beta}}{\dfrac{R_o}{1+R_m\,\beta}+R_L} = \frac{R_o\,R_L}{R_o + R_L\,(1+R_m\,\beta)}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_o\,R_L}{R_o + R_L}}{1+\dfrac{\beta R_m\,R_L}{R_o+R_L}}$$

$$= \frac{R'_o}{1+\beta R_M} \qquad \because R'_o = \frac{R_o\,R_L}{R_o+R_L} \text{ and } R_M = \frac{R_m\,R_L}{R_o+R_L} \qquad \dots (38)$$

Key Point: *Here,* R_M *is the open loop transresistance taking* R_L *in account.*

Current shunt feedback

In this topology, the output resistance can be measured by open circuiting the input source $I_s = 0$ and looking into the output terminals, with R_L disconnected, as shown in the Fig. 3.21.

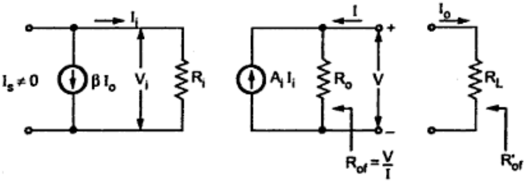


Fig. 3.21

Applying the KCL to the output node we get,

$$I = \frac{V}{R_o} - A_i\,I_i \qquad \dots (39)$$

The input current is given as,

$$I_i = -I_f = -\beta I_o \qquad \because I_s = 0$$

$$= \beta I \qquad \because I = -I_o \qquad \dots (40)$$

Substituting value of I_i from equation (40) in equation (39) we get,

$$I = \frac{V}{R_o} - A_i\,\beta I$$

$$\therefore \qquad I\,(1 + A_i\,\beta) = \frac{V}{R_o}$$

$$\therefore \qquad R_{of} = \frac{V}{I} = R_o\,(1 + \beta A_i) \qquad \ldots (41)$$

Key Point: *Here,* A_i *is the open loop current gain without taking* R_L *in account.*

$$R'_{of} = R_{of} \,||\, R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o\,(1+\beta A_i)\,R_L}{R_o\,(1+\beta A_i) + R_L} = \frac{R_o\,R_L\,(1+\beta A_i)}{R_o + R_L + \beta A_i\,R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_o\,R_L\,(1+\beta A_i)}{R_o + R_L}}{1 + \dfrac{\beta A_i\,R_o}{R_o + R_L}} = \frac{R'_o\,(1+\beta A_i)}{(1+\beta A_I)}$$

$$\because \qquad R'_o = \frac{R_o\,R_L}{R_o + R_L} \text{ and } A_I = \frac{A_i\,R_o}{R_o + R_L} \qquad \ldots (42)$$

Key Point: *Here,* A_I *is the open loop current gain taking* R_L *in account.*

Current series feedback

In this topology the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.22.

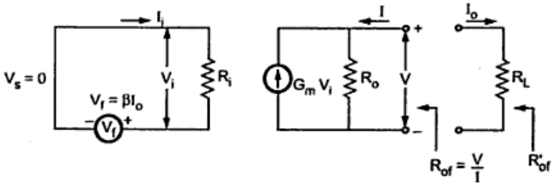


Fig. 3.22

Applying KCL to the output node we get,

$$I = \frac{V}{R_o} - G_m\,V_i \qquad \ldots (43)$$

The input voltage is given as,

$$V_i = -V_f = -\beta I_o$$

$$= \beta I \qquad \because I_o = -I \qquad \ldots (44)$$

Substituting value of V_i from equation (44) in equation (43) we get,

$$I = \frac{V}{R_o} - G_m \beta I$$

$$\therefore \quad I(1 + G_m \beta) = \frac{V}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I} = R_o(1 + G_m \beta) \quad \ldots (45)$$

Key Point: *Here,* G_m *is the open loop transconductance without taking* R_L *in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o(1+\beta G_m) R_L}{R_o(1+\beta G_m) + R_L} = \frac{R_o R_L (1+\beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_L R_o (1+\beta G_m)}{R_o + R_L}}{1 + \dfrac{\beta G_m R_o}{R_o + R_L}}$$

$$= \frac{R'_o (1+\beta G_m)}{1+\beta G_M} \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } G_M = \frac{G_m R_o}{R_o + R_L} \quad \ldots (46)$$

Key Point: *Note that here,* G_M *is the open loop current gain taking* R_L *in account.*

Table 3.1 summarizes the effect of negative feedback on amplifier.

Parameter	Voltage series	Current series	Current shunt	Voltage shunt
Gain with feedback	$A_{vf} = \frac{A_v}{1+\beta A_v}$ decreases	$G_{mf} = \frac{G_m}{1+\beta G_m}$ decreases	$A_{if} = \frac{A_i}{1+\beta A_i}$ decreases	$R_{mf} = \frac{R_m}{1+\beta R_{mf}}$ decreases
Stability	Improves	Improves	Improves	Improves
Frequency response	Improves	Improves	Improves	Improves
Frequency distortion	Reduces	Reduces	Reduces	Reduces
Noise and Nonlinear distortion	Reduces	Reduces	Reduces	Reduces
Input resistance	$R_{if} = R_i(1+\beta A_V)$ increases	$R_{if} = R_i(1+\beta G_M)$ increases	$R_{if} = \frac{R_i}{1+\beta A_I}$ decreases	$R_{if} = \frac{R_i}{1+\beta R_M}$ decreases
Output resistance	$R_{of} = \frac{R_o}{1+\beta A_v}$ decreases	$R_{of} = R_o(1+\beta G_m)$ increases	$R_{of} = R_o(1+\beta A_i)$ increases	$R_{of} = \frac{R_o}{1+\beta R_m}$ decreases

Table 3.1

➠ **Example 3.1 :** *An amplifier has mid-band voltage gain* ($A_{v\,mid}$) *of 1000 with* f_L *= 50 Hz and* f_H *= 50 kHz, if 5 % feedback is applied then calculate gain* f_L *and* f_H *with feedback.*

Solution : Given $\beta = \frac{5}{100} = 0.05$, $f_L = 50$, $f_H = 50$ kHz and $A_{V\,mid} = 1000$

a) Gain with feedback

$$A_{V\,mid} = \frac{A_{V\,mid}}{1+\beta A_{V\,mid}} = \frac{1000}{1+0.05\times 1000}$$

$$= \mathbf{19.6}$$

b)

$$f_{Lf} = \frac{f_L}{1+\beta A_{V\,mid}} = \frac{50}{1+0.05\times 1000}$$

$$= \mathbf{0.98\ Hz}$$

c)

$$f_{Hf} = f_H \times (1+\beta A_{V\,mid}) = 50\times 10^3 \times (1+0.05\times 1000)$$

$$= \mathbf{2.55\ MHz}$$

➠ **Example 3.2 :** *An amplifier with open loop voltage gain of 1000 delivers 10 W of power output at 10 % second harmonic distortion when input is 10 mV. If 40 dB negative feedback is applied and output power is to remain at 10 W, determine required input signal* V_s *and second harmonic distortion with feedback.*

Solution : Given $A_V = 1000$, Output power = 10 W,

a) β :

$$-40 = 20\log\left[\frac{1}{1+\beta A}\right]$$

$$\therefore \quad 1+\beta A = 100$$

$$\therefore \quad \beta A = 99$$

$$\therefore \quad \beta = \frac{99}{1000} = 0.099$$

Gain of the amplifier with feedback is given as

$$A_{Vf} = \frac{A_V}{1+\beta A_V} = \frac{1000}{100} = \mathbf{10}$$

b) To maintain output power 10 W, we should maintain output voltage constant and to maintain output voltage constant with feedback gain required V_s is

$$V_{sf} = V_s \times 100 = 10\ \text{mV} \times 100$$

$$= \mathbf{1\ V}$$

c) Second harmonic distortion is reduced by factor $1+\beta A$.

$$\therefore \quad D_{2f} = \frac{D_2}{1+\beta A} = \frac{0.1}{1+\beta A} = \frac{0.1}{100} = 0.001$$

$$= 0.1\ \%$$

Example 3.3 : *An amplifier with open loop gain of A = 2000 ± 150 is available. It is necessary to have the amplifier whose voltage gain varies by not more than ± 0.2 %. Calculate β and A_f.*

Solution : a) We know that

$$\frac{dA_f}{A_f} = \frac{0.1}{1+\beta A} \cdot \frac{dA}{A}$$

$$\therefore \quad \frac{0.2}{100} = \frac{1}{1+\beta A} \times \frac{150}{2000}$$

$$\therefore \quad 1+\beta A = 37.5$$

$$\therefore \quad \beta A = 36.5$$

$$\therefore \quad \beta = \frac{36.5}{2000} = 0.01825$$

$$= 1.825\ \%$$

b) $$A_f = \frac{A}{1+\beta A} = \frac{2000}{1+0.01825 \times 2000}$$

$$= 53.33$$

3.6 Advantages and Disadvantages of Negative Feedback

The introduction of negative feedback in the amplifier circuit reduces gain of the amplifier. This is the main disadvantage of using negative feedback in the amplifier. Inspite of this disadvantage the negative feedback is used in almost every amplifier, due to number of advantages provided by it. Some of the advantages provided by negative feedback are as listed below.

- Negative feedback stabilizes the gain of the amplifier.
- Negative feedback increases the bandwidth of the amplifier so that it provides nearly constant gain for large frequency range of the input signal.
- Negative feedback reduces the distortion in the amplifier output.
- Series negative feedback increases the input resistance of the amplifier. This avoids loading of the source of the amplifier.

- Voltage negative feedback decreases the output resistance of the amplifier. This avoids loading of amplifier itself when driving an output load.
- Negative feedback also stabilizes operating point.

3.7 Methodology of Feedback Amplifier Analysis

To analyze the feedback amplifier it is necessary to go through the following steps.

Step 1 : Identify topology (Type of feedback).

a) To find the type of sampling network

1. By shorting the output i.e. $V_o = 0$, if feedback signal (X_f) becomes zero then we can say that it is "voltage sampling".
2. By opening the output loop i.e. $I_o = 0$, if feedback signal (X_f) becomes zero then we can say that it is "current sampling".

b) To find the type of mixing network

1. If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop, we can say that it is "series mixing".
2. If the feedback signal is subtracted from the externally applied signal as a current in the input loop, we can say that it is "shunt mixing".

Thus by determining type of sampling network and mixing network, type of feedback amplifier can be determine. For example, if amplifier uses a voltage sampling and series mixing then we can say that it is a voltage series amplifier.

Step 2 : Find the input circuit.

1. For voltage sampling make $V_o = 0$ by shorting the output.
2. For current sampling make $I_o = 0$ by opening the output loop.

Step 3 : Find the output circuit.

1. For series mixing make $I_i = 0$ by opening the input loop.
2. For shunt mixing make $V_i = 0$ by shorting the input.

Step 2 and step 3 ensure that the feedback is reduced to zero without altering the loading on the basic amplifier.

Step 4 : Optional. Replace each active device by its h-parameter model at low frequency.

Step 5 : Find the open loop gain (gain without feedback), A of the amplifier.

Step 6 : Indicate X_f and X_o on the circuit and evaluate $\beta = X_f\ X_o$.

Step 7 : From A and β, find D, A_f, R_{if}, R_{of} and R'_{of}.

Characteristics	**Topology**			
	Voltage series	**Current series**	**Current shunt**	**Voltage shunt**
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
To find output loop, set	$I_i = 0$	$I_i = 0$	$V_i = 0$	$V_i = 0$
Single source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_V = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1 + \beta A$	$1 + \beta A_V$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_V/D	G_M/D	A_I/D	R_M/D
R_{if}	$R_i D$	$R_i D$	R_i/D	R_i/D
R_{of}	$\frac{R_o}{1+\beta A_v}$	$R_o (1 + \beta G_m)$	$R_o (1 + \beta A_i)$	$\frac{R_o}{1+\beta R_m}$
$R'_{of} = R_{of} \parallel R_L$	$\frac{R'_o}{1+\beta A_V}$	$\frac{R'_o(1+\beta G_m)}{1+\beta G_M}$	$\frac{R'_o(1+\beta A_i)}{1+\beta A_I}$	$\frac{R'_o}{1+\beta R_M}$

Table 3.2

3.8 Voltage Series Feedback

In this section, we will see two examples of the voltage series amplifier. First we will analyze transistor emitter follower circuit and then source follower using FET.

3.8.1 Transistor Emitter Follower

Fig. 3.23 shows the transistor emitter follower circuit. Here feedback voltage is the voltage across R_o and sampled signal is V_o across R_e.

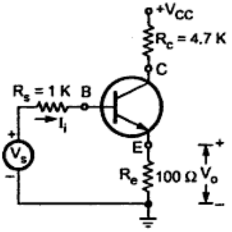


Fig. 3.23

Analysis

Step 1 : Identify topology.

By shorting output voltage ($V_o = 0$), feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 3.23 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

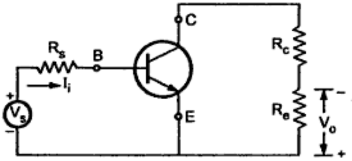


Fig. 3.24

To find the input circuit, set $V_o = 0$, and hence V_s in series with R_s appears between B and E. To find the output circuit, set $I_i = I_b = 0$, and hence R_e appears only in the output loop. With these connections we obtain the circuit as shown in the Fig. 3.24.

Step 4 : Replace transistor by its h-parameter equivalent circuit.

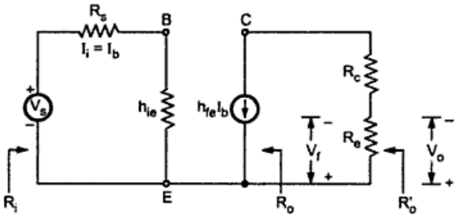


Fig. 3.25 Transistor replaced by its approximate h-parameter equivalent circuit

Step 5 : Find open loop voltage gain.

$$A_V = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_c}{V_s}$$

Applying KVL to input loop we get,

$$V_s = I_b (R_s + h_{ie})$$

Substituting value of V_s we get,

$$A_V = \frac{h_{fe}\, R_e}{R_s + h_{ie}} = \frac{50 \times 100}{1\,K + 1.1\,K} = 2.38$$

Step 6 : Indicate V_o and V_f and calculate β.

We have $\beta = \frac{V_f}{V_o} = 1$ ∵ Both voltage present across R_e.

Step 7 : Calculate D, A_{Vf} , R_{if} , R_{of} and R'_{of}.

$$\begin{aligned}
D &= 1+\beta A_V \\
&= 1 + 1 \times 2.38 \\
&= 3.38 \\
A_{Vf} &= \frac{A_V}{1+\beta A_V} \\
&= \frac{A_V}{D} = \frac{2.38}{3.38} \\
&= 0.7 \\
R_i &= R_s + h_{ie} \\
&= 1\,K + 1.1\,K = 2.1\,K \\
R_{if} &= R_i\, D \\
&= 2.1\,K \times 3.38 \\
&= 7.098\,K \\
R_o &= \infty \\
R_{of} &= \infty \\
R'_{of} &= \frac{R'_o}{D} \qquad \text{where } R'_o = R_e \\
\therefore \quad R'_{of} &= \frac{R_e}{D} = \frac{100}{3.38} \\
&= 29.58\ \Omega
\end{aligned}$$

3.8.2 FET Source Follower

Fig. 3.26 shows the FET source follower circuit. Here feedback voltage is the voltage across R_s and sampled signal is V_o across R_e.

Analysis :

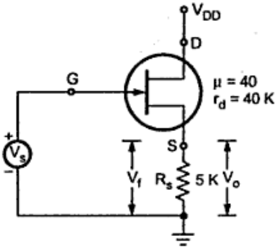


Fig. 3.26

Step 1 : Identify topology.

By shorting output voltage $V_o = 0$, feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 3.26 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

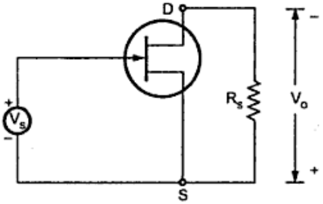


Fig. 3.27

Step 2 and Step 3 : Find input and output circuit.

To find the input circuit, set $V_s = 0$, and hence V_s appears between G and S. To find the output circuit, set $I_i = I_G = 0$, and hence R_s appears in the output loop. With these connections we obtain the circuit as shown in the Fig. 3.27.

Step 4 : Replace FET by its equivalent circuit.

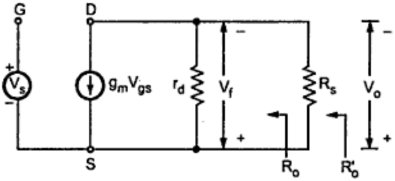


Fig. 3.28

Step 5 : Find open loop voltage gain.

$$A_V = \frac{V_o}{V_s} = \frac{g_m\ V_{gs}\ r_d R_s}{(r_d + R_s)\ V_s}$$

$$= \frac{g_m\ r_d\ R_s}{r_d + R_s} \qquad \because V_{gs} = V_s \qquad \dots (1)$$

$$= \frac{\mu R_s}{r_d + R_s} \qquad \because \mu = g_m\ r_d \qquad \dots (2)$$

$$= \frac{40 \times 5\ \text{K}}{40\ \text{K} + 5\ \text{K}} = 4.44$$

Step 6 : Indicate V_o and V_f and calculate β.

$$\beta = \frac{V_f}{V_o} = 1 \qquad \because \text{Both voltages present across } R_s$$

Step 7 : Calculate D, A_{Vf}, R_{if}, R_{of} and R'_{of}

$$D = 1 + \beta A_V = 1 + 1 \times 4.44$$

$$= 5.44 \qquad \dots (3)$$

$$A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{A_V}{D}$$

$$= \frac{4.44}{5.44} = 0.816$$

$$R_i = \infty \text{ and hence } R_{if} = R_i\ D = \infty \qquad \dots (4)$$

$$R_o = r_d = 40\ \text{k}\Omega \qquad \dots (5)$$

$$R_{of} = \frac{R_o}{D} = \frac{40\ \text{K}}{5.44} = 7.35\ \text{K} \qquad \dots (6)$$

$$R'_{of} = \frac{R'_o}{D}$$

where $R'_o = R_s \parallel r_d$

$$= \frac{R_s r_d}{R_s + r_d} = \frac{5\ \text{K} \times 40\ \text{K}}{5\ \text{K} + 40\ \text{K}} = 4.44\ \text{K}$$

$$\therefore \quad R'_{of} = \frac{4.44\ \text{K}}{5.44} = 816.2\ \Omega \qquad \dots (7)$$

3.8.3 Voltage Series Feedback Pair

Fig. 3.29 shows two cascaded stages. The output of second stage is connected through feedback network to the input of first stage in opposition to the input signal V_s.

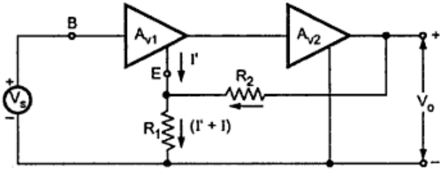


Fig. 3.29 Voltage series feedback pair

Analysis :

Step 1 : Identify topology.

By shorting output voltage $V_o = 0$, feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 3.29 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

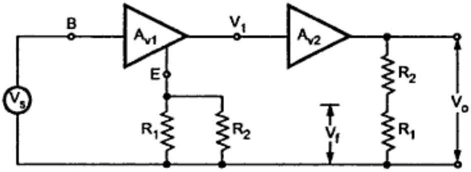

B
A_{V1}
V_1
A_{V2}
E
V_s
R_1
R_2
V_f
R_2
R_1
V_o

Fig. 3.30

To find input circuit, set $V_o = 0$, and hence R_2 appears in parallel with R_1 at first emitter. To find the output circuit, set $I_i = 0$ and hence R_1 appears in series with R_2 across output. The resulting circuit is shown in Fig. 3.30.

For this circuit, feedback factor β can be calculated as,

$$\beta = \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_2} \quad \dots (8)$$

➡ **Example 3.4 :** *Transistors in the feedback amplifier shown in Fig. 3.31 are identical and their 'h' parameters are* $h_{ie} = 1100\ \Omega$, $h_{fe} = 100$, $h_{re} = h_{oe} = 0$. *Neglect capacitances of all capacitors.*

i) State topology with justification.

ii) Calculate β, A_V, A_{Vf}, R_{if}, R_{of} *and* R'_{of}.

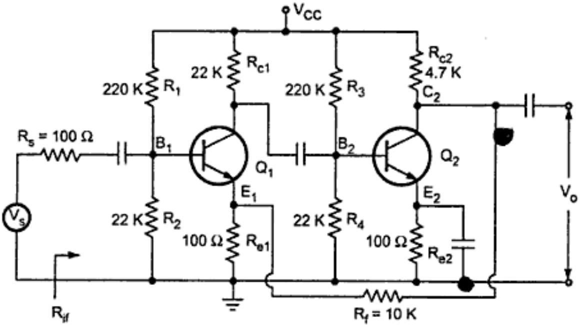

V_{CC}
R_{c2}
4.7 K
C_2
22 K
R_{c1}
220 K
R_1
220 K
R_3
$R_s = 100\ \Omega$
B_1
B_2
Q_1
Q_2
E_1
E_2
V_o
V_s
22 K
R_2
22 K
R_4
100 Ω
R_{e1}
100 Ω
R_{e2}
R_{if}
$R_f = 10$ K

Fig. 3.31

Solution : **Step 1 :** Identify topology.

The feedback voltage is applied across the resistance R_{e1} and it is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_0 = 0$ (connecting C_2 to ground), which gives parallel combination of R_e with R_f at E_1. To find output circuit, set $I_i = 0$ (opening the input node E_1 at emitter of Q_1), which gives series combination of R_f and R_{e1} across the output. The resultant circuit is shown in Fig. 3.32.

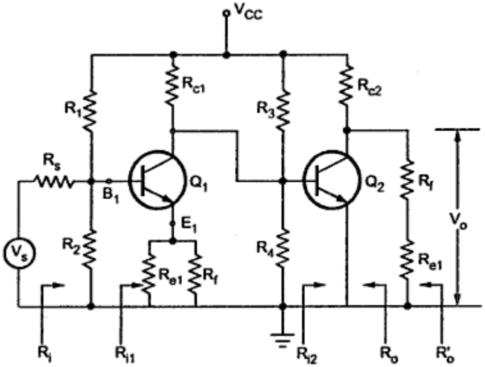


Fig. 3.32

Step 4 : Find open loop voltage gain (A_V).

$$R_{L2} = R_{c2} \parallel (R_{e1} + R_f)$$
$$= 4.7\text{ K} \parallel (100 + 10\text{ K})$$
$$= 3.21\text{ k}\Omega$$

$$A_{i2} = -h_{fe} = -100$$
$$R_{i2} = h_{ie} = 1100\ \Omega$$
$$A_{V2} = \frac{A_{i2} R_{L2}}{R_{i2}} = \frac{-100 \times 3.21\text{ K}}{1100\Omega}$$
$$= -291.82$$

$$A_{i1} = -h_{fe} = -100$$
$$R_{L1} = R_{c1} \parallel R_3 \parallel R_4 \parallel R_{i2}$$
$$= 22\text{ K} \parallel 220\text{ K} \parallel 22\text{ K} \parallel 1100$$
$$= 995\ \Omega$$

$$R_{i1} = h_{ie} + (1+h_{fe})R_{e1eff} \quad \text{where } R_{e1eff} = (R_{e1}||R_f)$$

$$= 1100 + (1 + 100)(100\ \Omega \,||\, 10\ K)$$

$$= 11.099\ k\Omega$$

$$\therefore \quad A_{V1} = \frac{A_{i1}R_{L1}}{R_{i1}} = \frac{-100\times 995}{11.099\times 10^3}$$

$$= -\ 8.96$$

The overall voltage gain without feedback is given as,

$$A_V = A_{V1}\times A_{V2} = (-291.82)\times(-8.96)$$

$$= 2614.7$$

The overall voltage gain taking R_s in account is given as,

$$A_V = \frac{V_o}{V_s} = \frac{A_V R_{i1}}{R_{i1}+R_s} = \frac{2614.7\times 11.099\times 10^3}{11.099\times 10^3 + 100}$$

$$= 2591.35$$

Step 5 : Calculate β.

Looking at Fig. 3.33.

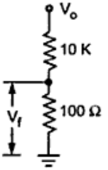


Fig. 3.33

$$\beta = \frac{V_f}{V_o} = \frac{100}{100+10\times 10^3}$$

$$= 0.0099$$

$$D = 1+\beta A_V = 1+0.0099\times 2591.35$$

$$= 26.65$$

$$\therefore \quad A_{Vf} = \frac{A_V}{D} = \frac{2591.35}{26.65} = 97.23$$

$$R_{if} = R_{i1}\,D = 11.099\times 10^3\times 26.65$$

$$= 295.788\ k\Omega$$

$$R'_{if} = R_{if} \,||\, R_1 \,||\, R_2 = 295.788\ K \,||\, 220\ K \,||\, 22\ K$$

$$= 18.73\ k\Omega$$

$$R_{of} = \frac{R_o}{D} = \frac{\infty}{D} = \infty$$

$$\therefore \quad R'_{of} = \frac{R'_o}{D} \quad \text{where } R'_o = R_{L2}$$

$$\therefore \quad R'_{of} = \frac{3.21\times 10^3}{26.65} = 120.45\ \Omega$$

3.9 Current Series Feedback

In this section, we will see two examples of the current series feedback amplifier. First we will analyze transistor common emitter circuit with unbypassed emitter resistance and then common source with unbypassed source resistance.

3.9.1 Common Emitter Configuration with Unbypassed R_e

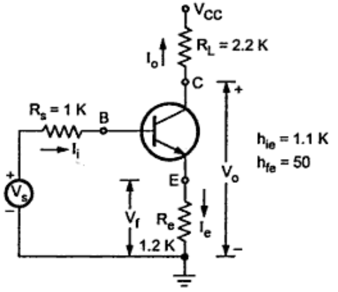


Fig. 3.34

Fig. 3.34 shows the common emitter circuit with unbypassed R_e. The common emitter circuit with unbypassed R_e is an example of current series feedback. In this configuration resistor R_e is common to base to emitter input circuit as well as collector to emitter output circuit and input current I_b as well as output current I_c both flow through it. The voltage drop across R_e, $V_f = (I_b + I_c) = I_e R_e = I_c R_e = -I_o R_e$. This voltage drop shows that the output current I_o is being sampled and it is converted to voltage by feedback network. At input side voltage V_f is subtracted from V_s to produce V_i. Therefore, the feedback applied in series.

Analysis

Step 1 : Identify topology.

By opening the output loop, (output current, $I_o = 0$), feedback signal becomes zero and hence it is current sampling. Looking at Fig. 3.34 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a current series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

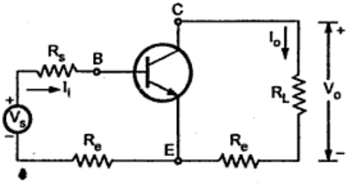


Fig. 3.35

To find input circuit set $I_o = 0$, then R_e appears at the input side. To find output circuit set $I_i = 0$, then R_e appears in the output circuit. The resulting circuit is shown in the Fig. 3.35.

Step 4 : Replace transistor with its approximate h-parameter equivalent circuit.

Fig. 3.36 shows the approximate h-parameter equivalent circuit.

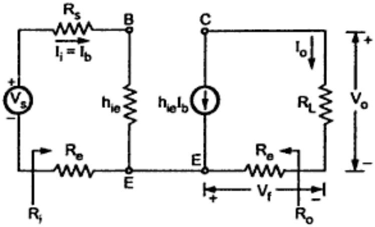


Fig. 3.36 Approximate h-parameter equivalent circuit

Step 5 : Find open loop transfer gain.

$$G_M = \frac{I_o}{V_i} = \frac{-h_{fe}I_b}{V_s}$$

$$= \frac{-h_{fe}I_b}{I_b(R_s + h_{ie} + R_e)}$$

$$= \frac{-h_{fe}}{R_s + h_{ie} + R_e} = \frac{50}{1\,K + 1.1\,K + 1.2\,K}$$

$$= -0.015 \qquad \ldots (1)$$

Step 6 : Indicate I_o and V_f and calculate β.

$$\beta = \frac{V_f}{I_o} = \frac{I_e R_e}{I_o}$$

$$= \frac{-I_o R_e}{I_o} = -R_e \qquad \because I_e = -I_o \quad \ldots (2)$$

$$= -1.2\,K$$

Step 7 : Calculate D, G_{Mf}, A_{Vf}, R_{if}, R_{of} and R'_{of}

$$D = 1 + \beta G_M = 1 + (-1.2\,K) \times (-0.015)$$

$$= 19.18 \qquad \ldots (3)$$

$$G_{Mf} = \frac{G_M}{D} = \frac{-0.015}{19.18}$$

$$= -0.782 \times 10^{-3} \qquad \ldots (4)$$

The voltage gain A_{Vf} is given as,

$$A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s} = G_{Mf}\ R_L \qquad \because G_{Mf} = \frac{I_o}{V_s}$$

$$= -0.782 \times 10^{-3} \times 2.2\ K$$

$$= -1.72 \qquad \ldots (5)$$

Looking at Fig. 3.36 R_i can be given as,

$$R_i = R_s + h_{ie} + R_e$$

$$= 1\ K + 1.1\ K + 1.2\ K = 3.3\ K \qquad \ldots (6)$$

$$R_{if} = R_i\ D = 3.3\ K \times 19.18$$

$$= 63.294\ K \qquad \ldots (7)$$

Looking at Fig. 3.36 R_o is given as,

$$R_o = \infty \qquad \ldots (8)$$

$$\therefore \quad R_{of} = R_o\ D = \infty \qquad \ldots (9)$$

$$R'_{of} = R_{of} \parallel R_L$$

$$= R'_L \qquad \because R_{of} = \infty$$

$$= 2.2\ K \qquad \ldots (10)$$

3.9.2 Common Source Configuration with R_s Unbypassed

Fig. 3.37 shows the common source circuit with unbypassed R_s. Here, the feedback signal is a voltage across R_s and the sampled signal is the load current I_o.

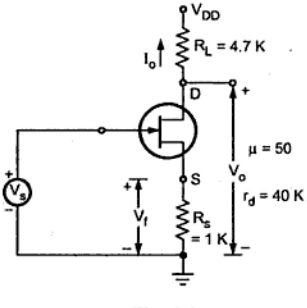


Fig. 3.37

Analysis

Step 1 : Identify topology.

By setting $V_o = 0$, drain current does not become zero therefore feedback does not become zero. Hence this is not voltage sampling. On the other hand, by setting $I_o = 0$, we have $V_f = 0$. Hence this is current sampling. The feedback voltage V_f is mixed in series with the input source. Hence the topology used is a current series feedback.

Step 2 and step 3 : Find input and output circuit.

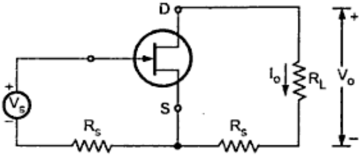


Fig. 3.38

To find input circuit set $I_o = 0$, then R_s appears at the input side. To find output circuit set $I_i = 0$, then R_s appears in the output circuit. The resulting circuit is shown in the Fig. 3.38.

Step 4 : Replace FET with its equivalent circuit.

Fig. 3.39 shows the equivalent circuit.

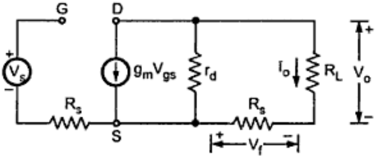


Fig. 3.39 FET replaced by its equivalent circuit

Step 5 : Find the open loop transconductance.

$$G_M = \frac{I_o}{V_s} = \frac{\frac{-g_m V_{gs} r_d}{r_d + R_L + R_s}}{V_s}$$

$$= \frac{-g_m r_d}{r_d + R_L + R_s} \quad \because V_s = V_{gs} \qquad \dots (11)$$

$$= \frac{-\mu}{r_d + R_L + R_s} \quad \because \mu = g_m r_d \qquad \dots (12)$$

$$= \frac{-50}{40\text{ K} + 4.7\text{ K} + 1\text{ K}} = -1.09 \times 10^{-3}$$

Step 6 : Calculate β.

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_s}{I_o}$$

$$= -R_s = -1\text{ K} \qquad \dots (13)$$

Step 7 : Calculate D, G_{Mf}, A_{Vf}, R_{if}, R_{of} and R'_{of}.

$$D = 1 + \beta\, G_M$$

$$= 1 + (-1\text{ K})(-1.09\times10^{-3})$$

$$= 2.09 \qquad \text{... (14)}$$

$$G_{Mf} = \frac{G_M}{D} = \frac{-1.09\times10^{-3}}{2.09}$$

$$= -0.5215\times10^{-3} \qquad \text{... (15)}$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s}$$

$$= G_{Mf}\, R_L \qquad \because G_{Mf} = \frac{I_o}{V_s}$$

$$= (-0.5215\times10^{-3})\times(4.7\text{ K})$$

$$= -2.45 \qquad \text{... (16)}$$

Looking at Fig. 3.39 R_i can be given as,

$$R_i = \infty \qquad \text{... (17)}$$

$$\therefore \quad R_{if} = R_i\, D = \infty \qquad \text{... (18)}$$

Looking at Fig. 3.39 R_o can be given as,

$$R_o = r_d + R_s = 40\text{ K} + 1\text{ K} = 41\text{ K} \qquad \text{... (19)}$$

$$R_{of} = R_o\,(1+\beta G_m) \text{ where } G_m = \lim_{R_L\to 0} G_M \qquad \text{... (20)}$$

$$\therefore \quad 1+\beta G_m = \frac{r_d + (1+\mu) R_s}{r_d + R_s}$$

$$\therefore \quad R_{of} = (r_d + R_s)\times\frac{r_d + (1+\mu) R_s}{r_d + R_s}$$

$$= r_d + (1+\mu) R_s$$

$$= 40\text{ K} + (1+50)\times 1\text{ K} = 91\text{ K} \qquad \text{... (21)}$$

$$R'_{of} = R_L \parallel R_{of}$$

$$= 4.7\text{ K} \parallel 91\text{ K} = 4.47\text{ K} \qquad \text{... (22)}$$

3.10 Current Shunt Feedback

Fig. 3.40 shows two transistors in cascade connection with feedback from second emitter to first base through resistor R′. Here, the feedback network formed by R′ and R_{e2} divides the current I_e. Since $I_e = -I_o$, the feedback network gives current feedback. At input side, we see that $I_i = I_s - I_f$, i.e. I_f is shunt subtracted from I_s to get I_i. Therefore, this configuration is a current shunt feedback.

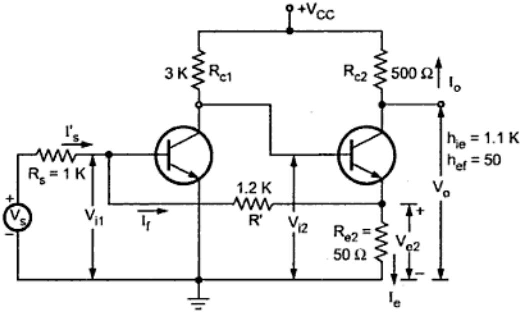

+V_CC
3 K
R_c1
R_c2
500 Ω
I_o
h_ie = 1.1 K
h_ef = 50
I'_s
R_s = 1 K
V_s
+
−
V_i1
I_f
1.2 K
R'
V_i2
R_e2 = 50 Ω
V_e2
+
−
V_o
I_e

Fig. 3.40

Step 1 : Identify topology.

By shorting output voltage ($V_o = 0$), feedback signal does not become zero and hence it is not voltage sampling. By opening the output loop ($I_o = 0$), feedback signal becomes zero and hence it is a current feedback. The feedback signal appears in shunt with input ($I_i = I_s - I_f$), hence the topology is current shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

The input circuit of the amplifier without feedback is obtained by opening the output loop at the emitter of Q_2 ($I_o = 0$). This places R′ in series with R_e from base to emitter of Q_1. The output circuit is found by shorting the input node (the base of Q_1), i.e. making $V_i = 0$. This places R′ in parallel with R_e. The resultant equivalent circuit is shown in Fig. 3.41.

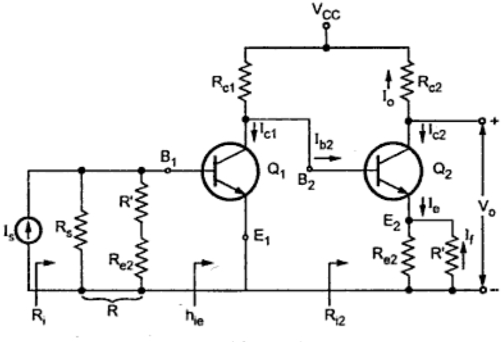

V_CC
R_c1
R_c2
I_o
I_c1
I_b2
I_c2
+
B_1
Q_1
B_2
Q_2
I_e
V_o
E_2
I_s
R_s
R'
R_e2
E_1
R_e2
R'
I_f
−
R_i
R
h_ie
R_i2

Fig. 3.41

Step 4 : Find open circuit transfer gain.

$$A_I = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s} \quad \ldots (1)$$

We know that,

$$\frac{-I_{c2}}{I_{b2}} = A_{i2} = -h_{fe} = -50 \text{ and} \quad \ldots (2)$$

$$\frac{-I_{c1}}{I_{b1}} = A_{i1} = -h_{fe} = -50$$

$$\therefore \quad \frac{I_{c1}}{I_{b1}} = 50 \quad \ldots (3)$$

Looking at Fig. 3.41 we can write,

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}} \quad \ldots (4)$$

where

$$R_{i2} = h_{ie} + (1 + h_{fe})(R_{e2} \parallel R')$$

$$= 1.1 + (51)\left(\frac{50 \times 1.2 \text{ K}}{50 + 1.2 \text{ K}}\right)$$

$$= 3.55 \text{ K}$$

$$\therefore \quad \frac{I_{b2}}{I_{c1}} = \frac{-3 \text{ K}}{3 \text{ K} + 3.55 \text{ K}} = -0.457$$

Looking at Fig. 3.41 we can write,

$$\frac{I_{b1}}{I_s} = \frac{R}{R + h_{ie}} \quad \ldots (5)$$

where

$$R = R_s \parallel (R' + R_e) = \frac{1.2 \text{ K} \times 1.25 \text{ K}}{1.2 \text{ K} + 1.25 \text{ K}}$$

$$= 0.612 \text{ K}$$

$$\therefore \quad \frac{I_{b1}}{I_s} = \frac{0.612 \text{ K}}{0.612 \text{ K} + 1.1 \text{ K}} = 0.358$$

Substituting the numerical values obtained from equations (2), (3), (4) and (5) in equation (1) we get,

$$A_I = (-50) \times (-0.457) \times (50) \times (0.358)$$

$$= 406$$

Step 5 : Calculate β

Looking at Fig. 3.41 we can write,

$$I_f = \frac{-I_e\,R_{e2}}{R_e + R'}$$

$$= \frac{-I_c\,R_{e2}}{R_e + R'} \qquad \because\ I_e \cong I_c$$

$$= \frac{I_o\,R_{e2}}{R_{e2} + R'} \qquad \because\ I_o = -I_c$$

$$\therefore \qquad \beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2} + R'} = \frac{50}{50 + 1.2\text{ K}}$$

$$= 0.04$$

Step 6 : Calculate D, R_i, R_{if}, A_{If}, A_{Vf}, R_o, R_{of}.

$$D = 1 + \beta A_I = 1 + (0.04) \times 406$$

$$= 17.2$$

$$A_{If} = \frac{A_I}{D} = \frac{406}{17.2}$$

$$= 23.6$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-I_{c2}\,R_{c2}}{I_s\,R_s}$$

$$= \frac{A_{If}\,R_{c2}}{R_s} \qquad \because\ \frac{-I_{c2}}{I_s} = A_{If}$$

$$= \frac{(23.6)\,(500)}{1.2\text{ K}} = 9.83$$

$$R_i = R \parallel h_{ie} = \frac{0.612\text{ K} \times 1.1\text{ K}}{0.612\text{ K} + 1.1\text{ K}}$$

$$= 0.394\text{ K}$$

$$R_{if} = \frac{R_i}{D} = \frac{0.394\text{ K}}{17.2}$$

$$= 23\ \Omega$$

$$R_o = \infty \qquad \because\ h_{oe} = 0$$

$$\therefore \qquad R_{of} = R_o\,D = \infty$$

$$R'_o = R_o \parallel R_{c2} = \infty \parallel 500 = 500\ \Omega$$

From calculation for A_I we note that A_I is independent of the load $R_L = R_{c2}$. Hence $A_i = \lim_{R_{c2} \to 0} = A_I$

$$\therefore \qquad R'_{of} = R'_o \frac{1+\beta A_i}{1+\beta A_I} = R'_o = R_{c2}$$

$$= 500\ \Omega$$

3.11 Voltage Shunt Feedback

Fig. 3.42 shows a common emitter amplifier with a resistor R′ connected from the output to the input.

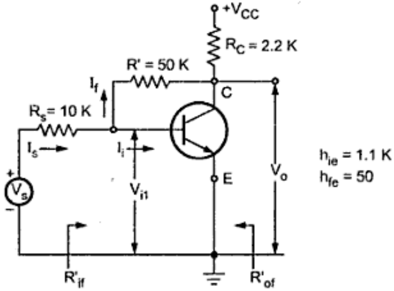


Fig. 3.42

Step 1 : Identify topology.

The feedback current I_f is given as,

$$I_f = \frac{V_i - V_o}{R'} \qquad \text{But } V_o > \beta V_i$$

$$\therefore \qquad I_f = \frac{-V_o}{R'}$$

By shorting output voltage ($V_o = 0$), feedback reduces to zero and hence it is a voltage sampling. As $I_i = I_s - I_f$, the mixing is shunt type and topology is voltage shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$, this places R′ between base and ground. To find output circuit, set $V_i = 0$, this places R′ between collector and ground.

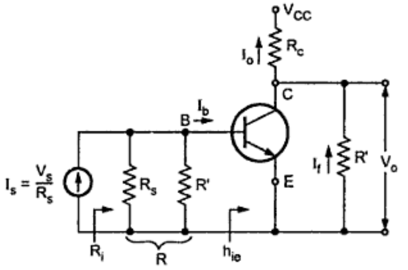


Fig. 3.43

The resultant circuit is shown in Fig. 3.43.

The feedback signal is the current I_f in the resistor R' which is in the output circuit as shown in the Fig. 3.43.

We have seen that

$$I_f = \frac{V_i - V_o}{R'} = \frac{-V_o}{R'} \qquad \because V_o > V_i$$

$$\therefore \quad \frac{I_f}{V_o} = \beta = \frac{-1}{R'}$$

$$R_{Mf} = \frac{R_M}{1+\beta\ R_M} = \frac{1}{\beta} \qquad \because \beta R_M >> 1$$

$$= -R'$$

$$\therefore \quad A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s}$$

$$= \frac{1}{\beta R_s} = \frac{-R'}{R_s}$$

Step 4 : Find the open circuit transresistance.

$$R_M = \frac{V_o}{I_s} = \frac{I_o R_c'}{I_s} = \frac{-I_c R_c'}{I_s} \qquad \dots (1)$$

where $R_c' = R_c \parallel R' = 2.2\text{ K} \parallel 50\text{ K}$

$= 2.1\text{ K}$

and $$\frac{-I_c}{I_s} = \frac{-I_c}{I_b}\frac{I_b}{I_s}$$

$$\frac{-I_c}{I_b} = A_i = -h_{fe} = -50 \text{ and} \qquad \dots (2)$$

$$\frac{I_b}{I_s} = \frac{R}{R + h_{ie}}$$ where $R = R_3 \parallel R' = 10\text{ K} \parallel 50\text{ K} = 8.33\text{ K}$

$$\therefore \quad \frac{I_b}{I_s} = \frac{8.33\text{ K}}{8.33\text{ K} + 1.1\text{ K}}$$

$$= 0.883 \qquad \ldots (3)$$

Substituting values of equations (2) and (3) in equation (1) we have,

$$R_M = \frac{-I_c\, R_c'}{I_s} = \frac{-I_c}{I_b}\,\frac{I_b}{I_s} \times R_c' = -h_{fe}\,\frac{R}{R+h_{ie}}\,R_c'$$

$$= (-50) \times (0.833) \times 2.1\text{ K}$$

$$= \mathbf{-92.715\ K}$$

Step 5 : Calculate β.

$$\beta = \frac{-1}{R'} = \frac{-1}{50\text{ K}}$$

$$= \mathbf{-2 \times 10^{-5}}$$

Step 6 : Calculate D, R_{Mf}, A_{Vf}, R_{if}, R_{of} and R'_{of}

$$D = 1 + \beta R_M$$

$$= 1 + (-2 \times 10^{-5})\,(-92.715 \times 10^3)$$

$$= \mathbf{2.854}$$

$$R_{Mf} = \frac{R_M}{D} = \frac{-92.715\text{ K}}{2.854}$$

$$= \mathbf{-32.48\ K}$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{Mf}}{R_s}$$

$$= \frac{-32.48\text{ K}}{10\text{ K}} = \mathbf{-3.248}$$

Looking at Fig. 3.43 we can write,

$$R_i = R \parallel h_{ie} = \frac{R\,h_{ie}}{R + h_{ie}}$$

$$= \frac{8.33\text{ K} \times 1.1\text{ K}}{8.33\text{ K} + 1.1\text{ K}} = \mathbf{0.971\ K}$$

$$R_{if} = \frac{R_i}{D} = \frac{0.971\text{ K}}{2.854}$$

$$= \mathbf{340.22\ \Omega}$$

If the input resistance looking to the right of R_s (from base to emitter in Fig. 3.42) is R'_{if}, then

$$R_{if} = R'_{if} || R_s$$

Solving this we get,

$$R'_{if} = \mathbf{352.2\ \Omega.}$$

The impedance seen by the voltage source V_s is $R_s + R'_{if} = 10\text{ K} + 352.2 = 10352\ \Omega$.

If R_c is considered an external load, the output resistance, neglecting feedback is

$$R_o = R' = \mathbf{50\ K}$$

Since $$R_m = \lim_{R_c \to \infty} R_M = -h_{fe} \frac{R}{R + h_{ie}} R'$$

$$= \frac{-50 \times 50000 \times 8330}{8330 + 1100} = -2.2\text{ M}\Omega$$

$\therefore$ $$\lim_{R_c \to \infty} R'_c = R'$$

$$R_{of} = \frac{R_o}{1 + \beta R_m} = \frac{50000}{1 + 2 \times 10^{-5} \times 2200000}$$

$$= \mathbf{1111\ \Omega}$$

$$R'_{of} = R_{of} || R_c = \frac{(1111)(2200)}{3311} = \mathbf{738.2\ \Omega}$$

Alternatively, R'_{of} can be calculated as,

$$R'_{of} = \frac{R'_o}{D} \quad \text{where } R'_o = R_c || R' = 2.2\text{ K} || 50\text{ K} = 2.1\text{ K}$$

$$= \frac{2.1\text{ K}}{2.854} = \mathbf{736\ \Omega}$$

Examples with Solutions

➡ **Example 3.5 :** *For the feedback amplifier shown in Fig. 3.44 calculate :*

i) A_{Vf} ii) R_{if} iii) R_{of}

Identify the topology of feedback and justify your answer.

Given : $r_s = 0$, $h_{fe} = 50$, $h_{ie} = 1.1\text{ K}$, $h_{re} = h_{oe} = 0$.

Assume all coupling and bypass capacitors to be arbitrarily large.

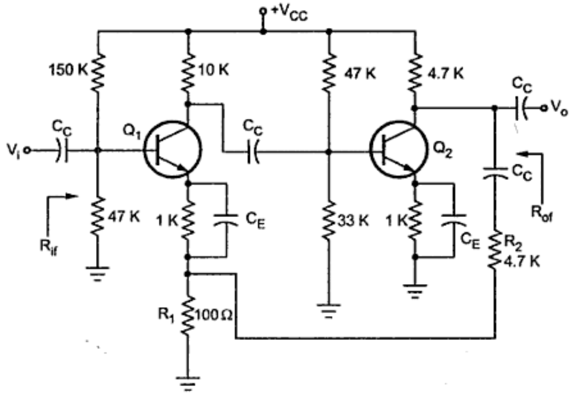

+V_{CC}
150 K
10 K
47 K
4.7 K
C_C
V_o
V_i
C_C
Q_1
C_C
Q_2
C_C
R_{of}
47 K
1 K
C_E
33 K
1 K
C_E
R_2
4.7 K
R_{if}
R_1
100Ω

Fig. 3.44

Solution : **Step 1 : Identify topology.**

The feedback voltage is applied across R_1 (100 Ω), which is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : **Find input and output circuit**

To find input circuit, set $V_o = 0$, which gives parallel combination of R_1 with R_2 at E_1 as shown in the the Fig. 3.45. To find output circuit, set $I_i = 0$ by opening the input node, E_1 at emitter of Q_1, which gives the series combination of R_2 and R_1 across the output. The resultant circuit is shown in Fig. 3.45.

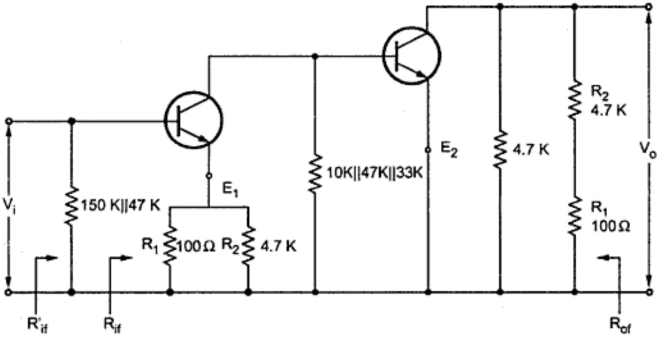

V_i
150 K||47 K
E_1
R_1
100Ω
R_2
4.7 K
10K||47K||33K
E_2
4.7 K
R_2
4.7 K
R_1
100Ω
V_o
R'_{if}
R_{if}
R_{of}

Fig. 3.45

Step 4 : Find the open loop voltage gain (A_V).

$$R_{L2} = 4.7\text{ K} \parallel (4.7\text{ K} + 100\ \Omega)$$

$$= 2.37\text{ K}$$

Since $h_{oe} = h_{re} = 0$ we can use approximate analysis.

$$A_{i2} = -h_{fe} = -50$$

$$R_{i2} = h_{ie} = 1.1\text{ K}$$

$$A_{V2} = \frac{A_{i2}R_{L2}}{R_{i2}} = \frac{-50\times 2.37\times 10^3}{1.1\times 10^3} = -107.73$$

$$R_{L1} = 10\text{ K} \parallel 47\text{ K} \parallel 33\text{ K} \parallel 1.1\text{ K}$$

$$= 942\ \Omega$$

$$A_{i1} = -h_{fe} = -50$$

$$R_{i1} = h_{ie} + (1+h_{fe})\,R_e = 1.1\text{ K} + (1+50)\,(100 \parallel 4.7\text{ K})$$

$$= 6.093\text{ K}$$

$$A_{V1} = \frac{A_{i1}R_{L1}}{R_{i1}} = \frac{-50\times 942}{6.093\times 10^3} = -7.73$$

$$\therefore \quad A_V = A_{V1}\times A_{V2} = (-7.73)\times(-107.73)$$

$$= 832.75$$

Step 5 : Calculate β and D.

$$\beta = \frac{R_1}{R_1+R_2} = \frac{100}{100+4700} = \frac{1}{48}$$

$$D = 1 + A\beta = 1 + \frac{832.75}{48} = 18.35\ \Omega$$

Step 6 : Calculate A_{Vf}, R_{of} and R_{if}.

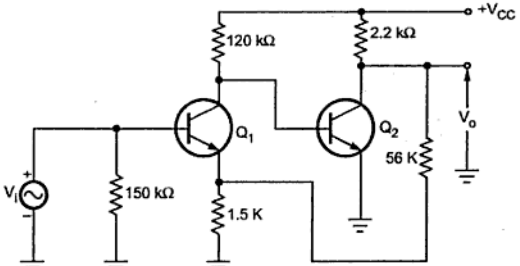
$$A_{Vf} = \frac{A_V}{D} = \frac{832.75}{18.35} = \mathbf{45.38}$$

$$R_{if} = R_{i1}D = 6.093\text{ K}\times 18.35 = \mathbf{111.8\ K}$$

$$R_{of} = \frac{R_o}{D} = \frac{R_{L2}}{D} = \frac{2.37\text{ K}}{18.35}$$

$$= \mathbf{129.15\ \Omega}$$

Example 3.6 : *For feedback amplifier shown in Fig. 3.46, identify the feedback topology with proper justification.*



$+V_{CC}$
120 kΩ
2.2 kΩ
Q_1
Q_2
V_o
56 K
V_i
+
-
150 kΩ
1.5 K

Fig. 3.46

The transistors used are identical with the following parameters :

$h_{fe} = 200$, $h_{ie} = 2\ k\Omega$, $h_{re} = 10^{-4}$, $h_{oe} = 10^{-6}$ A/V

Calculate

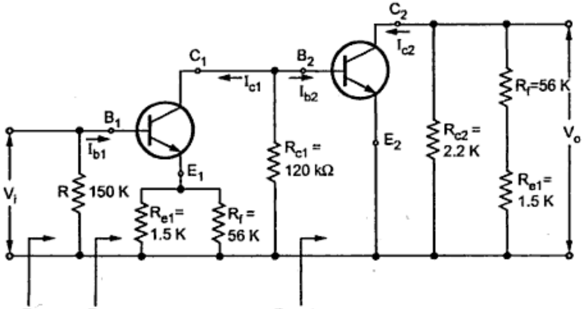
i) A_{Vf} *ii)* R_{if} *iii)* R_{of}

Solution : Step 1 : Identify topology.

The feedback voltage is applied across R_{e1} = 1.5 K, which is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $V_o = 0$, which gives parallel combination of R_{e1} with R_f at E_1 as shown in the Fig. 3.47. To find output circuit, set $I_i = 0$ by opening the input node, E_1 at emitter of Q_1, which gives the series combination of R_f and R_{e1} across the output. The resultant circuit is shown in Fig. 3.47.



C_2
I_{c2}
C_1
B_2
I_{c1}
I_{b2}
B_1
I_{b1}
E_1
E_2
R_{c1} = 120 kΩ
R_{c2} = 2.2 K
R_f=56 K
V_o
R_{e1}= 1.5 K
V_i
R 150 K
R_{e1}= 1.5 K
R_f = 56 K
R_i
R_{i1}
$R_{i2} = h_{ie}$

Fig. 3.47

Step 4 : Find the open loop voltage gain (A_V).

$$R_{L2} = R_{c2} \parallel (R_f + R_{e1})$$
$$= 2.2\text{ K} \parallel (56\text{ K} + 1.5\text{ K})$$
$$= \mathbf{2.119\text{ K}}$$

Since $h_{oe} R_{L2} = 10^{-6} \times 2.119\text{ K} = 0.002119$ is less than 0.1 we use approximate analysis.

$$A_{i2} = -h_{fe} = -200$$
$$R_{i2} = h_{ie} = 2\text{ k}\Omega$$
$$\therefore \quad A_{V2} = \frac{A_{i2} R_{L2}}{R_{i2}} = \frac{-200 \times 2.119\text{ K}}{2\text{ K}}$$
$$= \mathbf{-211.9}$$
$$R_{L1} = R_{C1} \parallel R_{i2} = 120\text{ K} \parallel 2\text{ K}$$
$$= \mathbf{1.967\text{ K}}$$

Since $h_{oe} R_{L1} = 10^{-6} \times 1.967 = 0.001967$ is less than 0.1 we use approximate analysis.

$$A_{i1} = -h_{fe} = -200$$
$$R_{i1} = h_{ie} + (1 + h_{fe}) R_e$$
$$= 2\text{ K} + (1 + 200)(1.5\text{ K} \parallel 56\text{ K})$$
$$= \mathbf{295.63\text{ K}}$$
$$\therefore \quad A_{V1} = \frac{A_{i1} R_{L1}}{R_{i1}} = \frac{-200 \times 1.967\text{ K}}{295.63\text{ K}}$$
$$= \mathbf{-1.33}$$

The overall gain without feedback is

$$A_V = A_{V1} \times A_{V2} = (-1.33) \times (-211.9)$$
$$= \mathbf{281.82}$$

Step 5 : Calculate β

$$\beta = \frac{V_f}{V_o}$$
$$= \frac{1.5\text{ K}}{56\text{ K} + 1.5\text{ K}}$$
$$= \mathbf{0.026}$$

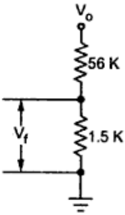


Fig. 3.48

Step 6 : Calculate D, A_{Vf}, R_{if}, R_{of}

$$D = 1+\beta A_V$$

$$= 1 + (0.026) \times 281.82 = 8.327$$

$$\therefore \quad A_{Vf} = \frac{A_V}{D} = \frac{281.82}{8.327}$$

$$= \mathbf{33.84}$$

$$R_i = R_{i1} \parallel R = 295.63\text{ K} \parallel 150\text{ K}$$

$$= \mathbf{99.5\ K}$$

$$\therefore \quad R_{if} = R_i \times D = 99.5 \times 8.327$$

$$= \mathbf{828.53\ K}$$

$$R_o = \frac{1}{h_{oe}} = \frac{1}{10^{-6}}$$

$$= \mathbf{1\ M\Omega}$$

$$R_{of} = \frac{R_o}{D} = \frac{1M}{8.327}$$

$$= \mathbf{120\ K}$$

$$R'_o = R_o \parallel R_{c2} \parallel (R_f + R_{e1}) = R_o \parallel R_{L2}$$

$$= 1\text{ M} \parallel 2.119\text{ K}$$

$$= \mathbf{2.1145\ K}$$

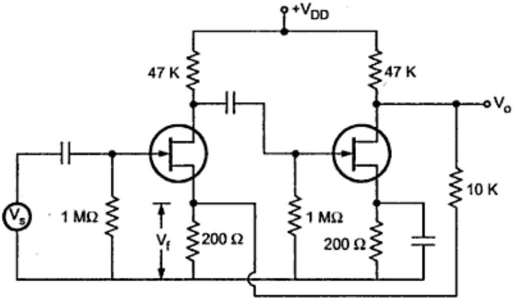
$$R'_{of} = \frac{R'_o}{D} = \frac{2.1145\text{ K}}{8.327}$$

$$= \mathbf{254\ \Omega}$$

Example 3.7 : *The two stage feedback amplifier shown in Fig. 3.49 uses FET. The parameters are* $r_d = 10$ *K and* $\mu = 40$.

i) Identify the topology of feedback.

ii) Calculate D, A_{Vf}, R_{if}, R_{of} *and* R'_{of}.



+V_DD
47 K
47 K
V_o
10 K
V_s
1 MΩ
V_f
200 Ω
1 MΩ
200 Ω

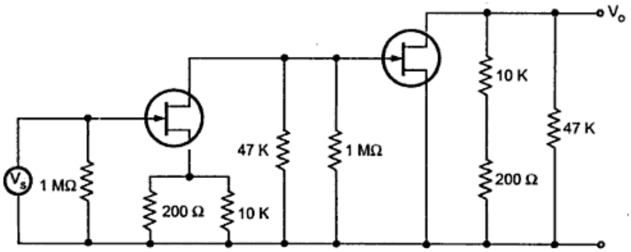
Fig. 3.49

Solution : Step 1 : Identify topology

By shorting output voltage ($V_o = 0$), feedback voltage V_f becomes zero and hence it is voltage sampling. The feedback voltage is applied in series with the input voltage hence the topology is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$. This places the parallel combination of resistors 10 K and 200 Ω at first source. To find output circuit, set $I_i = 0$. This places the resistors 10 K and 200 Ω in series across the output. The resultant circuit is shown in Fig. 3.50.



V_o
10 K
47 K
47 K
1 MΩ
V_s
1 MΩ
200 Ω
200 Ω
10 K

Fig. 3.50

Step 4 : Replace FET with its equivalent circuit.

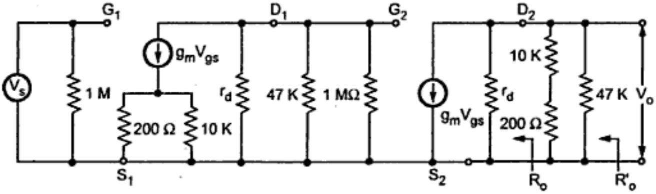


Fig. 3.51

Step 5 : Find open loop transfer gain.

$$A_V = \frac{V_o}{V_s} = A_{V1}\,A_{V2}$$

$$A_{V2} = \frac{-\mu\,R_{L2}}{R_{L2}+r_d}$$

where $R_{L2} = (10\text{ K} + 200\ \Omega) \parallel 47\text{ K}$

$$= 8.38\text{ K}$$

$$\therefore \quad A_{V2} = \frac{-40\times 8.38\times 10^3}{8.38\times 10^3 + 10\times 10^3}$$

$$= -18.237$$

$$A_{V1} = \frac{\mu\,R_{Deff}}{r_d + R_{Deff} + (1+\mu)\,R_{seff}}$$

where $R_{Deff} = R_D \parallel R_{G2} = 47\text{ K} \parallel 1\text{ M}\Omega$

$$= 44.89\text{ k}\Omega$$

$R_{seff} = 200 \parallel 10\text{ K}$

$$A_{V1} = \frac{-40\times 44.98\times 10^3}{10\times 10^3 + 44.89\times 10^3 + (1+40)\,(10\text{ K} \parallel 200)}$$

$$= -28.59$$

$$\therefore \quad \text{Overall } A_V = -28.59\times -18.237$$

$$= 521.39$$

Step 6 : Calculate β.

$$\beta = \frac{V_f}{V_o} = \frac{200}{200+10\times 10^3}$$

$$= 0.0196$$

Step 7 : Calculate D, A_{Vf}, R_{if}, R'_{of}.

$$\begin{aligned}
D &= 1 + \beta A_V \\
&= 1 + 0.0196 \times 521.39 \\
&= 11.22 \\
A_{Vf} &= \frac{A_V}{D} = \frac{521.39}{11.22} = 46.47 \\
R_i &= R_G = 1\ \text{M}\Omega \\
R_{if} &= R_i \times D \\
&= 1 \times 10^6 \times 11.22 \\
&= 11.22\ \text{M}\Omega \\
R_o &= r_d \\
&= 10\ \text{K} \\
R'_o &= r_d \parallel R_{L2} = 10\ \text{K} \parallel 8.38\ \text{K} \\
&= 4.559\ \text{k}\Omega \\
\therefore \quad R'_{of} &= \frac{R'_o}{D} = \frac{4.559 \times 10^3}{11.22} \\
&= 406\ \Omega
\end{aligned}$$

Example 3.8 : *The circuit shows three stage FET amplifier.*

The identical FETs have following parameters.
$r_d = 8\ \text{k}\Omega$, $g_m = 5\ \text{mA/V}$, $R_g = 1\ \text{M}\Omega$,
$R_g = R_1 + R_2$, $R_1 = 50\ \Omega$, $R_d = 40\ \text{k}\Omega$
Calculate voltage gain including feedback.

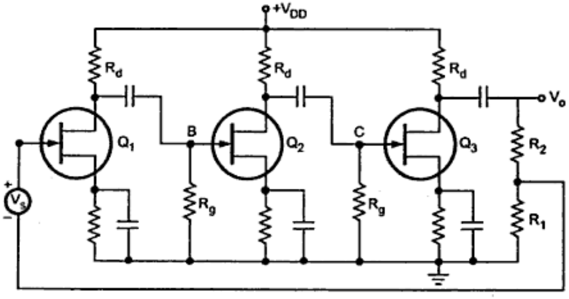


Fig. 3.52

Solution : Here, output voltage is sampled and fed in series with the input signal. Hence the topology is voltage series feedback.

The open loop voltage gain for one stage is given as,

$$A_V = -g_m R_{eq}$$

where

$$R_{eq} = r_d \parallel R_d \parallel (R_{i1} + R_2)$$

$$= 8\ \text{K} \parallel 40\ \text{K} \parallel (1\ \text{M}\Omega)$$

$$= 6.62\ \text{k}\Omega$$

$$A_V = -5 \times 10^3 \times 6.62 \times 10^3$$

$$= -33.11$$

$$A_V = \text{Overall voltage gain} = |A_{V\,mid}|^3 = |-33.11|^3$$

$$= -36306$$

$$\beta = \frac{V_f}{V_o} = \frac{-R_1}{R_g} = \frac{-R_1}{R_1 + R_2} = \frac{50}{1 \times 10^6}$$

$$= -5 \times 10^{-5}$$

$$\therefore \quad D = 1 + \beta\,|A_V| = 1 + (-5 \times 10^{-5}) \times (-36306)$$

$$= 2.815$$

$$\therefore \quad A_{Vf} = \frac{A_V}{D}$$

$$= \frac{-36306}{2.8153} = -12.895 \times 10^3$$

$$\therefore \quad A_{Vf} = -12.895 \times 10^3$$

➡ Example 3.9 : *In the example 3.8, if output is taken between point B and ground, calculate* A_{Vf}.

Solution : Here, output terminals are B and ground, thus the forward gain is the gain of Q_1 and it is,

$$A_{BN} = -33.11$$

However, Q_2 and Q_3 must be considered as a part of feedback loop.

Here

$$\beta_{BN} = \frac{V_f}{V_B} = \frac{V_f}{V_o} \times \frac{V_o}{V_C} \times \frac{V_C}{V_B}$$

where V_B and V_C are voltages at point B and C, respectively.

$$\therefore \qquad \beta_{BN} = \frac{V_f}{V_o} \times A_{V3} \times A_{V2} \qquad \because \frac{V_o}{V_C} = A_{V3} \text{ and } \frac{V_C}{V_B} = A_{V2}$$

$$\therefore \qquad \beta_{BN} = \frac{-R_1}{R_g} \times A_{V3} \times A_{V2} = -5 \times 10^{-5} \times (-33.11) \times (-33.11)$$

$$= -0.0548$$

Note that the loop gain $-\beta_{BN} A_{BN} = A^3_{V_o} \dfrac{R_1}{R_g}$

$$= -1.815 = -\beta A$$

which is the same value as in example 3.8. It should be clear that regardless of where the output terminals are taken, the loop gain is unchanged.

$$\therefore \qquad A_{Vf} = \frac{A_{BN}}{1 + A\beta} = \frac{-33.11}{1 + 1.815} = -11.76$$

➡ **Example 3.10 :** *The two stage FET amplifier shown in the Fig. 3.53 uses identical FETs with $\mu = 50$, $r_d = 10$ K. For this circuit :*

(1) Identify the feedback topology.

(2) Draw the circuit diagram of basic amplifier without feedback.

(3) Calculate A_{Vf}, R_{if} and R_{of}

Assume all capacitors to be large enough so as to act as short circuit at the lowest frequency of interest.

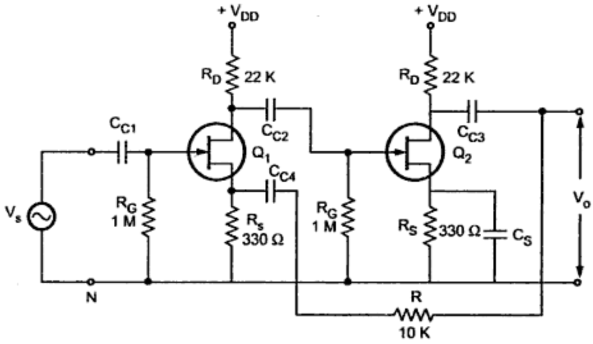


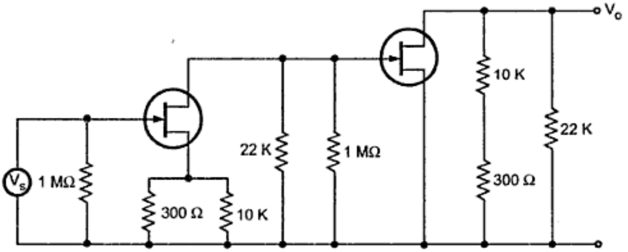
Fig. 3.53

Solution : Step 1 : Identify topology.

By shorting output voltage ($V_o = 0$), feedback voltage V_f becomes zero and hence it is voltage sampling. The feedback voltage is applied in series with the input voltage hence the topology is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit.

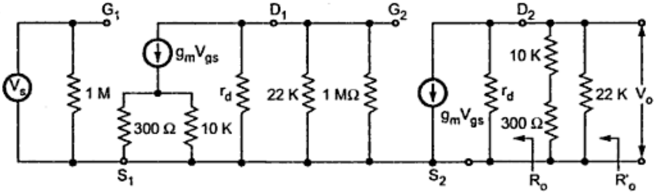
To find input circuit, set $V_o = 0$. This places the parallel combination of resistors 10 K and 300 Ω at first source. To find output circuit, set $I_i = 0$. This places the resistors 10 K and 300 Ω in series across the output. The resultant circuit is shown in Fig. 3.54.



V_o
10 K
22 K
22 K
1 MΩ
300 Ω
V_s
1 MΩ
300 Ω
10 K

Fig. 3.54

Step 4 : Replace FET with its equivalent circuit.



G_1
D_1
G_2
D_2
g_mV_{gs}
V_s
1 M
r_d
22 K
1 MΩ
300 Ω
10 K
S_1
g_mV_{gs}
r_d
10 K
300 Ω
22 K
V_o
S_2
R_o
R'_o

Fig. 3.55

Step 5 : Find open loop transfer gain.

$$A_V = \frac{V_o}{V_s} = A_{V1}\,A_{V2}$$

$$A_{V2} = \frac{-\mu\,R_{L2}}{R_{L2}+r_d}$$

where

$$R_{L2} = (10\text{ K} + 300\ \Omega) \parallel 22\text{ K}$$

$$= 7\text{ k}\Omega$$

$$A_{V2} = \frac{-50 \times 7 \times 10^3}{7 \times 10^3 + 10 \times 10^3}$$

$$= -20.59$$

$$A_{V1} = \frac{\mu R_{Deff}}{r_d + R_{Deff} + (1+\mu)R_{seff}}$$

where $R_{Deff} = R_D || R_{G2} = 22\text{ K} || 1\text{ M}\Omega$

$$= 21.53\text{ k}\Omega$$

$$R_{seff} = 330 || 10\text{ K}$$

$$\therefore \quad A_{V1} = \frac{-50 \times 21.53 \times 10^3}{10 \times 10^3 + 21.53 \times 10^3 + (1+50)(330 \; || \; 10\text{ K})}$$

$$= -22.51$$

$$\therefore \quad \text{Overall } A_V = A_{V1} \times A_{V2}$$

$$= -20.59 \times (-22.51)$$

$$= 463.5$$

Step 6 : Calculate β

$$\beta = \frac{V_f}{V_o} = \frac{R_s}{R_s + R_f} = \frac{330}{330 + 10000}$$

$$= 0.0319$$

Step 7 : Calculate D, A_{Vf}, R_{if}, R'_{of}.

$$D = 1 + \beta A_V$$

$$= 1 + 0.0319 \times 463.5$$

$$= 15.786$$

$$A_{Vf} = \frac{A_V}{D} = \frac{463.5}{15.785} = 29.36$$

$$R_i = R_G = 1\text{ M}\Omega$$

$$R_{if} = R_i \times D = 1 \times 10^6 \times 15.785$$

$$= 15.785\text{ M}\Omega$$

$$R'_o = r_d \; || \; R_{L2} = 10\text{ K} || 7\text{ K}$$

$$= 4.118\text{ k}\Omega$$

$$R'_{of} = \frac{R'_o}{D} = \frac{4.118 \times 10^3}{15.785} = 261\ \Omega$$

➡ **Example 3.11 :** *For the circuit shown in the Fig. 3.56, determine closed loop voltage gain, input resistance with feedback and output resistance with feedback. Assume ideal input voltage source. The BJTs used are identical with h_{fe} = 50 and h_{ie} = 1 K. Assume $h_{oe} = h_{re} = 0$. Assume all capacitors to be arbitrarily large.*

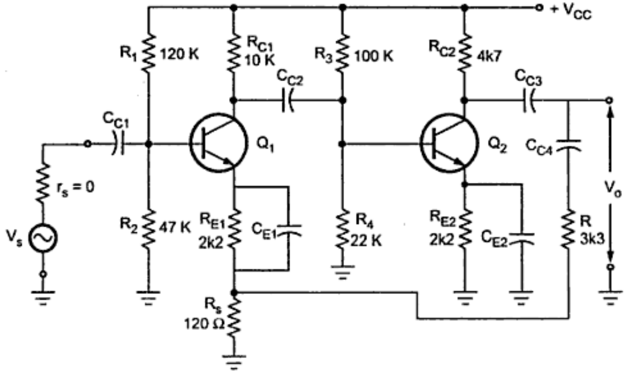

+ V_{CC}
R_1 120 K
R_{C1} 10 K
R_3 100 K
R_{C2} 4k7
C_{C2}
C_{C3}
C_{C1}
Q_1
Q_2
C_{C4}
$r_s = 0$
V_o
V_s
R_2 47 K
R_{E1} 2k2
C_{E1}
R_4 22 K
R_{E2} 2k2
C_{E2}
R 3k3
R_s 120 Ω

Fig. 3.56

Solution : Step 1 : Identify topology.

The feedback voltage is applied across the resistance R_{e1} and it is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$ (connecting C_2 to ground), which gives parallel combination of R_e with R_f at E_1. To find output circuit, set $I_i = 0$ (opening the input node E_1 at emitter of Q_1), which gives series combination of R_f and R_{e1} across the output. The resultant circuit is shown in Fig. 3.57.

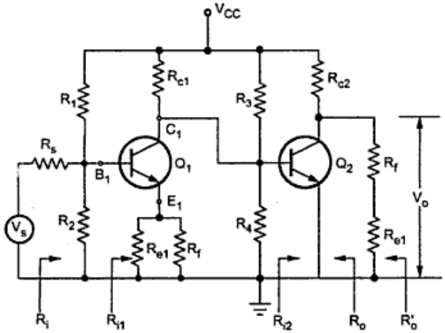

V_{CC}
R_{c1}
R_{c2}
R_1
R_3
C_1
R_s
Q_1
Q_2
R_f
B_1
E_1
V_o
V_s
R_2
R_4
R_{e1}
R_f
R_{e1}
R_i
R_{i1}
R_{i2}
R_o
R'_o

Fig. 3.57

Step 4 : Find open loop voltage gain (A_V).

$$R_{L2} = R_{c2} \parallel (R_s + R)$$

$$= 4.7\text{ K} \parallel (120 + 3.3\text{ K})$$

$$= 1.98\text{ k}\Omega$$

$$A_{i2} = -h_{fe} = -50$$

$$R_{i2} = h_{ie} = 1000\Omega = 1\text{ K}$$

$$A_{V2} = \frac{A_{i2} R_{L2}}{R_{i2}} = \frac{-50 \times 1.98\text{ K}}{1\text{ K}}$$

$$= -99$$

$$A_{i1} = -h_{fe} = -50$$

$$R_{L1} = R_{c1} \parallel R_3 \parallel R_4 \parallel R_{i2}$$

$$= 10\text{ K} \parallel 100\text{ K} \parallel 22\text{ K} \parallel 1\text{ K}$$

$$= 865.46\ \Omega$$

$$R_{i1} = h_{ie} + (1 + h_{fe}) R_{e1eff}$$

where $R_{e1\,eff} = R_s \parallel R$

$$= 1000 + (1 + 50)\ (120 \parallel 3.3\text{ K})$$

$$= 6.9\text{ k}\Omega$$

$$A_{V1} = \frac{A_{i1} R_{L1}}{R_{i1}} = \frac{-50 \times 865.46}{6900}$$

$$= -6.27$$

The overall voltage gain,

$$A_V = A_{V1} \times A_{V2}$$

$$= -6.27 \times (-99)$$

$$= 620.73$$

Step 5 : Calculate β.

$$\beta = \frac{V_f}{V_o} = \frac{R_s}{R_s + R}$$

$$= \frac{120}{120 + 3300} = 0.035$$

Step 6 : Calculate D, A_{Vf}, R_{if}, R_{of} and R'_{of}.

$$D = 1+\beta A_V = 1+0.035\times 620.73 = 22.725$$

$$A_{Vf} = \frac{A_V}{D} = \frac{620.73}{22.725} = 27.3$$

$$R_{if} = R_{i1}D = 6.9\text{ K}\times 22.725$$

$$= 156.8\text{ k}\Omega$$

$$R_{of} = \frac{R_o}{D} = \frac{\infty}{D} = \infty$$

$$R'_{of} = \frac{R'_o}{D} = \frac{R_{L2}}{D} = \frac{1.98\text{ K}}{22.725}$$

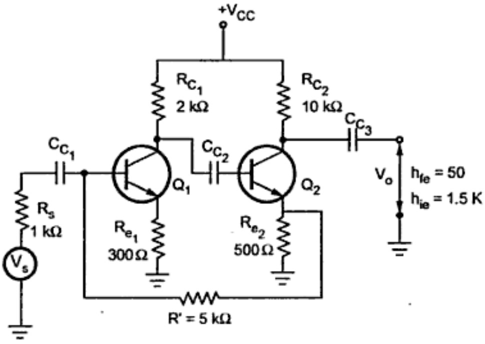
$$= 87.12\ \Omega$$

Example 3.12 : *For the circuit shown in Fig. 3.58.*

i) Identify the topology of feedback.

ii) Draw equivalent circuit diagram.

iii) Determine values of A_I, β and A_{If}.



+V_{CC}
R_{C_1}
2 kΩ
R_{C_2}
10 kΩ
C_{C_3}
C_{C_1}
C_{C_2}
Q_1
Q_2
V_o
h_{fe} = 50
h_{ie} = 1.5 K
R_s
1 kΩ
V_s
R_{e_1}
300 Ω
R_{e_2}
500 Ω
R' = 5 kΩ

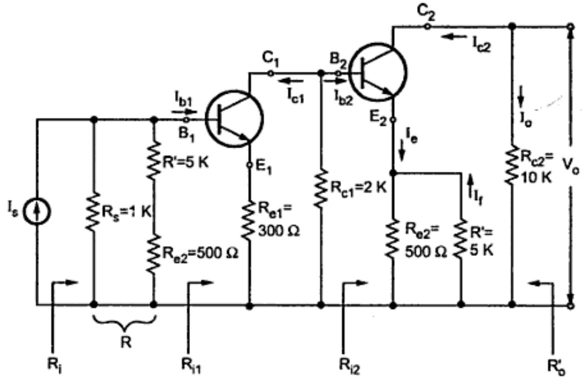
Fig. 3.58

Solution : Step 1 : Identify topology.

The feedback is given from emitter of Q_2 to the base of Q_2. If $I_o = 0$ then feedback current through 5 K register is zero, hence it is current sampling. As feedback signal is mixed in shunt with input, the amplifier is current shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

The input circuit of the amplifier without feedback is obtained by opening the output loop at the emitter of Q_2 ($I_o = 0$). This places R′ (5 K) in series with R_e from base to emitter of Q_1. The output circuit is found by shorting the input node, i.e. making $V_i = 0$. This places R′ (5 K) in parallel with R_e. The resultant equivalent circuit is shown in Fig. 3.59.



C2
Ic2
C1
B2
Ib1
Ic1
Ib2
B1
E2
Ie
Io
R'=5 K
E1
Rc2= 10 K
Vo
Rc1=2 K
If
Is
Rs=1 K
Re1= 300 Ω
Re2= 500 Ω
R'= 5 K
Re2=500 Ω
R
Ri
Ri1
Ri2
R'o

Fig. 3.59

Step 4 : Find open circuit transfer gain.

$$A_I = \frac{I_o}{I_s} = \frac{-I_c}{I_s} = \frac{-I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

We know that $\frac{-I_{c2}}{I_{b2}} = A_{i2} = -h_{fe} = -50$ and

$$\frac{-I_{c1}}{I_{b1}} = A_{i1} = -h_{fe} = 50$$

$$\therefore \quad \frac{I_{c1}}{I_{b1}} = 50$$

Looking at Fig. 3.59 we can write,

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}}$$

where

$$\begin{aligned} R_{i2} &= h_{ie} + (1 + h_{fe}) (R_{e2} \parallel R') \\ &= 1.5\text{ K} + (1 + 50) (500 \parallel 5\text{ K}) \\ &= 24.6818\text{ k}\Omega \end{aligned}$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-2\times10^3}{2\times10^3+24.6818\times10^3} = \mathbf{-0.07495}$$

$$\frac{I_{b1}}{I_s} = \frac{R}{R+R_{i1}} \quad \text{where } R = R_s || (R'+R_{e2})$$

$$\therefore \quad R = (1\times10^3) \, || \, (5\times10^3+500) = \mathbf{846.1538 \ \Omega}$$

and $$R_{i1} = h_{ie}+(1+h_{fe})\,R_{e1} = 16.8 \text{ k}\Omega$$

$$\therefore \quad \frac{I_{b1}}{I_s} = \frac{846.1538}{846.1538+16.8\times10^3} = 0.04795$$

$$\therefore \quad A_I = (-50)\times(0.07495)\times(50)\,(0.04795) = \mathbf{8.9848}$$

Step 5 : Calculate β.

$$\beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2}+R'} = \frac{500}{500+5\times10^3} = \mathbf{0.0909}$$

Step 6 : Calculate D, A_{If}.

$$D = 1+\beta A_I = 1+(0.0909)\,(8.9848) = \mathbf{1.8168}$$

$$\therefore \quad A_{If} = \frac{A_I}{D} = \frac{8.9848}{1.8168} = \mathbf{4.9453}$$

Example 3.13 : *For a given amplifier in Fig. 3.60 write the type of topology and calculate the values of* β, A_V, A_{Vf}, R_{if}, R_{of} *and* R'_{of}. *h-parameters of identical two transistors are* $h_{ie} = 1100\ \Omega$, $h_{fe} = 500$, $h_{oe} = h_{re} = 0$.

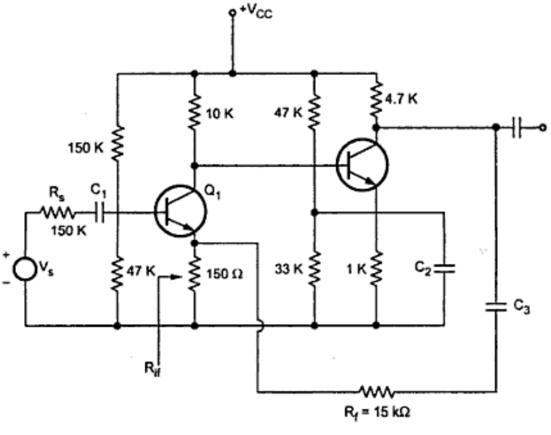


Fig. 3.60

Solution : Step 1 : Identify topology.

The feedback voltage is applied across R_1 (150 Ω), which is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$, which gives parallel combination of R_1 with R_2 at E_1 as shown in the the Fig. 3.61. To find output circuit, set $I_i = 0$ by opening the input node, E_1 at emitter of Q_1, which gives the series combination of R_2 and R_1 across the output. The resultant circuit is shown in Fig. 3.61.

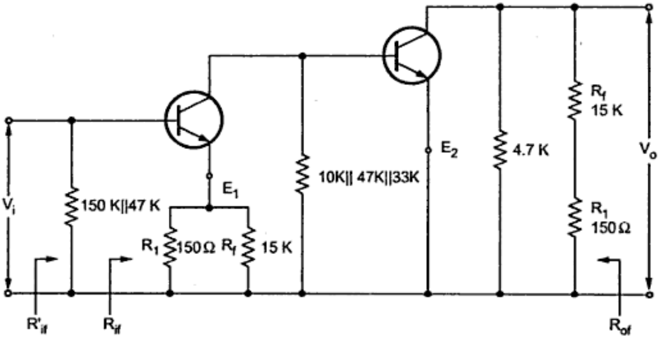


Fig. 3.61

Step 4 : Find the open loop voltage gain (A_V).

$$R_{L2} = 4.7\text{ K} \parallel (15\text{ K} + 150)$$

$$= 3.59\text{ k}\Omega$$

Since $h_{oe} = h_{re} = 0$, we can use approximate analysis.

$$A_{i2} = -h_{fe} = -500$$

$$R_{i2} = h_{ie} = 1100\Omega$$

$$A_{V2} = \frac{A_{i2}R_{L2}}{R_{i2}} = \frac{-500 \times 3.59 \times 10^3}{1100} = -1632$$

$$R_{L1} = 10\text{ K} \parallel 47\text{ K} \parallel 33\text{ K} \parallel R_{i2}$$

$$= 10\text{ K} \parallel 47\text{ K} \parallel 33\text{ K} \parallel 1100$$

$$= 942\ \Omega$$

$$A_{i1} = -h_{fe} = -500$$

$$R_{i1} = h_{ie} + (1+h_{fe})\,R_e = 1100 + (1+500)\,(150 \,||\, 15\text{ K})$$

$$= 75.5\text{ k}\Omega$$

$$A_{V1} = \frac{A_{i1}R_{L1}}{R_{i1}} = \frac{-500\times 942}{75.5\times 10^3} = -6.238$$

$$A_V = A_{V1}\times A_{V2} = (-6.238)\times(-1632)$$

$$= 10180$$

Step 5 : Calculate β and D.

$$\beta = \frac{R_1}{R_1+R_2} = \frac{150}{150+15000} = 0.0099$$

$$D = 1 + A\,\beta = 1 + 10180 \times 0.0099$$

$$= 101.782$$

Step 6 : Calculate A_{Vf}, R_{of} and R_{if}.

$$A_{Vf} = \frac{A_V}{D} = \frac{10180}{101.782} \simeq 100$$

$$R_{if} = R_{i1}D = 75.5\times 10^3 \times 101.782$$

$$= 7.684\text{ M}\Omega$$

$$R_{of} = \frac{R_o}{D} = \frac{R_{L2}}{D} = \frac{3.59\times 10^3}{101.782} = 35.27\,\Omega$$

➠ **Example 3.14 :** *An RC coupled amplifier has a mid frequency gain 500 and lower and upper 3 dB frequencies of 100 Hz and 20 kHz. A negative feedback with β = 0.01 is incorporated into amplifier circuit.*

Calculate :

i) Gain with feedback.

ii) New bandwidth.

Solution : **Given :** $A_{V\,mid} = 500$, $f_L = 100$ Hz, $f_H = 20$ kHz and $\beta = 0.01$

$$A_{Vf} = \frac{A_{V\,mid}}{1+\beta A_{Vmid}} = \frac{500}{1+0.01\times 500} = 83.33$$

$$f_{Lf} = \frac{f_L}{1+\beta A_{Vmid}} = \frac{100}{1+0.01\times 500} = 16.67\text{ Hz}$$

$$f_{Hf} = f_H \times (1+\beta A_{Vmid})$$

$$= 20\times 10^{3}\ (1+0.01\times 500)$$

$$= 120\text{ kHz}$$

$$BW_f = f_{Hf} - f_{Lf} = 120\text{ kHz} - 16.67\text{ Hz}$$

$$= 119.9833\text{ kHz}$$

Example 3.15 : *For the circuit shown in Fig. 3.62.*

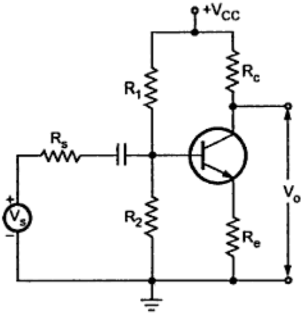


Fig. 3.62

i) Identify topology used in feedback amplifier

ii) Show that voltage gain with feedback

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-h_{fe}R_c\left(\dfrac{1}{1+\dfrac{R_s}{R_b}}\right)}{R_s' + h_{ie} + (1+h_{fe})R_e}$$

where $R_s' = R_s \parallel R_1 \parallel R_2$

Solution : Step 1 : Identify topology.

By shorting output ($V_o = 0$), feedback voltage does not become zero. By opening the output loop feedback becomes zero and hence it is current sampling. The feedback is applied in series with the input signal, hence topology used is current series feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $I_o = 0$. This places R_e in series with input. To find output circuit $I_i = 0$. This places R_e in the output side. The resultant circuit is shown in Fig. 3.63.

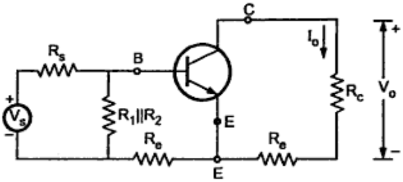

C
B
E
E
R_s
$R_1||R_2$
R_e
R_e
R_c
I_o
V_s
V_o
+
–
+
–

Fig. 3.63

Step 4 : Replace transistor with its h-parameter equivalent.

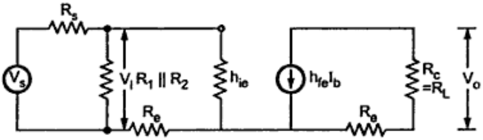

R_s
V_s
V_i
$R_1 \parallel R_2$
R_e
h_{ie}
$h_{fe}I_b$
R_e
R_c
$=R_L$
V_o

Fig. 3.64

Step 5 : Find open loop transfer gain.

From equation (5) of section 3.9.1 we have

$$A_{Vf} = \frac{I_o R_L}{V_s} = G_{Mf} R_L$$

$$= \frac{-h_{fe} R_L}{R_s' + h_{ie} + (1+h_{fe})R_e}$$

Here $$R_s' = R_s \parallel R_1 \parallel R_2$$

$$= R_s \parallel R_b \qquad \because R_b = R_1 \parallel R_2$$

$\therefore$ $$\frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

where $$\frac{V_i}{V_s} = \frac{R_b}{R_s + R_b}$$

$\therefore$ $$\frac{V_o}{V_s} = \frac{-h_{fe} R_L}{R_s' + h_{ie} + (1+h_{fe})R_e} \times \frac{R_b}{R_s + R_b}$$

Dividing both numerator and denominator by $R_s + R_b$ we get,

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-h_{fe} R_c \times \dfrac{R_b}{R_b + R_s}}{R_s' + h_{ie} + (1+h_{fe})R_e} \quad \because R_L = R_c$$

$$= \frac{-h_{fe}R_c\left(\frac{1}{1+\frac{R_s}{R_b}}\right)}{R_s'+h_{ie}+(1+h_{fe})R_e}$$

Example 3.16 : *For the BJT amplifier shown in the Fig. 3.65, calculate its* G_{Mf}, R_{if}, R_{of}.

For the BJT, assume $h_{ie} = 1\ K$, $h_{fe} = 50$, $h_{re} = h_{oe} = 0$.

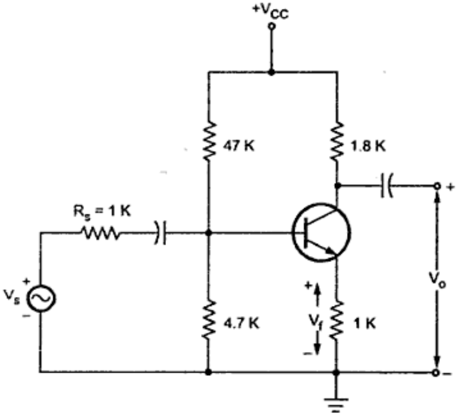


Fig. 3.65

Solution : Refer example 3.15.

$$A_{Vf} = \frac{-h_{fe}R_c\left(\frac{1}{1+\frac{R_s}{R_b}}\right)}{R_s'+h_{ie}+\left(1+h_{fe}\right)R_e} \quad \text{where } R_s' = R_s||R_1||R_2$$

$$= 1\ K||47\ K||4.7\ K = 810\ \Omega$$

$$= \frac{-50\times1.8\times10^3\left(\frac{1}{1+\frac{1000}{4272}}\right)}{810+1000+(1+50)\times1000} = \frac{-72928.679}{52810} = -\mathbf{1.38}$$

$$G_{Mf} = \frac{A_{Vf}}{R_L} = \frac{-1.38}{1.8\times10^3} = -7.66 \times 10^{-4}$$

$$\beta = \frac{V_f}{I_o} = \frac{I_e R_e}{I_o} = \frac{-I_o R_e}{I_o} = -R_e = -1 \text{ K}$$

$$G_{Mf} = \frac{G_M}{1+\beta G_M}$$

$$-7.66\times10^{-4} = \frac{G_M}{1+(-1000)G_M}$$

$$\therefore \quad G_M = -3.2735 \times 10^{-3}$$

$$D = 1+\beta G_M = 1+(-1000)(-3.2735\times10^{-3})$$

$$= 4.2735$$

$$R_i = R_s + (h_{ie}+R_e) \parallel R_D = 1\text{ K}+(1\text{ K}+1\text{ K})\parallel(47\text{ K}\parallel 4.7\text{ K})$$

$$= 1\text{ K} + 1.36\text{ K} = 2.36\text{ K}$$

$$R_{if} = R_i D = 2.36\text{ K} \times 4.2735 = 10\text{ K}$$

$$R_o = \infty$$

$$R_{of} = R_o D = \infty$$

$$R'_{of} = R_{of} \parallel R_L = R_L$$

$$= 1.8\text{ k}\Omega$$

Example 3.17 : *Identify the topology and find the transfer gains (both with and without considering R_s), feedback factor, R_{if} and R_{of} of the circuit given below. Assume $h_{ie} = 1$ kΩ, $h_{fe} = 150$, $h_{re} = h_{oe} = 0$.*

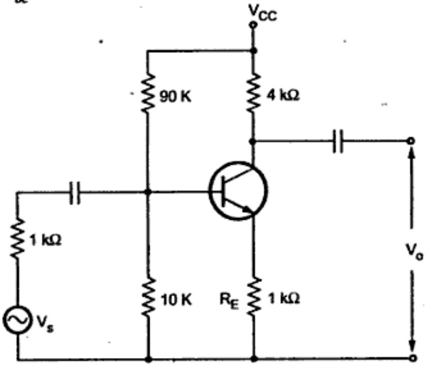


Fig. 3.66

Solution : Refer example 3.15.

$$A_{Vf} = \frac{-h_{fe}R_c\left[\frac{1}{1+\frac{R_s}{R_b}}\right]}{R'_s+h_{ie}+(1+h_{fe})R_e} \quad \text{where } R'_s = R_s \parallel R_1 \parallel R_2$$

$$= 1\text{ K} \parallel 90\text{ K} \parallel 10\text{ K} = \mathbf{900\ \Omega}$$

$$= \frac{-50\times4\times10^3\left[\frac{1}{1+\frac{1000}{9000}}\right]}{900+1000+(1+150)\times1000}$$

$$= -1.177$$

$$G_{Mf} = \frac{A_{Vf}}{R_L} = \frac{-1.177}{4\times10^3} = \mathbf{-2.943\times10^{-4}}$$

$$\beta = \frac{V_f}{I_o} = \frac{I_eR_e}{I_o} = \frac{-I_oR_e}{I_o} = -R_e = \mathbf{-1\ K}$$

$$G_{Mf} = \frac{G_M}{1+\beta G_M}$$

$$\therefore \quad -2.943\times10^{-4} = \frac{G_M}{1+(-1000)\,G_M}$$

$$\therefore \quad G_M = \mathbf{-4.17\times10^{-4}}$$

$$D = 1+\beta G_M = 1+(-1000)(-4.17\times10^{-4})$$

$$= \mathbf{1.417}$$

$$R_i = R_s+(h_{ie}+R_e)\,||\,R_B = 1\text{ K}+(1000+1000)\parallel 9\text{ K}$$

$$= \mathbf{2.636\ k\Omega}$$

$$R_{if} = R_iD = 2.636\text{ K}\times1.417 = \mathbf{3.735\ k\Omega}$$

$$R_o = \infty$$

$$R_{of} = R_o\,D = \infty$$

$$R'_{of} = R_{of}\,||\,R_L = R_L$$

$$= \mathbf{4\ k\Omega}$$

➠ **Example 3.18 :** *An RC coupled amplifier has mid frequency gain 400 and lower and upper 3 dB frequencies 100 Hz and 15 kHz respectively. A negative feedback with $\beta = 0.01$ is incorporated into amplifier circuit. Calculate gain with feedback and new bandwidth.*

Solution : Given : $A_{V\,mid} = 400$, $f_L = 100$ Hz, $f_H = 15$ kHz and $\beta = 0.01$

$$A_{Vf} = \frac{A_{V\,mid}}{1+\beta A_{V\,mid}} = \frac{400}{1+0.01\times 400} = 80$$

$$f_{Lf} = \frac{f_L}{1+\beta A_{V\,mid}} = \frac{100}{1+0.01\times 400} = 20$$

$$f_{Hf} = f_H \times (1+\beta A_{Vmid}) = 15 \times 10^3 \times (1 + 0.01 \times 400)$$

$$= \mathbf{75\ kHz}$$

$$BW_f = f_{Hf} - f_{Lf} = 75 \times 10^3 - 20$$

$$= \mathbf{74.98\ kHz}$$

➠ **Example 3.19 :** *A single stage amplifier has a voltage gain of 10 and bandwidth 1 MHz. Three such stages are cascaded and negative feedback of 10 % is applied to cascade stage. Find overall voltage gain and bandwidth of cascade stage.*

Solution : Given : $A_V = 10$, $BW = 1 \times 10^6$, $n = 3$

i) Overall voltage gain

The gain of cascaded amplifier without feedback

$$= 10 \times 10 \times 10 = 1000$$

$$A_{Vf} = \frac{A_V}{1+\beta A_V} = \frac{1000}{1+0.1\times 1000} = 9.9$$

ii) Bandwidth of cascaded stage

Bandwidth of cascaded amplifier without feedback

$$BW(\text{cascade}) = BW\sqrt{2^{1/n}-1}$$

$$= 1 \times 10^6 \sqrt{2^{1/3}-1} = 509.82\text{ kHz}$$

$$BW_f = BW \times (1 + \beta A_{V\,mid})$$

$$= 509.82 \times 10^3 \times (1 + 0.1 \times 1000)$$

$$= \mathbf{51.49\ MHz}$$

Review Questions

1. *What is positive feedback ?*
2. *What is negative feedback ?*
3. *What do you mean by voltage amplifier and current amplifier ? Give their equivalent circuit.*
4. *With the help of general block diagram explain the term feedback.*
5. *Define the following terms in connection with feedback.*
   (i) Return difference feedback (ii) Closed loop voltage gain (iii) Open loop voltage gain
6. *What are the different types of feed back amplifiers. Give their equivalent circuits.*
7. *Give topology for various types of feedback amplifiers.*
8. *Explain the sampling and mixing networks.*
9. *Classify various feedback amplifiers.*
10. *Define the feedback factor* β.
11. *Show various ways of introducing negative feedback in amplifiers.*
12. *Show that for current series feedback amplifier input and output resistances are increased by a factor* $(1 + A\beta)$ *with feedback.*
13. *Show that for voltage shunt feedback amplifier transresistance gain,* R_1 *and* R_0 *are decreased by a factor* $(1 + A\beta)$ *with feedback.*
14. *Draw the block schematic of amplifier with negative feedback.*
    Explain the consequences of introducing negative feedback in small signal amplifier.
15. *Classify the amplifier based on feedback topology and give their block diagrams. How the input and output impedances are effected in each case.*
16. *Draw the circuit diagram of a current series feedback circuit and derive expressions for voltage gain and output resistance, and input resistance.*
17. *State the transfer gain of each configuration and define feedback factor.*
18. *Draw the circuit diagram of voltage series feedback and derive expressions for input resistance and output resistance.*
19. *Draw the circuit diagram of a voltage shunt feedback using BJT and derive expression for voltage gain with feedback.*
20. *How the negative feedback effect on input and output resistances. Justify your statement with required derivations.*
21. *How do you classify feed back amplifier and what are they. Can you say that the feedback effects on bandwidth of an amplifier-justify your answer.*
22. *Briefly discuss about the effect of feedback on amplifier band width.*
23. *Define desensitivity D ? For large values of D what is* A_f *? What is the significance of this result?*
24. *What is the effect of employing negative feedback on voltage and current gains of practical voltage amplifier ? Derive the relevant relationships.*

25. *Draw the circuit for current shunt amplifier and justify the type of feedback. Derive the expression for* A_V, β, R_i *and* R_o *for the circuit.*
26. *Explain the concept of feedback as applied to electronic amplifier circuits. What are the advantages and disadvantages of positive and negative feedback.*
27. *Compare various feedback amplifiers with different topologies.*
28. *What are the advantages and disadvantages of negative feedback.*
29. *Draw the frequency response of an amplifier without and with feedback and show the band width for each case and how these two curves are related to gain bandwidth product.*
30. *For the circuit shown in Fig. 3.67,* $A = A_V = -1000$, $B = V_f/V_o = 1/100$, $R_s = R_c = R_e = 1 k\Omega$, $h_{ie} = 1\ k\Omega$, $h_{fe} = 100$ *and* h_{re}, h_{oe} *are negligible.*

    Find i) V_i *as a function of* V_s *and* V_f *(Assume that the inverting amplifier input resistance is infinite), ii)* $A_{Vf} = V_o/V_s = A.\ V_i/V_s$.

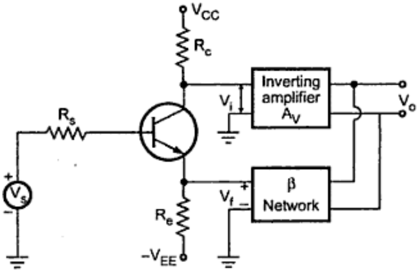


Fig. 3.67

4

Oscillators

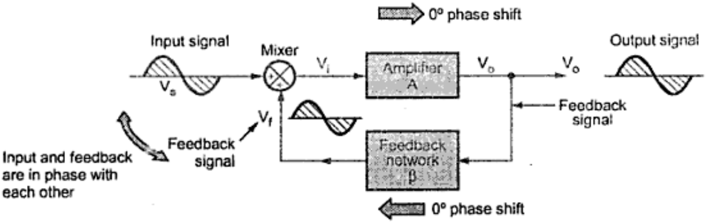
4.1 Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal, and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are out of phase, the feedback is called **negative feedback.**

The positive feedback results into oscillations and hence used in electronic circuits to generate the oscillations of desired frequency. Such circuits are called oscillators.

4.2 Concept of Positive Feedback

The feedback is a property which allows to feedback the part of the output, to the same circuit as its input. Such a feedback is said to be positive whenever the part of the output that is fed back to the amplifier as its input, is in phase with the original input signal applied to the amplifier. Consider a non-inverting amplifier with the voltage gain A as shown in the Fig. 4.1.



0° phase shift
Input signal
Mixer
V_i
Amplifier A
V_o
V_o
Output signal
V_s
Feedback signal
V_f
Feedback signal
Input and feedback are in phase with each other
Feedback network β
0° phase shift

Fig. 4.1 Concept of positive feedback

Assume that a sinusoidal input signal (voltage) V_s is applied to the circuit. As amplifier is non-inverting, the output voltage V_o is in phase with the input signal V_s. The part of the output is fed back to the input with the help of a feedback network. How much part of the output is to be fed back, gets decided by the feedback network gain β. No phase change is introduced by the feedback network. Hence the feedback voltage V_f is in phase with the input signal V_s.

Key Point: *As the phase of the feedback signal is same as that of the input applied, the feedback is called positive feedback.*

4.2.1 Expression for Gain with Feedback

The amplifier gain is A i.e. it amplifies its input V_i, A times to produce output V_o.

$$\therefore \qquad \boxed{A = \frac{V_o}{V_i}}$$

This is called **open loop gain** of the amplifier.

For the overall circuit, the input is supply voltage V_s and net output is V_o. The ratio of output V_o to input V_s considering effect of feedback is called **closed loop gain** of the circuit or **gain with feedback** denoted as A_f.

$$\therefore \qquad \boxed{A_f = \frac{V_o}{V_s}}$$

The feedback is positive and voltage V_f is added to V_s to generate input of amplifier V_i. So referring Fig. 4.1 we can write,

$$\boxed{V_i = V_s + V_f} \qquad ...(1)$$

The feedback voltage V_f depends on the feedback element gain β. So we can write,

$$\boxed{V_f = \beta V_o} \qquad ...(2)$$

Substituting (2) in (1),

$$V_i = V_s + \beta V_o$$

$$\therefore \qquad V_s = V_i - \beta V_o \qquad ... (3)$$

Substituting in expression for A_f,

$$A_f = \frac{V_o}{V_i - \beta V_o}$$

Dividing both numerator and denominator by V_i,

$$\therefore \qquad A_f = \frac{(V_o / V_i)}{1-\beta(V_o / V_i)}$$

$$\therefore \qquad \boxed{A_f = \frac{A}{1-A\beta}} \qquad \ldots \text{ as } A = \frac{V_o}{V_i}$$

Now consider the various values of β and the corresponding values of A_f for constant amplifier gain of A = 20.

A	β	A_f
20	0.005	22.22
20	0.04	100
20	0.045	200
20	0.05	∞

Table 4.1

Conclusions :

The above result shows that the gain with feedback increases as the amount of positive feedback increases. In the limiting case, the gain becomes infinite. This indicates that circuit can produce output without external input ($V_s = 0$), just by feeding the part of the output as its own input. Similarly, output cannot be infinite but gets driven into the oscillations. In other words, the circuit stops amplifying and starts oscillating.

Key Point: *Thus without an input, the output will continue to oscillate whose frequency depends upon the feedback network or the amplifier or both. Such a circuit is called as an* ***oscillator****.*

It must be noted that β the feedback network gain is always a fraction and hence $\beta < 1$. So the feedback network is an attenuation network. To start with the oscillations $A\beta > 1$ but the circuit adjusts itself to get $A\beta = 1$, when it produces sinusoidal oscillations while working as an oscillator.

An oscillator is an amplifier, which uses a positive feedback and without any external input signal, generates an output waveform, at a desired frequency.

An oscillator is a circuit which basically acts as a generator, generating the output signal which oscillates with constant amplitude and constant desired frequency. An oscillator does not require any input signal. An electrical device, alternator generates a sinusoidal voltage at a desired frequency of 50 Hz in our nation but electronic oscillator can generate a voltage of any desired waveform at any frequency. An oscillator can generate the output waveform of high frequency upto gigahertz.

4.3 Barkhausen Criterion

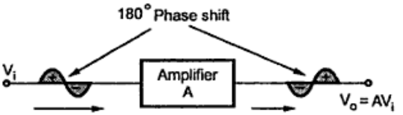

180° Phase shift
V_i
Amplifier A
$V_o = AV_i$

Fig. 4.2 Inverting amplifier

Consider a basic inverting amplifier with an open loop gain A. The feedback network attenuation factor β is less than unity. As basic amplifier is inverting, it produces a phase shift of 180° between input and output as shown in the Fig. 4.2.

Now the input V_i applied to the amplifier is to be derived from its output V_o using feedback network.

But the feedback must be positive i.e. the voltage derived from output using feedback network must be in phase with V_i. Thus the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input. This ensures positive feedback.

The arrangement is shown in the Fig. 4.3.

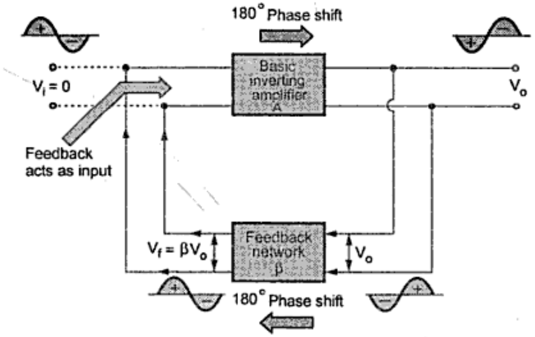

180° Phase shift
$V_i = 0$
Basic inverting amplifier A
V_o
Feedback acts as input
$V_f = \beta V_o$
Feedback network β
V_o
180° Phase shift

Fig. 4.3 Basic block diagram of oscillator circuit

Consider a fictitious voltage V_i applied at the input of the amplifier. Hence we get,

$$\boxed{V_o = A\ V_i} \qquad \text{...(1)}$$

The feedback factor β decides the feedback to be given to input,

$$\boxed{V_f = \beta\ V_o} \qquad \text{...(2)}$$

Substituting (1) into (2) we get,

$$\boxed{V_f = A\,\beta\,V_i} \quad \text{...(3)}$$

For the oscillator, we want that feedback should drive the amplifier and hence V_f must act as V_i. From equation (3) we can write that, V_f is sufficient to act as V_i when,

$$\boxed{|\,A\,\beta\,| = 1} \quad \text{...(4)}$$

And the phase of V_f is same as V_i i.e. feedback network should introduce 180° phase shift in addition to 180° phase shift introduced by inverting amplifier. This ensures positive feedback. So total phase shift around a loop is 360°.

In this condition, V_f drives the circuit and without external input circuit works as an oscillator.

The two conditions discussed above, required to work the circuit as an oscillator are called **Barkhausen Criterion** for oscillation.

The **Barkhausen Criterion** states that :

1. The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely **0° or 360°**.
2. The magnitude of the product of the open loop gain of the amplifier (A) and the magnitude of the feedback factor β is unity i.e. **$|\,A\,\beta\,| = 1$.**

Satisfying these conditions, the circuit works as an oscillator producing sustained oscillations of constant frequency and amplitude.

In reality, no input signal is needed to start the oscillations. In practice, $A\beta$ is made greater than 1 to start the oscillations and then circuit adjusts itself to get $A\beta = 1$, finally resulting into self sustained oscillations. Let us see the effect of the magnitude of the product $A\beta$ on the nature of the oscillations.

4.3.1 $|\,A\,\beta\,| > 1$

When the total phase shift around a loop is 0° or 360° and $|A\beta| > 1$, then the output oscillates but the oscillations are of growing type. The amplitude of oscillations goes on increasing as shown in the Fig. 4.4.

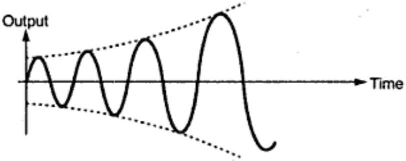


Fig. 4.4 Growing type oscillations

4.3.2 | A β | = 1

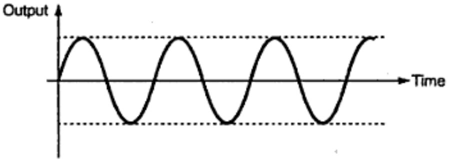


Fig. 4.5 Sustained oscillations

As stated by Barkhausen criterion, when total phase shift around a loop is 0° or 360° ensuring positive feedback and $|A\ \beta| = 1$ then the oscillations are with constant frequency and amplitude called sustained oscillations.

Such oscillations are shown in the Fig. 4.5.

4.3.3 | A β | < 1

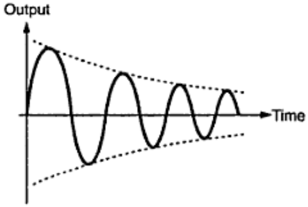


Fig. 4.6 Exponentially decaying oscillations

When total phase shift around a loop is 0° or 360° but $|A\beta| < 1$ then the oscillations are of decaying type i.e. such oscillation amplitude decreases exponentially and the oscillations finally cease. Thus circuit works as an amplifier without oscillations. The decaying oscillations are shown in the Fig. 4.6.

So to start the oscillations without input, $|A\beta|$ is kept higher than unity and then circuit adjusts itself to get $|A\beta| = 1$ to result sustained oscillations.

4.3.4 Starting Voltage

It is mentioned that no external input is required in case of oscillators. In the earlier analysis also, the input V_i is assumed as fictitious input and practically no such input is required. The oscillator output supplies its own input under proper conditions. The obvious question is if no input is required, how oscillator starts ? And where does the starting voltage come from ?

Every resistance has some free electrons. Under the influence of normal room temperature, these free electrons move randomly in various directions. Such a movement of the free electrons generate a voltage called **noise voltage,** across the resistance. Such noise voltages present across the resistances are amplified. Hence to amplify such small noise voltages and to start the oscillations, $|A\beta|$ is kept greater than unity at start. Such amplified voltage appears at the output terminals. The part of this output is sufficient to drive the input of amplifier circuit. Then circuit adjusts itself to get $|A\beta| = 1$ and with phase shift of 360° we get sustained oscillations.

4.4 Classification of Oscillators

The oscillators are classified based on the nature of the output waveform, the parameters used, the range of frequency etc. The various ways in which oscillators are classified as :

4.4.1 Based on the Output Waveform

Under this, the oscillators are classified as sinusoidal and nonsinusoidal oscillators. The sinusoidal oscillators generate purely sinusoidal waveform at the output. While nonsinusoidal oscillators generate an output waveform as triangular, square, sawtooth etc. In this chapter, we are going to discuss only sinusoidal oscillators.

4.4.2 Based on the Circuit Components

The oscillators using the components resistance (R) and capacitor (C), are called RC oscillators. While the oscillators using the components inductance (L) and capacitor (C), are called LC oscillators. In some oscillators, crystal is used, which are called crystal oscillators.

4.4.3 Based on the Range of Operating Frequency

If the oscillators are used to generate the oscillations at audio frequency range which is 20 Hz to 100 - 200 kHz, then the oscillators are classified as low frequency (L.F.) or audio frequency (A.F.) oscillators. While the oscillators used at the frequency range more than 200 - 300 kHz upto gigahertz (GHz) are classified as high frequency (H.F.) or radio frequency (R.F.) oscillators. The RC oscillators are used at low frequency range while the LC oscillators are used at high frequency range.

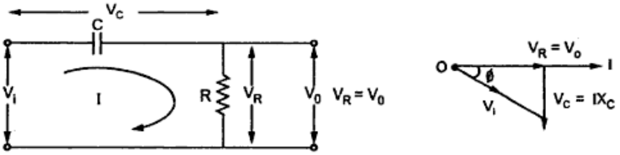
4.4.4 Based on : Whether Feedback is Used or Not ?

The oscillators in which the feedback is used, which satisfies the required conditions, are classified as feedback type of oscillators. The oscillators in which the feedback is not used to generate the oscillations, are classified as nonfeedback oscillators. The nonfeedback oscillators use the negative resistance region of the characteristics of the device used. The example of the nonfeedback type of oscillator is the UJT relaxation oscillator.

4.5 R-C Phase Shift Oscillator

RC phase shift oscillator basically consists of an amplifier and a feedback network consisting of resistors and capacitors arranged in ladder fashion. Hence such an oscillator is also called ladder type RC phase shift oscillator.

To understand the operation of this oscillator let us study RC circuit first, which is used in the feedback network of this oscillator. The Fig. 4.7 shows the basic RC circuit.



(a) Circuit **Fig. 4.7** **(b) Phasor diagram**

The capacitor C and resistance R are in series. Now X_C is the capacitive reactance in ohms given by,

$$X_C = \frac{1}{2\pi f C} \quad \Omega$$

The total impedance of the circuit is,

$$Z = R - j\,X_C = R - j\left(\frac{1}{2\pi f C}\right) \ \Omega = |Z| \ \angle -\phi ° \Omega$$

The r.m.s. value of the input voltage applied is say V_i volts. Hence the current is given by,

$$I = \frac{V_i \angle 0°}{Z} = \frac{V_i \angle 0°}{|Z| \angle -\phi}$$

$$\therefore \qquad \boxed{\begin{array}{rcl} I & = & \frac{V_i}{Z} \angle +\phi \quad A \\ |Z| & = & \sqrt{R^2 + (X_C)^2} \\ \phi & = & \tan^{-1}\left(\frac{X_C}{R}\right) \end{array}}$$

where $|Z|$ is as above and ϕ as above.

From expression of current it can be seen that **current I leads input voltage V_i by angle ϕ.**

The output voltage V_o is the drop across resistance R given by,

$$\boxed{V_o = V_R = IR}$$

The voltage across the capacitor is,

$$\boxed{V_C = I\,X_C}$$

The drop V_R is in phase with current I while the drop V_C lags current I by 90° i.e. I leads V_C by 90°. The phasor diagram is shown in the Fig. 4.7 (b).

By using proper values of R and C, **the angle ϕ is adjusted in practice equal to 60°**, as required for RC phase shift oscillator.

4.5.1 RC Feedback Network

As stated earlier, RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. Thus if one RC network produces phase shift of $\phi = 60°$ then to produce phase shift of 180° such three RC networks must be connected in cascade. Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60°, thus total phase shift due to feedback is 180° ($3 \times 60°$). Such a feedback network is shown in the Fig. 4.8.

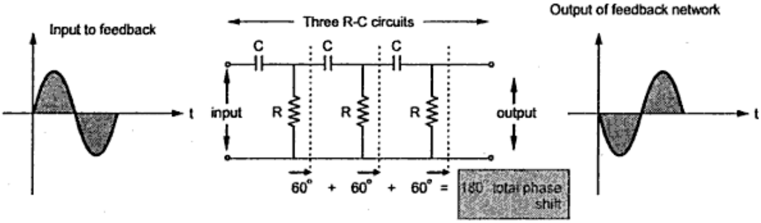

Input to feedback
t
Three R-C circuits
C
C
C
input
R
R
R
output
60° + 60° + 60° = 180° total phase shift
Output of feedback network
t

Fig. 4.8 Feedback network in RC phase shift oscillator

The network is also called the **ladder network.** All the resistance values and all the capacitance values are same, so that for a particular frequency, each section of R and C produces a phase shift of 60°.

4.5.2 Phase Shift Oscillator using Transistor

In a practical RC phase shift oscillator, a common emitter (CE) single stage amplifier is used as a basic amplifier. This produces 180° phase shift. The feedback network consists of 3 RC sections each producing 60° phase shift. Such a RC phase shift oscillator using BJT amplifier is shown in the Fig. 4.9.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

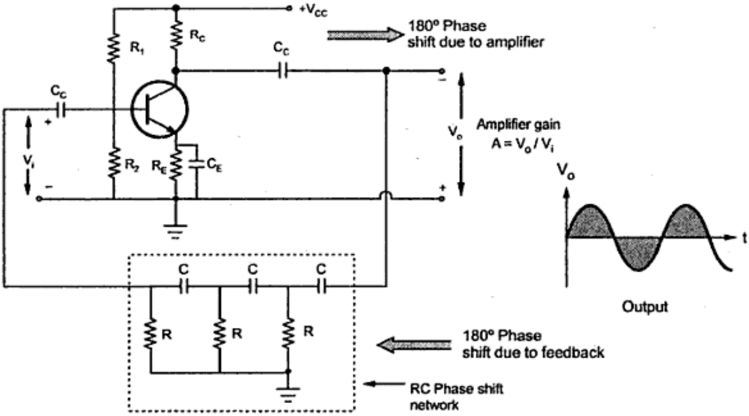

+Vcc
R1
Rc
Cc
180° Phase
shift due to amplifier
Cc
+
Vi
-
R2
RE
CE
-
Vo
+
Amplifier gain
A = Vo / Vi
Vo
t
Output
C
C
C
R
R
R
180° Phase
shift due to feedback
RC Phase shift
network

Fig. 4.9 Transistorised RC phase shift oscillator

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{6}\,R\,C}}$$

The frequency is measured in Hz.

Actually to satisfy the Barkhausen condition, the expression for the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi\,R\,C}\cdot\frac{1}{\sqrt{6+4K}}}$$

where $K = \frac{R_C}{R}$

As practically R_C/R is small, K is neglected,

The condition of h_{fe} for the transistor to obtain the oscillations is given by,

$$\boxed{h_{fe} > 4K + 23 + \frac{29}{K}}$$

And value of K for minimum h_{fe} is 2.7 hence minimum h_{fe} = 44.5. So transistor with h_{fe} less than 44.5 cannot be used in phase shift oscillator.

But for most of practical circuits, the expression for the frequency is considered as,

$$\boxed{f = \frac{1}{2\pi\sqrt{6}\,RC}}$$

4.5.3 Derivation for the Frequency of Oscillations

Replacing the transistor by its approximate h-parameter model, we get the equivalent oscillator circuit as shown in the Fig. 4.10.

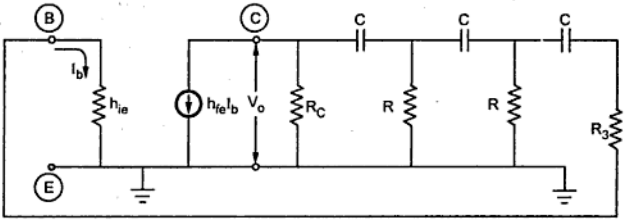


Fig. 4.10 Equivalent circuit using h-parameter model

Practically R_3 is used such that h_{ie} of transistor alongwith R_3 completers the need of R.

$$\therefore \quad \boxed{R = h_{ie} + R_3}$$

Note : If the resistances R_1 and R_2 are not neglected then the input impedance of the amplifier stage becomes as,

$$\boxed{R_i' = R_1 \,||\, R_2 \,||\, h_{ie}} \qquad \dots (1)$$

In such a case, the value of R_3 must be so selected that

$$\boxed{R_i' + R_3 = R} \qquad \dots (2)$$

Similarly we can replace, the current source h_{fe} I_b by its equivalent voltage source. And assume the ratio of the resistance R_C to R be K.

$$\therefore \quad \boxed{K = \frac{R_C}{R}}$$

The modified equivalent circuit is shown in the Fig. 4.11.

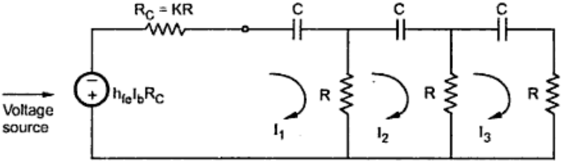


Fig. 4.11 Modified equivalent circuit

Applying KVL for the various loops in the modified equivalent circuit we get,

For Loop 1,

$$-I_1\, R_C - \frac{1}{j\omega C} I_1 - I_1\, R + I_2\, R - h_{fe}\, I_b\, R_C = 0$$

Replacing R_C by KR and $j\omega$ by s we get,

$$\therefore \qquad +I_1\,[(K+1)\,R + \frac{1}{sC}] - I_2\, R = -\text{hfe}\, I_b\, KR \qquad \text{... (3)}$$

For Loop 2,

$$-\frac{1}{j\omega C} I_2 - I_2R - I_2R + I_1R + I_3R = 0$$

$$\therefore \qquad -I_1R + I_2\left[2R + \frac{1}{sC}\right] - I_3R = 0 \qquad \text{... (4)}$$

For Loop 3,

$$-I_3\, \frac{1}{j\omega C} - I_3R - I_3R + I_2R = 0$$

$$\therefore \qquad -I_2R + I_3\left[2R + \frac{1}{sC}\right] = 0 \qquad \text{... (5)}$$

Using Cramer's Rule to solve for I_3,

$$D = \begin{vmatrix} (K+1)\,R + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$$

$$= \left[(K+1)\,R + \frac{1}{sC}\right]\left[2R + \frac{1}{sC}\right]^2 - R^2\left[2R + \frac{1}{sC}\right] - R^2\left[(K+1)\,R + \frac{1}{sC}\right]$$

$$= \frac{[sRC\,(K+1)+1]\,[2sCR+1]^2}{s^3\,C^3} - \frac{R^2\,(2sCR+1)}{sC} - \frac{R^2\,[(K+1)\,sRC+1]}{s\,C}$$

First term can be written as,

$[sKRC + sRC + 1]\ [4\ s^2\ C^2\ R^2 + 4\ sRC + 1]/s^3\ C^3$

$$= \frac{4\,s^3\,K\,R^3\,C^3 + 4\,s^3\,R^3\,C^3 + 4\,s^2\,C^2\,R^2 + 4\,s^2\,K\,R^2\,C^2 + 4s^2\,R^2\,C^2 + 4sRC + sKRC + sRC + 1}{s^3\,C^3}$$

Second and the Third term can be combined to get,

$$= \frac{-R^2\,[KsRC + sRC + 1] - R^2\,[1 + 2sRC]}{s\,C}$$

$$= \frac{-[2R^2 + 3s\,R^3\,C + Ks\,R^3\,C]}{s\,C}$$

Combining the two terms and taking LCM as s^3C^3 we get,

$$D = \frac{s^3\,C^3\,R^3\,[4K+4] + s^2\,C^2\,R^2\,[4K+8] + sRC[5+K] + 1 - [2\,R^2 + 3\,s\,R^3\,C + Ks\,R^3\,C]\,s^2\,C^2}{s^3\,C^3}$$

$$= \frac{s^3\,C^3\,R^3\,[3K+1] + s^2\,C^2\,R^2\,[4K+6] + sRC[5+K] + 1}{s^3\,C^3} \qquad \ldots (6)$$

Now

$$D_3 = \begin{vmatrix} (K+1)\,R + \frac{1}{sC} & -R & -h_{fe}\,I_b\,KR \\ -R & 2R + \frac{1}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= -R^2\,(h_{fe}\,I_b\,KR)$$

$$= -K\,R^3\,h_{fe}\,I_b \qquad \ldots (7)$$

$$\therefore \qquad I_3 = \frac{D_3}{D}$$

$$= \frac{-KR^3\,h_{fe}\,I_b\,s^3\,C^3}{s^3\,C^3\,R^3\,[3K+1] + s^2\,C^2\,R^2\,[4K+6] + sRC\,[5K+1] + 1} \qquad \ldots (8)$$

Now I_3 = Output current of the feedback circuit

I_b = Input current of the amplifier

$I_c = h_{fe}\,I_b$ = Input current of the feedback circuit

$$\therefore \qquad \beta = \frac{\text{Output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{h_{fe}\,I_b}$$

And $$A = \frac{\text{Output of amplifier circuit}}{\text{Input to amplifier circuit}} = \frac{I_3}{I_b} = h_{fe}$$

∴ $$A\beta = \frac{I_3}{h_{fe}\, I_b} \times h_{fe} = \frac{I_3}{I_b} \qquad \ldots (9)$$

Using equation (9) we get,

$$A\beta = \frac{-KR^3\, h_{fe}\, s^3\, C^3}{s^3\, C^3\, R^3\, [3K+1] + s^2\, C^2\, R^2\, [4K+6] + sRC\,[5K+1] + 1} \qquad \ldots (10)$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = j^3\omega^3 = -j\omega^3$ in the equation (10) we get,

$$A\beta = \frac{-j\omega^3\, KR^3\, C^3\, h_{fe}}{-j\omega^3\, C^3\, R^3\, [3K+1] - \omega^2\, C^2\, R^2\, [4K+6] + j\omega RC\,[5+K] + 1}$$

Separating the real and imaginary parts in the denominator we get,

$$A\beta = \frac{-j\omega^3\, KR^3\, C^3\, h_{fe}}{[1 - 4K\omega^2\, C^2\, R^2 - 6\,\omega^2\, C^2\, R^2] - j\omega[3K\,\omega^2\, R^3\, C^3 + \omega^2\, R^3\, C^3 - 5RC - KRC]}$$

Dividing numerator and denominator by $j\omega^3\, R^3\, C^3$,

$$A\beta = \frac{Kh_{fe}}{\left\{\dfrac{(1 - 4K\omega^2\, C^2\, R^2 - 6\,\omega^2\, C^2\, R^2)}{-j\omega^3\, R^3\, C^3}\right\} - \left\{\dfrac{j\omega[3K\,\omega^2\, R^3\, C^3 + \omega^2\, R^3\, C^3 - 5RC - KRC]}{-j\omega^3\, R^3\, C^3}\right\}}$$

Replacing $-1/j = j$,

$$= \frac{Kh_{fe}}{j\left\{\dfrac{1}{\omega^3\, R^3\, C^3} - \dfrac{4K}{\omega RC} - \dfrac{6}{\omega RC}\right\} + \left\{3K+1 - \dfrac{5}{\omega^2\, R^2\, C^2} - \dfrac{K}{\omega^2\, R^2\, C^2}\right\}}$$

Replacing $\frac{1}{\omega RC} = \alpha$ for simiplicity

∴ $$A\beta = \frac{K h_{fe}}{[3K+1-5\alpha^2-K\alpha^2] + j[\alpha^3 - 4K\alpha - 6\alpha]} \qquad \ldots (11)$$

As per the Barkhausen Criterion, $\angle A\beta = 0°$. Now the angle of numerator term Kh_{fe} of the equation (11) is 0° hence to have angle of the Aβ term as 0°, the imaginary part of the denominator term must be 0.

∴ $$\alpha^3 - 4K\alpha - 6\alpha = 0$$

$$\alpha(\alpha^2 - 4K - 6) = 0$$

∴ $$\alpha^2 = 4K + 6 \text{ neglecting zero value}$$

$$\therefore \qquad \alpha = \sqrt{4K+6}$$

$$\therefore \qquad \frac{1}{\omega RC} = \sqrt{4K+6}$$

$$\boxed{\omega = \frac{1}{RC\sqrt{4K+6}}}$$

$$\therefore \qquad \boxed{f = \frac{1}{2\pi RC\sqrt{4K+6}}} \qquad \ldots(12)$$

This is the frequency at which $\angle A\beta = 0°$. At the same frequency, $|A\beta| = 1$.

Substituting $\alpha = \sqrt{4K+6}$ in the equation (11) we get,

$$A\beta = \frac{Kh_{fe}}{3K+1-(4K+6)[5+K]}$$

$$= \frac{Kh_{fe}}{3K+1-20K-30-4K^2-6K}$$

$$= \frac{Kh_{fe}}{-4K^2-23K-29}$$

Now $\qquad |A\beta| = 1$

$$\therefore \qquad \left|\frac{Kh_{fe}}{-4K^2-23K-29}\right| = 1$$

$$\therefore \qquad Kh_{fe} = 4K^2+23K+29$$

$$\boxed{h_{fe} = 4K + 23 + \frac{29}{K}} \qquad \ldots(13)$$

This must be the value of h_{fe} for the oscillations.

.5.4 Minimum Value of h_{fe} for the Oscillations

To get minimum value of h_{fe},

$$\frac{d\,h_{fe}}{dK} = 0$$

$$\therefore \qquad \frac{d}{dk}\left[4K+23+\frac{29}{K}\right] = 0$$

$$\therefore \qquad \left[4-\frac{29}{K^2}\right] = 0$$

$$\therefore \quad K^2 = \frac{29}{4}$$

$$\therefore \quad K = 2.6925 \text{ for minimum } h_{fe} \qquad \ldots (14)$$

Substituting in the equation (13),

$$(h_{fe})_{min} = 4\,(2.6925) + 23 + \frac{29}{(2.6925)}$$

$$\therefore \quad \boxed{(h_{fe})_{min} = 44.54} \qquad \ldots(15)$$

Key Point: *Thus for the circuit to oscillate, we must select the transistor whose* (h_{fe}) *min should be greater than 44.54.*

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

➡ **Example 4.1:** *Find the capacitor C and* h_{fe} *for the transistor to provide a resonating frequncy of 10 kHz of a transistorised phase shift oscillator. Assume* $R_1 = 25\ k\Omega$, $R_2 = 57\ k\Omega$, $R_C = 20\ k\Omega$, $R = 7.1\ k\Omega$ *and* $h_{ie} = 1.8\ k\Omega$.

Solution : Referring to equation (1),

$$R_i' = R_1 \parallel R_2 \parallel h_{ie} = 25\ k\Omega \parallel 57\ k\Omega \parallel 1.8\ k\Omega$$

$$\frac{1}{R_i'} = \frac{1}{25} + \frac{1}{57} + \frac{1}{1.8}$$

$$\therefore \quad R_i' = 1.631\ k\Omega$$

$$\text{Now} \quad R_i' + R_3 = R$$

$$\therefore \quad R_3 = R - R_i' = 7.1 - 1.631$$

$$= 5.47\ K\Omega$$

$$K = \frac{R_C}{R} = \frac{20}{7.1} = 2.816$$

$$\text{Now} \quad f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$$\therefore \quad 10\times10^3 = \frac{1}{2\pi\times7.1\times10^3\times C\times\sqrt{6+4\times2.816}}$$

$$\therefore \quad C = 539.45\ \text{pF}$$

$$h_{fe} \geq 4K + 23 + \frac{29}{K} \qquad \text{refer equation (13)}$$

$$\therefore \quad h_{fe} \geq 4\times 2.816+23+\frac{29}{2.816}$$

$$\therefore \quad h_{fe} \geq \mathbf{44.562}$$

4.5.5 Advantages

The advantages of R - C phase shift oscillator are,

1. The circuit is simple to design.
2. Can produce output over audio frequency range.
3. Produces sinusoidal output waveform.
4. It is a fixed frequency oscillator.

4.5.6 Disadvantages

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

And the frequency stability is poor due to the changes in the values of various components, due to effect of temperature, aging etc.

➠ **Example 4.2 :** *In a RC phase shift oscillator, the phase shift network uses the resistances each of 4.7 kΩ and the capacitors each of 0.47 μF. Find the frequency of oscillations.*

Solution : The given values are, $R = 4.7\ k\Omega$ and $C = 0.47\ \mu F$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6}\times 4.7\times 10^{3}\times 0.47\times 10^{-6}} = \mathbf{29.413\ Hz}$$

➠ **Example 4.3 :** *Estimate the values of R and C for an output frequency of 1 kHz in a RC phase shift oscillator.*

Solution : $f = 1$ kHz

Now $$f = \frac{1}{2\pi\sqrt{6}RC}$$

Choose $C = \mathbf{0.1\ \mu F}$

$$\therefore \quad 1\times 10^{3} = \frac{1}{2\pi\sqrt{6}R\times 0.1\times 10^{-6}}$$

$$\therefore \quad R = \mathbf{649.747\ \Omega}$$

Choose $R = \mathbf{680\ \Omega}$ standard value

4.5.7 FET Phase Shift Oscillator

The practical circuit of FET phase shift oscillator is shown in the Fig. 4.12.

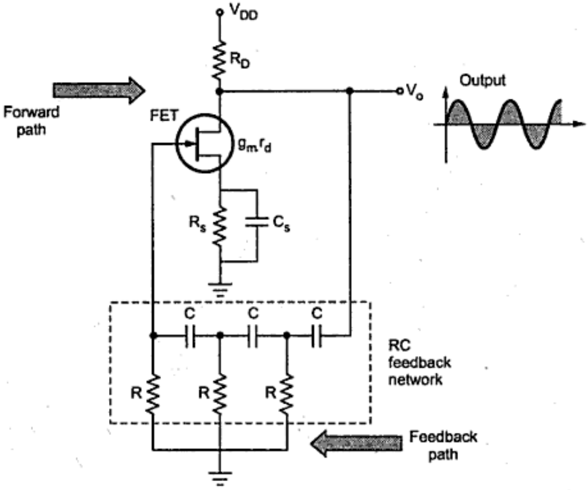

V_{DD}
R_D
Forward path
FET
g_m, r_d
V_o
Output
R_s
C_s
C
C
C
R
R
R
RC feedback network
Feedback path

Fig. 4.12 FET phase shift oscillator

For the amplifier stage FET is used. It is self biased with a capacitor bypassed source resistance R_S and a drain bias resistance R_D. The important parameters of FET are g_m and r_d. From FET amplifier theory we can write,

$$\boxed{|A| = g_m R_L} \quad \text{... (27)}$$

Where R_L is the parallel equivalent of R_D and r_d.

$$\boxed{R_L = \frac{R_D\, r_d}{R_D + r_d}} \quad \text{... (28)}$$

Key Point : *The input impedance of the FET amplifier stage can be conveniently assumed as infinite, as long as the operating frequency is low enough to neglect the capacitive impedances.*

The feedback network is again three stage R_C network having gain,

$$\boxed{\begin{aligned} |\beta| &= \frac{1}{29} \\ |A| &\geq 29 \end{aligned}} \qquad \ldots (29)$$

∴

Hence the condition on gain of the amplifier is same as in case of op-amp, the frequency of the oscillator is given by,

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}} \qquad \ldots (30)$$

Example 4.4 : *A phase shift oscillator is to be designed with FET having* $g_m = 5000\ \mu S$, $r_d = 4\ k\Omega$ *while the resistance in the feedback circuit is 9.7 kΩ. Select the proper value of C and* R_D *to have the frequency of oscillations as 5 kHz.*

Solution : Using the expression for the frequency

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$\therefore \quad 5\times10^3 = \frac{1}{2\pi\times9.7\times10^3\times C\times\sqrt{6}}$$

$$\therefore \quad C = \mathbf{1.34\ nF}$$

Now using the equation (27),

$$|A| = g_m R_L$$

$$\therefore \quad |A| \geq 29$$

$$\therefore \quad g_m R_L \geq 29$$

$$\therefore \quad R_L \geq \frac{29}{g_m} \geq \frac{29}{5000\times10^{-6}} \geq 5.8\ k\Omega$$

With value of $R_L = 6.8\ k\Omega$,

$$R_L = \frac{R_D\, r_d}{R_D + r_d}$$

$$\therefore \quad 6.8\times10^3 = \frac{R_D\times40\times10^3}{R_D + 40\times10^3}$$

$$\therefore \quad R_D + 40 \times 10^3 = 5.8823\ R_D$$

$$\therefore \quad 4.8823\ R_D = 40 \times 10^3$$

$$\therefore \quad R_D = \mathbf{8.12\ k\Omega}$$

While for minimum value of $R_L = 5.8\ k\Omega$

$$R_D = \mathbf{6.78\ k\Omega}$$

4.6 Wien Bridge Oscillator

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But **Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage.** As total phase shift required is 0° or 2nπ radians, in Wien bridge type no phase shift is necessary through feedback.

Key Point : *Thus the total phase shift around a loop is 0°.*

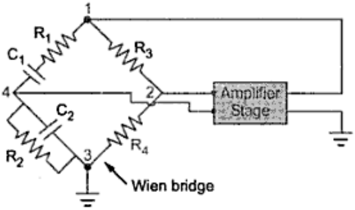


Fig. 4.13 Basic circuit of Wien bridge oscillator

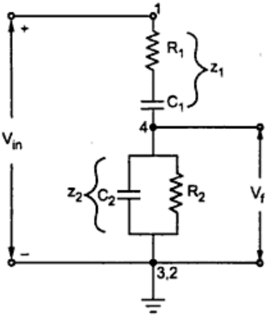


Fig. 4.14 Feedback network of Wien bridge oscillator

Let us study the basic version of the Wien bridge oscillator and its analysis.

A basic Wien bridge used in this oscillator and an amplifier stage is shown in the Fig. 4.13.

The output of the amplifier is applied between the terminals 1 and 3, which is the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own input through the Wien bridge as a feedback network.

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called **frequency sensitive arms.** This is because the components of these two arms decide the frequency of the oscillator. Let us find out the gain of the feedback network. As seen earlier input V_{in} to the feedback network is between 1 and 3 while output V_f of the feedback network is between 2 and 4. This is shown in the Fig. 4.14. Such a feedback network is called **lead-lag network**. This is because at very low frequencies it acts like a lead while at very high frequencies it acts like lag network.

Now from the Fig. 4.14, as shown,

$$\boxed{Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1+j\omega R_1 C_1}{j\omega C_1}}$$

$$Z_2 = R_2 \parallel \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$$\therefore \quad \boxed{Z_2 = \frac{R_2}{1+j\omega R_2 C_2}} \quad \ldots (1)$$

Replacing $j\omega = s$,

$$\boxed{Z_1 = \frac{1+s R_1 C_1}{s C_1}}$$

and

$$\boxed{Z_2 = \frac{R_2}{1+s R_2 C_2}}$$

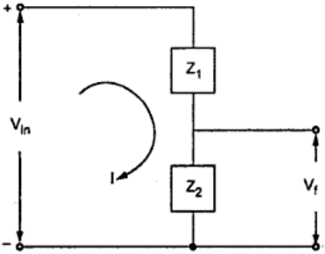


Fig. 4.15 Simplified circuit

$$I = \frac{V_{in}}{Z_1 + Z_2}$$

and $$V_f = I Z_2$$

$\therefore$ $$V_f = \frac{V_{in} Z_2}{Z_1 + Z_2}$$

$\therefore$ $$\boxed{\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}} \qquad \text{...(2)}$$

Substituting the values of Z_1 and Z_2,

$$\beta = \frac{\left[\frac{R_2}{1+sR_2C_2}\right]}{\left[\frac{1+sR_1C_1}{sC_1}\right]+\left[\frac{R_2}{1+sR_2C_2}\right]}$$

$$\beta = \frac{s C_1 R_2}{(1+s R_1 C_1)(1+s R_2 C_2)+s C_1 R_2}$$

$$= \frac{s C_1 R_2}{1+s (R_1 C_1 + R_2 C_2)+s^2 R_1 R_2 C_1 C_2 + s C_1 R_2}$$

$$= \frac{s C_1 R_1}{1+s (R_1 C_1 + R_2 C_2 + C_1 R_2)+s^2 R_1 R_2 C_1 C_2}$$

Replacing s by $j\omega$, $s^2 = -\omega^2$

$\therefore$ $$\beta = \frac{j\omega C_1 R_2}{(1-\omega^2 R_1 R_2 C_1 C_2)+j\omega(R_1 C_1 + R_2 C_2 + C_1 R_2)} \qquad \text{... (3)}$$

Rationalising the expression,

$$\beta = \frac{j\omega C_1 R_2 \left[(1-\omega^2 R_1 R_2 C_1 C_2)-j\omega(R_1 C_1 + R_2 C_2 + C_1 R_2)\right]}{\left(1-\omega^2 R_1 R_2 C_1 C_2\right)^2 + \omega^2 \left(R_1 C_1 + R_2 C_2 + C_1 R_2\right)^2}$$

$$\boxed{\beta = \frac{\omega^2 C_1 R_2 (R_1 C_1 + R_2 C_2 + C_1 R_2)+j\omega C_1 R_2 (1-\omega^2 R_1 R_2 C_1 C_2)}{\left(1-\omega^2 R_1 R_2 C_1 C_2\right)^2 + \omega^2 \left(R_1 C_1 + R_2 C_2 + C_1 R_2\right)^2}}$$

... (4)

To have zero phase shift of the feedback network, its imaginary part must be zero.

$$\therefore \quad \omega(1-\omega^2 R_1R_2C_1C_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{R_1R_2C_1C_2} \text{ neglecting zero value.}$$

$$\boxed{\omega = \frac{1}{\sqrt{R_1R_2C_1C_2}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}} \qquad \ldots(5)$$

Key Point : *This is the frequency of the oscillator and it shows that the components of the frequency sensitive arms are the deciding factors, for the frequency.*

In practice, $R_1 = R_2 = R$ and $C_1 = C_2 = C$ are selected.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R^2C^2}}$$

$$\boxed{f = \frac{1}{2\pi RC}} \qquad \ldots(6)$$

At $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the gain of the feedback network becomes,

$$\beta = \frac{\omega^2 RC(3RC) + j\omega RC\left(1-\omega^2R^2C^2\right)}{\left(1-\omega^2R^2C^2\right) + \omega^2(3RC)^2}$$

Substituting $f = \frac{1}{2\pi RC}$ i.e. $\omega = \frac{1}{RC}$,

we get the magnitude of the feedback network at the resonating frequency of the oscillator as,

$$\beta = \frac{3}{0 + \frac{1}{R^2C^2} \times (3RC)^2} = \frac{3}{9}$$

$$\therefore \quad \boxed{\beta = \frac{1}{3}} \qquad \ldots(7)$$

The positive sign of β indicates that the phase shift by the feedback network is 0°. Now to satisfy the Barkhausen criterion for the sustained oscillations, we can write,

$$|A\beta| \geq 1$$

$$\therefore \quad |A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{3}\right)}$$

$$\therefore \quad \boxed{|A| \geq 3}$$

This is the required gain of the amplifier stage, without any phase shift.

If $R_1 \neq R_2$ and $C_1 \neq C_2$ then

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}}$$

Substituting in the equation (4) we get,

$$\boxed{\beta = \frac{C_1R_2}{(R_1C_1 + R_2C_2 + C_1R_2)}}$$

$$|A\beta| \geq 1$$

$$\therefore \quad \boxed{A \geq \frac{R_1C_1 + R_2C_2 + C_1R_2}{C_1R_2}} \quad \text{... (8)}$$

Another important advantage of the Wien bridge oscillator is that by varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be provided.

Let us see the various versions of the Wien bridge oscillator by considering various circuits for the amplifier stage.

4.6.1 Transistorised Wien Bridge Oscillator

In this circuit, two stage common emitter transistor amplifier is used. Each stage contributes 180° phase shift hence the total phase shift due to the amplifier stage becomes 360° i.e. 0° which is necessary as per the oscillator conditions.

The practical, transistorised Wien bridge oscillator circuit is shown in the Fig. 4.16.

The bridge consists of R and C in series, R and C in parallel, R_3 and R_4. The feedback is applied from the collector of Q_2 through the coupling capacitor, to the bridge circuit.

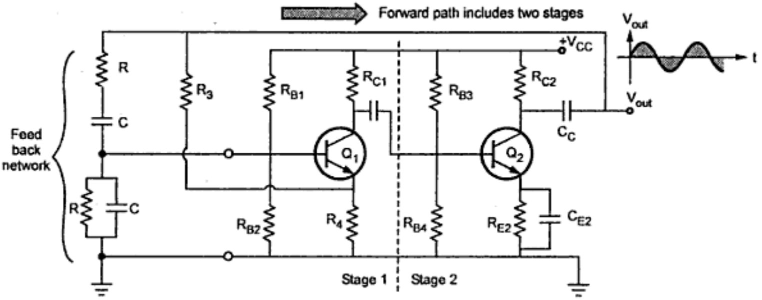


Fig. 4.16 Transistorised Wien bridge oscillator

The resistance R_4 serves the dual purpose of emitter resistance of the transistor Q_1 and also the element of the Wien bridge.

The two stage amplifier provides a gain much more than 3 and it is necessary to reduce it. To reduce the gain, the negative feedback is used without bypassing the resistance R_4. The negative feedback can accomplish the gain stability and can control the output magnitude. The negative feedback also reduces the distortion and therefore output obtained is a pure sinusoidal in nature. The amplitude stability can be improved using a nonlinear resistor for R_4. Due to this, the loop gain depends on the amplitude of the oscillations. Increase in the amplitude of the oscillations, increases the current through nonlinear resistance, which results into an increase in the value of nonlinear resistance R_4. When this value increases, a greater amount of negative feedback is applied. This reduces the loop gain. And hence signal amplitude gets reduced and controlled.

4.6.2 Wien Bridge Oscillator using FET

As a single stage FET amplifier gives a phase shift of 180° and it is required to have 360° phase shift from amplifier stage, the two stages of FET amplifier is the feature of the Wien bridge oscillator using FET.

The basic feedback network of Wien bridge remains same. Hence the condition of the oscillations, remains same.

The practical circuit of Wien bridge oscillator using two stage FET amplifier is shown in the Fig. 4.17.

The RC series and parallel combination forms the frequency sensitive arms of the Wien bridge. The resistances R_3 and R_4 form the part of the feedback path. The unbypassed source resistance R_4 provides the negative feedback required for gain stabilization. The amplifier gain is the product of the gains of the two stages. The operation of the circuit is similar to the Wien bridge oscillator circuit with op-amp.

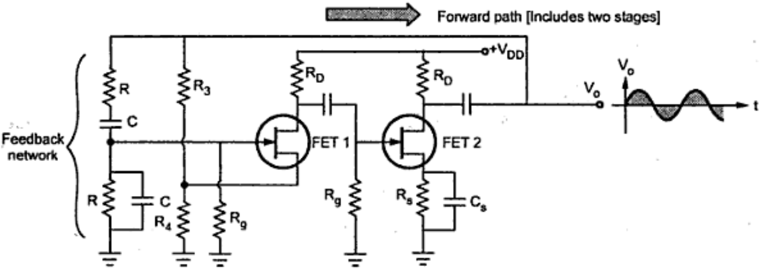


Fig. 4.17 FET Wien bridge oscillator

Key Point : *All the conditions derived earlier for the oscillating conditions are equally applicable to this circuit.*

➡ **Example 4.5 :** *The frequency sensitive arms of the Wien bridge oscillator uses* $C_1 = C_2 = 0.001\ \mu F$ *and* $R_1 = 10\ k\Omega$ *while* R_2 *is kept variable. The frequency is to be varied from 10 kHz to 50 kHz, by varying* R_2*. Find the minimum and maximum values of* R_2*.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

For

$$f = 10\text{ kHz},$$

$$10\times10^3 = \frac{1}{2\pi\sqrt{\left(10\times10^3\times R_2\times(0.001\times10^{-6}\right)^2}}$$

$$\therefore \quad R_2 = \mathbf{25.33\ k\Omega}$$

For

$$f = 50\text{ kHz}$$

$$50\times10^3 = \frac{1}{2\pi\sqrt{\left(10\times10^3\times R_2\times(0.001\times10^{-6}\right)^2}}$$

$$\therefore \quad R_2 = \mathbf{1.013\ k\Omega}$$

So minimum value of R_2 is 1.013 kΩ while the maximum value of R_2 is 25.33 kΩ.

4.7 Comparison of RC Phase Shift and Wien Bridge Oscillators

The similarities and the differences between the two oscillators are given in the Table 4.2.

Sr. No.	RC Phase Shift Oscillator	Wien Bridge Oscillator
1)	It is a phase shift oscillator used for low frequency range.	It is also a phase shift oscillator used for low frequency range.
2)	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
3)	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
4)	Op-amp is used in an inverting mode.	Op-amp is used in non-inverting mode.
5)	Op-amp circuit introduces 180° phase shift.	Op-amp circuit does not introduce any phase shift.
6)	The frequency of oscillations is, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is, $f = \frac{1}{2\pi RC}$
7)	The amplifier gain condition is, $\lvert A \rvert \geq 29$	The amplifier gain condition is, $\lvert A \rvert \geq 3$
8)	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

Table 4.2

4.8 Tuned Oscillator Circuits

The oscillators which use the elements L and C to produce the oscillations are called LC oscillator or tuned oscillators. The circuit using elements L and C is called **tank circuit** or **oscillatory circuit**, which is an important part of LC oscillators. This circuit is also referred as resonating circuit, or tuned circuit. These oscillators are used for high frequency range from 200 kHz upto few GHz. Due to high frequency range, these oscillators are often used for sources of RF (radio frequency) energy. Let us study the basic action of LC tank circuit first.

4.8.1 Operation of LC Tank Circuit

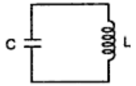


Fig. 4.18 LC tank circuit

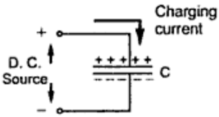

Charging current
+
D. C. Source
−
+ + + + +
C

Fig. 4.19 Initial charging

The LC tank circuit consists of elements L and C connected in parallel as shown in the Fig. 4.18.

Let capacitor is initially charged from a d.c. source with the polarities as shown in the Fig. 4.19.

When the capacitor gets charged, the energy gets stored in a capacitor called electrostatic energy. When such a charged capacitor is connected across inductor L in a tank circuit, the capacitor starts discharging through L, as shown in the Fig. 4.20. The arrow indicates direction of flow of conventional current. Due to such current flow, the magnetic field gets set up around the inductor L. Thus inductor starts storing the energy. When capacitor is fully discharged, maximum current flows through the circuit. At this instant all the electrostatic energy get stored as a magnetic energy in the inductor L. This is shown in the Fig. 4.21.

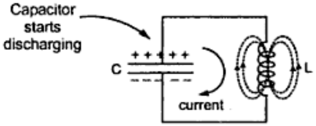

Capacitor starts discharging
+ + + + +
C
current
L

Fig. 4.20

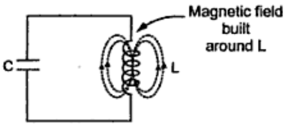

Magnetic field built around L
C
L

Fig. 4.21

Now the magnetic field around L starts collapsing. As per Lenz's law, this starts charging the capacitor with opposite polarity making lower plate positive and upper plate negative, as shown in the Fig. 4.22.

After some time, capacitor gets fully charged with opposite polarities, as compared to its initial polarities. This is shown in the Fig. 4.23. The entire magnetic energy gets converted back to electrostatic energy in capacitor.

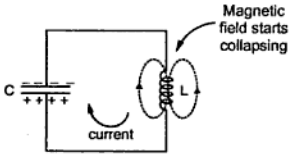

Magnetic field starts collapsing
C
+ + + +
current
L

Fig. 4.22

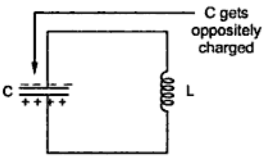

C gets oppositely charged
C
+ + + +
L

Fig. 4.23

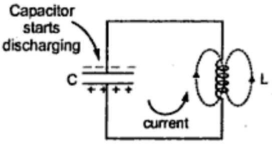


Fig. 4.24

Now capacitor again starts discharging through inductor L. But the direction of current through circuit is now opposite to the direction of current earlier in the circuit. This is shown in the Fig. 4.24. Again electrostatic energy is converted to magnetic energy. When capacitor is fully discharged, the magnetic field starts collapsing, charging the capacitor again in opposite direction.

Key Point: *Thus capacitor charges with alternate polarities and discharges producing alternating current in the tank circuit.*

This is nothing but oscillatory current. But every time when energy is transferred from C to L and L to C, the losses occur due to which amplitude of oscillating current keeps on decreasing everytime when energy transfer takes place. Hence actually we get exponentially decaying oscillations called damped oscillations. These are shown in the Fig. 4.25. Such oscillations stop after sometime.

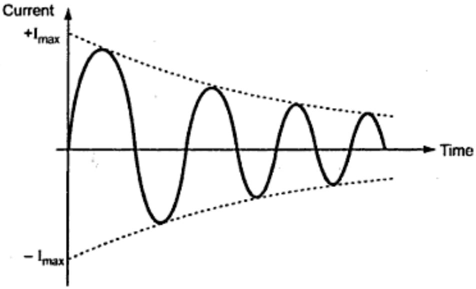


Fig. 4.25 Damped oscillations

Key Point : *In LC oscillator, the transistor amplifier supplies this loss of energy at the proper times.*

The care of proper polarity is taken by the feedback network. Thus LC tank circuit alongwith transistor amplifier can be used to obtain oscillators called LC oscillators. Due to supply of energy which is lost, the oscillations get maintained hence called **sustained oscillations** or **undamped oscillations.**

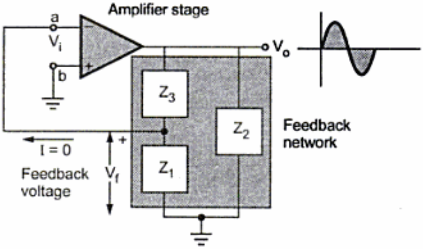
The frequency of oscillations generated by LC tank circuit depends on the values L and C and is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{LC}}}$$

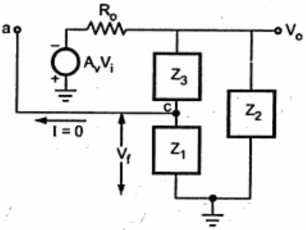
where L is in henries and C is in farads.

4.8.2 Basic Form of LC Oscillator Circuit

As stated earlier, LC tuned circuit forms the feedback network while an op-amp, FET or bipolar junction transistor can be active device in the amplifier stage. The Fig. 4.26 (a) shows the basic form of LC oscillator circuit with gain of the amplifier as A_v. The amplifier output feeds the network consisting of impedances Z_1, Z_2 and Z_3. Assume an active device with infinite input impedance such as FET or op-amp. Then the basic circuit can be replaced by its linear equivalent circuit as shown in the Fig. 4.26 (b).


Amplifier stage
a
V_i
b
−
+
V_o
Z_3
Z_2
Z_1
Feedback network
I = 0
Feedback voltage
V_f
+

(a) Basic form of LC oscillators


R_o
a
V_o
−
A_vV_i
+
Z_3
Z_2
c
Z_1
I = 0
V_f

(b) Equivalent circuit
Fig. 4.26

Amplifier provides a phase shift of 180°, while the feedback network provides an additional phase shift of 180°, to satisfy the required condition.

i) Analysis of the amplifier stage

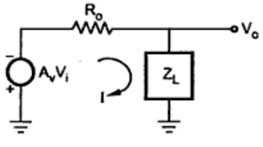


Fig. 4.27

As input impedance of the amplifier is infinite, there is no current flowing towards the input terminals. Let R_o be the output impedance of the amplifier stage.

As I = 0, Z_1, Z_3 appears in series and the combination in parallel with Z_2. The equivalent be Z_L i.e. load impedance. So circuit can be reduced, as shown in the Fig. 4.27.

$$\therefore \quad I = \frac{-A_V V_i}{R_o + Z_L} \quad \dots (1)$$

While

$$V_o = I Z_L \quad \dots (2)$$

$$\therefore \quad V_o = \frac{-A_V V_i Z_L}{R_o + Z_L}$$

$$\therefore \quad \boxed{\frac{V_o}{V_i} = A = \frac{-A_V Z_L}{R_o + Z_L}} \quad \dots (3)$$

where A is the gain of the amplifier stage.

ii) Analysis of the feedback stage

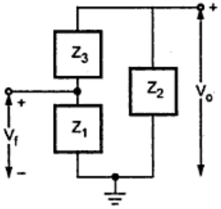


Fig. 4.28

For the feedback factor (β) calculation, consider only the feedback circuit as shown in the Fig. 4.28.

From the voltage division in parallel circuit, we can write,

$$V_f = V_o \left[\frac{Z_1}{Z_1 + Z_3}\right] \quad \dots (4)$$

$$\therefore \quad \frac{V_f}{V_o} = \beta = \frac{Z_1}{Z_1 + Z_3} \quad \dots (5)$$

But as the phase shift of the feedback network is 180°,

$$\therefore \quad \boxed{\beta = -\frac{Z_1}{Z_1 + Z_3}} \quad \dots (6)$$

Obtain an expression for $-A\beta$ as basic Barkhausen condition is $-A\beta = 1$. Refer Equation (4) of the section 4.3.

$$\therefore \qquad -A\beta = \frac{-A_V Z_1 Z_L}{(R_o + Z_L) \times (Z_1 + Z_3)} \qquad \text{... (7)}$$

This is the required loop gain. Now Z_L can be written as $(Z_1 + Z_3) \| Z_2$ i.e.

$$Z_L = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \qquad \text{... (8)}$$

$$\therefore \qquad -A\beta = \frac{-A_V Z_1 \left[\frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right]}{\left[R_o + \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right](Z_1 + Z_3)}$$

Dividing numerator and denominator by $\frac{(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$,

$$= \frac{-A_V Z_1 Z_2}{\left[\frac{R_o (Z_1 + Z_2 + Z_3)}{(Z_1 + Z_3)} + Z_2\right](Z_1 + Z_3)}$$

$$= \frac{-A_V Z_1 Z_2}{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)} \qquad \text{... (9)}$$

As Z_1 Z_2 and Z_3 are the pure reactive elements,

$$Z_1 = jX_1, \quad Z_2 = jX_2 \quad \text{and } Z_3 = jX_3$$

where $X = \omega L$ for an inductive reactance

and $X = \frac{-1}{\omega C}$ for a capacitive reactance.

$$-A\beta = \frac{-A_V (jX_1)(jX_2)}{R_o (jX_1 + jX_2 + jX_3) + jX_2 (jX_1 + jX_3)}$$

$$\boxed{-A\beta = \frac{A_V X_1 X_2}{-X_2 (X_1 + X_3) + jR_o (X_1 + X_2 + X_3)}} \qquad \text{... (10)}$$

To have 180° phase shift, the imaginary part of the denominator must be zero.

$$\therefore \quad \boxed{X_1 + X_2 + X_3 = 0} \qquad \text{... (11)}$$

Substituting in the equation (10),

$$-A\beta = \frac{-A_V X_1 X_2}{X_2 (X_1 + X_3)}$$

But from the equation (11), $X_1 + X_3 = -X_2$

$$\therefore \qquad -A\beta = \frac{-A_V X_1}{-X_2} = +A_V\left(\frac{X_1}{X_2}\right) \qquad \ldots(12)$$

According to the Barkhausen criterion, $-A\beta$ must be positive and must be greater than or equal to unity. As A_V is positive, the $-A\beta$ will be positive only when X_1 and X_2 will have same sign. This indicates that X_1 and X_2 must be of same type of reactances either both inductive or capacitive.

While from the equation (11), we can say that $X_3 = -(X_1 + X_2)$ must be inductive if X_1, X_2 are capacitive while X_3 must be capacitive if X_1, X_2 are inductive.

Table 4.3 shows the various types of the LC oscillators depending on the design of the reactances X_1, X_2 and X_3.

Oscillator type	Reactance elements in the tank circuit		
	X_1	X_2	X_3
Hartley Oscillator	L	L	C
Colpitts Oscillator	C	C	L

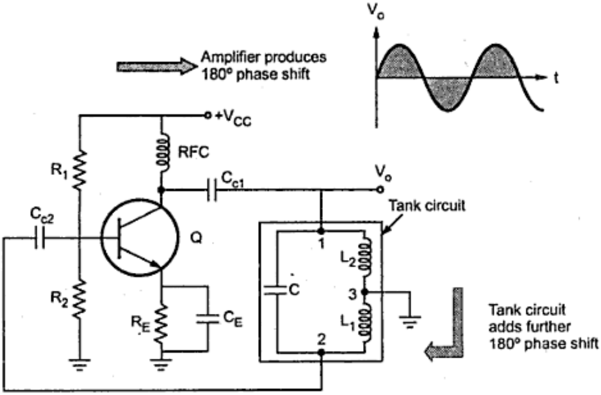
Table 4.3

4.9 Hartley Oscillator

As seen earlier, a LC oscillator which uses two inductive reactances and one capacitive reactance in its feedback network is called Hartley Oscillator.

4.9.1 Transistorised Hartley Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 4.29.



Amplifier produces 180° phase shift
V₀
t
+V_CC
RFC
R₁
C_c1
V₀
Tank circuit
C_c2
Q
1
L₂
C
3
R₂
R_E
C_E
L₁
2
Tank circuit adds further 180° phase shift

Fig. 4.29 Transistorised Hartley oscillator

The resistances R_1 and R_2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high for high frequencies, hence it can be treated as open circuit. While for d.c. conditions, the reactance is zero hence causes no problem for d.c. capacitors.

Hence due to RFC, the isolation between a.c. and d.c. operation is achieved. R_E is also a biasing circuit resistance and C_E is the emitter bypass capacitor. C_{C1} and C_{C2} are the coupling capacitor.

The common emitter amplifier provides a phase shift of 180°. As emitter is grounded, the base and the collector voltages are out of phase by 180°. As the centre of L_1 and L_2 is grounded, when upper end becomes positive, the lower becomes negative and viceversa. So the LC feedback network gives an additional phase shift of 180°, necessary to satisfy oscillation conditions.

4.9.2 Derivation of Frequency of Oscillations

The output current which is the collector current is $h_{fe}I_b$ where I_b is the base current. Assuming coupling condensers are short, the capacitor C is between base and collector. The inductance L_1 is between base and emitter while the inductance L_2 is between collector and emitter. The equivalent circuit of the feedback network is shown in the Fig. 4.30.

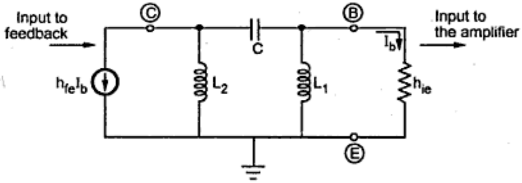


Fig. 4.30 Equivalent circuit

As h_{ie} is the input impedance of the transistor. The output of the feedback is the current I_b which is the input current of the transistor. While input to the feedback network is the output of the transistor which is $I_c = h_{fe}I_b$, converting current source into voltage source we get,

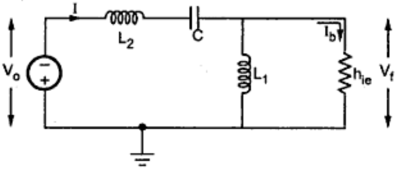


Fig. 4.31 Simplified equivalent circuit

$$V_o = h_{fe}I_b X_{L_2} = h_{fe}I_b j\omega L_2 \qquad \ldots (1)$$

Now L_1 and h_{ie} are in parallel, so the total current I drawn from the supply is,

$$I = \frac{-V_o}{[X_{L_2} + X_C] + [X_{L_1} \| h_{ie}]} \qquad \ldots (2)$$

Negative sign, as current direction shown in opposite to the polarities of V_o.

Now $$X_{L_2} + X_C = j\omega L_2 + \frac{1}{j\omega C}$$

and $$X_{L_1} \| h_{ie} = \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}$$

Substituting in the equation (2) we get,

$$I = \frac{-h_{fe} I_b j\omega L_2}{\left[j\omega L_2 + \frac{1}{j\omega C}\right] + \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}} \qquad \ldots (3)$$

Replacing $j\omega$ by s,

$$I = \frac{-s h_{fe} I_b L_2}{\left[s L_2 + \frac{1}{sC}\right] + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2}{\frac{[1+s^2 L_2 C]}{sC} + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2 (sC)(s L_1 + h_{ie})}{[1+s^2 L_2 C][s L_1 + h_{ie}] + (sC)(s L_1 h_{ie})}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s L_1 + h_{ie} + s^2 L_2 C h_{ie} + s^2 L_1 C h_{ie}}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s^2 C h_{ie}(L_1 + L_2) + s L_1 + h_{ie}}$$

According to current division in parallel circuit,

$$I_b = I \times \frac{X_{L_1}}{XL_1 + h_{ie}}$$

$$= I \times \frac{j\omega L_1}{(j\omega L_1 + h_{ie})}$$

$$I_b = I \times \left[\frac{sL_1}{(sL_1 + h_{ie})}\right] \qquad \ldots (4)$$

Substituting value of I from equation (3) in (4),

$$I_b = \frac{-s^2 h_{fe} I_b L_2 C(sL_1 + h_{ie})}{[s^3(L_1 L_2 C) + s^2 C\, h_{ie}(L_1 + L_2) + sL_1 + h_{ie}]} \times \frac{sL_1}{(sL_1 + h_{ie})}$$

$$= \frac{-s^3 h_{fe} I_b C L_1 L_2}{s^3(L_1 L_2 C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 h_{ie}}$$

$$\therefore \quad 1 = \frac{-s^3 h_{fe} C L_1 L_2}{s^3(L_1 L_2 C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 + h_{ie}} \qquad \ldots (5)$$

Substituting $s = j\omega$, $s^2 = -\omega^2$, $s^3 = -j\omega^3$ we get

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C - \omega^2 C h_{ie}(L_1 + L_2) + j\omega L_1 + h_{ie}}$$

$$= \frac{j\omega^3 h_{ie} C L_1 L_2}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)] + j\omega L_1 (1 - \omega^2 L_2 C)} \qquad \ldots (6)$$

Rationalising the R.H.S of the above equation,

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2 [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2) - j\omega L_1 (1 - \omega^2 L_2 C)]}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2}$$

$$= \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C) + j\omega^3 h_{fe} L_1 L_2 C\,[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_1^2 L_2 C)^2} \qquad \ldots (7)$$

To satisfy this equation, imaginary part of R. H. S. must be zero.

$$\therefore \ \omega^3 h_{fe} L_1 L_2 C\, [h_{ie} - \omega^2 h_{ie} C\,(L_1 + L_2)] = 0$$

$$\therefore \ \omega^3 h_{fe} h_{ie} L_1 L_2 C\, [1 - \omega^2 C\,(L_1 + L_2)] = 0$$

$$\therefore \quad 1 - \omega^2 C\,(L_1 + L_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{C(L_1 + L_2)}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{C(L_1 + L_2)}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}} \qquad \ldots (8)$$

This is the frequency of the oscillations. At this frequency, the restriction of the value of h_{fe} can be obtained, by equating the magnitudes of the both sides of the equation (7).

$$\therefore \quad 1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C(1-\omega^2 L_2 C)}{0+\omega^2 L_1^2 (1-\omega^2 L_2 C)^2} \text{ at } \omega = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{(1-\omega^2 L_2 C)} \text{ at } \omega = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{\left[1-\frac{L_2 C}{C(L_1+L_2)}\right]} = \frac{h_{fe} L_2}{L_1}$$

$$\therefore \quad \boxed{h_{fe} = \frac{L_1}{L_2}} \quad \text{... (9)}$$

This is the value of h_{fe}, required to satisfy the oscillating conditions.

For a mutual inductance of M,

$$\boxed{h_{fe} = \frac{L_1+M}{L_2+M}} \quad \text{... (10)}$$

Now $L_1 + L_2$ is the equivalent inductance of the two inductances L_1 and L_2, connected in series denoted as

$$\boxed{L_{eq} = L_1 + L_2} \quad \text{... (11)}$$

Hence the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{C L_{eq}}}} \quad \text{... (12)}$$

Key Point: *So if the capacitor C is kept variable, frequency can be varied over a large range as per the requirement.*

In practice, L_1 and L_2 may be wound on a single core so that there exists a mutual inductance between them denoted as M.

In such a case, the mutual inductance is considered while determining the equivalent inductance L_{eq}. Hence,

$$\boxed{L_{eq} = L_1 + L_2 + 2M} \quad \text{... (13)}$$

If L_1 and L_2 are assisting each other then sign of 2M is positive while if L_1 and L_2 are in series opposition then sign of 2M is negative.

The expression for the frequency of the oscillations remain same as given by (12).

A practical circuit where the mutual inductance exists between L_1 and L_2, of transistorised Hartley oscillator is shown in the Fig. 4.30.

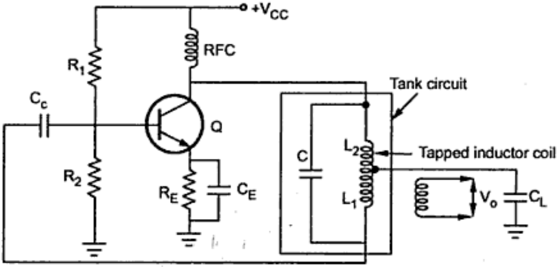


Fig. 4.32 Another form of transistorised Hartley oscillator

Key Point : *The Hartley oscillators are widely used in the radio receivers as local oscillators.*

Example 4.6 : *In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied.*

Solution : The frequency is given by,

$$f = \frac{1}{2\pi\sqrt{C(L_{eq})}}$$

where $L_{eq} = L_1 + L_2 = 2\times10^{-3} + 20\times10^{-6} = 0.00202$

For $f = f_{max} = \mathbf{2050\ kHz}$

$$2050\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}}$$

$\therefore$ $C = \mathbf{2.98\ pF}$

For $f = f_{min} = \mathbf{950\ kHz}$

$$950\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}}$$

$\therefore$ $C = \mathbf{13.89\ pF}$

Hence C must be varied from 2.98 pF to 13.89 pF, to get the required frequency variation.

4.9.3 FET Hartley Oscillator

If FET is used as an active device in an amplifier stage, then the circuit is called FET Hartley oscillator. The practical circuit is shown in the Fig. 4.33.

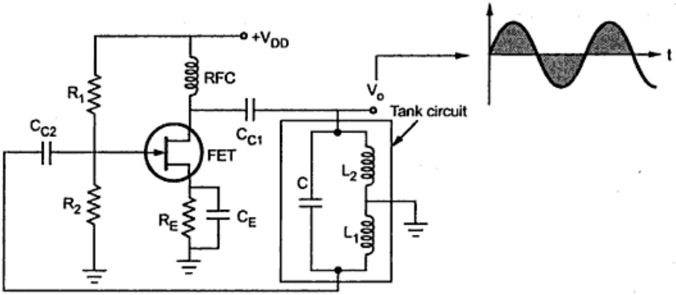


Fig. 4.33 FET Hartley oscillator

The resistances R_1, R_2 bias the FET along with R_s. The C_s in the source bypass capacitor. To maintain Q point stable, coupling capacitors C_{C1}, C_{C2} are used. These have very large values compared to capacitor C. The tank circuit is shown in a box.

We know,

$$X_1 + X_2 + X_3 = 0$$

And $$X_1 = j\omega L_1,\ X_2 = j\omega L_2 \text{ and } X_3 = \frac{1}{j\omega C}$$

Solving for ω, we get the same expression for the frequency as derived earlier.

$$\boxed{f = \frac{1}{2\pi\sqrt{C\,L_{eq}}}}$$

where $$\boxed{L_{eq} = L_1 + L_2 \text{ or } L_1 + L_2 + 2\,M}$$

This is dependent on whether L_1, L_2 are wound on the same core or not.

If $L_1 = L_2 = L$, then the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{2}\sqrt{LC}}} \quad \text{... (14)}$$

➠ **Example 4.7 :** *Calculate the frequency of oscillations of a Hartley oscillator having* $L_1 = 0.5\ mH$, $L_2 = 1\ mH$ *and* $C = 0.2\ \mu F$.

Solution : The given values are,

$$L_1 = 0.5\ \text{mH}, \quad L_2 = 1\ \text{mH}, \quad C = 0.2\ \mu\text{F}$$

Now $$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

and $$L_{eq} = L_1 + L_2 = 0.5 + 1 = 1.5\ \text{mH}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{1.5\times10^{-3}\times0.2\times10^{-6}}} = \mathbf{9.19\ kHz}$$

4.10 Colpitts Oscillator

An LC oscillator which uses two capacitive reactances and one inductive reactance in the feedback network i.e. tank circuit, is called **Colpitts oscillator.**

4.10.1 Transistorised Colpitts Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 4.34.

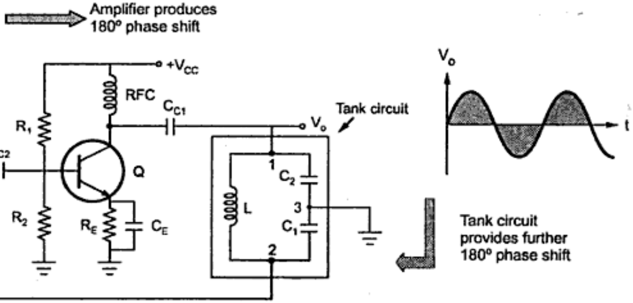

Amplifier produces
180° phase shift
+V_{CC}
RFC
C_{C1}
R_1
C_{C2}
Q
R_2
R_E
C_E
V_o
Tank circuit
L
1
C_2
3
C_1
2
V_o
t
Tank circuit
provides further
180° phase shift

Fig. 4.34 Transistorised Colpitts oscillator

The basic circuit is same as transistorised Hartley oscillator, except the tank circuit. The common emitter amplifier causes a phase shift of 180°, while the tank circuit adds further 180° phase shift, to satisfy the oscillating conditions.

4.10.2 Derivation of Frequency of Oscillations

As seen earlier, the output current I_c which is $h_{fe}\ I_b$ acts as input to the feedback network. While the base current I_b acts as the output current of the tank circuit, flowing through the input impedance of the amplifier h_{ie}. The equivalent circuit of the tank circuit is shown in the Fig. 4.35.

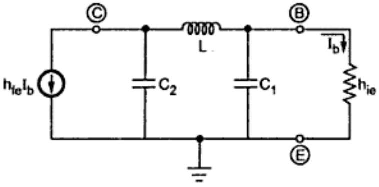


Fig. 4.35 Equivalent circuit

Converting the current source into the voltage source. We get the equivalent circuit as shown in the Fig. 4.36.

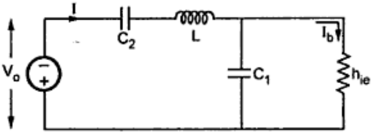


Fig. 4.36 Simplified equivalent circuit

$$V_o = h_{fe}\, I_b\, X_{C_2} = h_{fe}\, I_b \frac{1}{j\omega C_2} \qquad \text{...(1)}$$

The total current I, drawn from the supply is,

$$I = \frac{-V_o}{[X_{C_2} + X_L] + [X_{C_1} \parallel h_{ie}]} \qquad \text{... (2)}$$

The negative sign is because the current direction is assumed in the opposite direction to that, would be due to the polarities of V_o.

Now $$X_{C2} + X_L = \frac{1}{j\omega C_2} + j\omega L$$

and $$X_{C1} \parallel h_{ie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\left[\frac{1}{j\omega C_1} + h_{ie}\right]}$$

Substituting in the equation (4.79),

$$\therefore \qquad I = \frac{-h_{fe}\, I_b\left(\frac{1}{j\omega C_2}\right)}{\left[\frac{1}{j\omega C_2}+j\omega L\right]+\left[\frac{\frac{h_{ie}}{j\omega C_1}}{h_{ie}+\frac{1}{j\omega C_1}}\right]} \qquad \ldots (3)$$

Replacing jω by s,

$$\therefore \qquad I = \frac{-h_{fe}\, I_b\left(\frac{1}{s C_2}\right)}{\left[\frac{1}{s C_2}+s L\right]+\left[\frac{\frac{h_{ie}}{s C_1}}{h_{ie}+\frac{1}{s C_1}}\right]}$$

$$= \frac{-h_{fe}\, I_b\left(\frac{1}{s C_2}\right)}{\frac{(1+s^2 L C_2)}{s C_2}+\left[\frac{h_{ie}}{1+s C_1 h_{ie}}\right]}$$

$$= \frac{-h_{fe}\, I_b\left(\frac{1}{s C_2}\right)(s C_2)(1+s C_1 h_{ie})}{(1+s^2 L C_2)(1+s C_1 h_{ie})+s C_2 h_{ie}}$$

$$= \frac{-h_{fe}\, I_b\,(1+s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie}+s^2 L C_2+s C_1 h_{ie}+1+s C_2 h_{ie}}$$

$$= \frac{-h_{fe}\, I_b\,(1+s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie}+s^2 L C_2+s h_{ie}(C_1+C_2)+1} \qquad \ldots (4)$$

According to the current division in the parallel circuit,

$$I_b = I\times\frac{X_{C_1}}{(X_{C1}+h_{ie})} = \frac{I\times\frac{1}{j\omega C_1}}{\left(h_{ie}+\frac{1}{j\omega C_1}\right)}$$

$$\therefore \qquad I_b = \frac{I}{(1+s\, h_{ie}\, C_1)} \qquad \ldots (5)$$

Substituting value of I from the equation (4), in (5), we get

$$= \frac{-h_{fe}\, I_b\, (1+s\, C_1\, h_{ie})}{s^3\, L\, C_1\, C_2\, h_{ie} + s^2\, L C_2 + s\, h_{ie}\, (C_1 + C_2) + 1} \times \frac{1}{(1+s\, C_1\, h_{ie})}$$

$$= \frac{-h_{fe}\, I_b}{s^3\, L\, C_1\, C_2\, h_{ie} + s^2\, L C_2 + s\, h_{ie}\, (C_1 + C_2) + 1}$$

$$\therefore \quad 1 = \frac{-h_{fe}}{s^3\, L\, C_1\, C_2\, h_{ie} + s^2\, L C_2 + s\, h_{ie}\, (C_1 + C_2) + 1} \quad \text{... (6)}$$

Replacing s by $j\omega$, and s^2 by $-\omega^2$ and s^3 by $-j\omega^3$

$$\therefore \quad 1 = \frac{-h_{fe}}{-j\omega^3\, L\, C_1\, C_2\, h_{ie} - \omega^2\, L C_2 + j\omega h_{ie}\, (C_1 + C_2) + 1}$$

$$= \frac{-h_{fe}}{(1-\omega^2\, L\, C_2) + j\omega h_{ie}\, [C_1 + C_2 - \omega^2\, L\, C_1\, C_2]} \quad \text{... (7)}$$

There is no need to rationalize this as there are no j terms in the numerator, as in the equation (6 of 4.10.2).

It can be seen that, to satisfy the equation, the imaginary part of the denominator of the right hand side must be zero.

$$\therefore \quad \omega\, h_{ie}\, [C_1 + C_2 - \omega^2\, L\, C_1\, C_2] = 0$$

$$\therefore \quad C_1 + C_2 - \omega^2\, L\, C_1\, C_2 = 0$$

$$\therefore \quad \omega^2 = \frac{(C_1 + C_2)}{L\, C_1\, C_2} = \frac{1}{L\left[\frac{C_1\, C_2}{(C_1 + C_2)}\right]}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L\left[\frac{C_1\, C_2}{(C_1 + C_2)}\right]}}}$$

Now $\frac{C_1\, C_2}{C_1 + C_2}$ is nothing but the equivalent of two capacitors C_1 and C_2 in series.

$$\therefore \quad \boxed{C_{eq} = \frac{C_1\, C_2}{C_1 + C_2}}$$

$$\therefore \qquad \boxed{\omega = \frac{1}{\sqrt{L\,C_{eq}}}} \qquad \ldots(8)$$

$$\therefore \qquad \boxed{f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}} \qquad \ldots(9)$$

This is the frequency of the oscillations in the Colpitts oscillator.

Substituting this frequency in the equation (7) and equating the magnitudes of the both sides, the restriction on the value of h_{fe} can be obtained as,

$$\boxed{h_{fe} = \frac{C_2}{C_1}} \qquad \ldots(10)$$

Thus the behaviour of Colpitts oscillator is similar to the Hartley oscillator, as basic LC oscillator circuit is same, except the tank circuit.

Key Point: *The Colpitts oscillator is very commonly used as local oscillator in superheterodyne radio receiver.*

4.10.3 Colpitts Oscillator using FET

If in the basic circuit of Colpitts oscillator, the FET is used as an active device in the amplifier stage, the circuit is called as FET Colpitts oscillator. The tank circuit remains same as before. The working of the circuit and oscillating fequency also remains the same.

The practical circuit of FET Colpitts oscillator is shown in the Fig. 4.37.

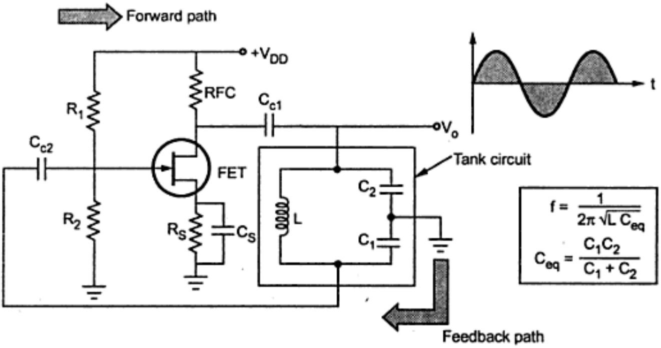


Fig. 4.37 FET Colpitts oscillator

Example 4.8 : *Find the frequency of the oscillations of transistorised Colpitts oscillator having tank circuit parameters as $C_1 = 150$ pF, $C_2 = 1.5$ nF and $L = 50$ μH.*

Solution : The equivalent capacitance is given by,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{150\times10^{-12}\times1.5\times10^{-9}}{150\times10^{-12}+1.5\times10^{-9}}$$

$$= 136.363\times10^{-12} \text{ F}$$

Now
$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$= \frac{1}{2\pi\sqrt{50\times10^{-6}\times136.363\times10^{-12}}}$$

$$= \mathbf{1.927\ MHz}$$

Example 4.9 : *In a Colpitts oscillator, $C_1 = C_2 = C$ and $L = 100$ μH. The frequency of oscillations is 500 kHz. Determine value of C.*

Solution : The given values are,

$$L = 100\ \mu\text{H},\ C_1 = C_2 = C \text{ and } f = 500 \text{ kHz}$$

Now
$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\therefore \quad 500\times10^3 = \frac{1}{2\pi\sqrt{100\times10^{-6}\times C_{eq}}}$$

$$\therefore \quad (500\times10^3)^2 = \frac{1}{4\pi^2\times100\times10^{-6}\times C_{eq}}$$

$$\therefore \quad C_{eq} = 1.0132\times10^{-9} \text{ F}$$

but
$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \quad \text{and} \quad C_1 = C_2 = C$$

$$\therefore \quad C_{eq} = \frac{C\times C}{C+C} = \frac{C}{2}$$

$$\therefore \quad 1.0132\times10^{-9} = \frac{C}{2}$$

$$\therefore \quad C = 2.026\times10^{-9}\text{ F} = \mathbf{2.026\text{ nF}}$$

4.11 Clapp Oscillator

To achieve the frequency stability, Colpitts oscillator circuit is slightly modified in practice, called Clapp oscillator. The basic tank circuit with two capacitive reactances and one inductive reactance remains same. But the modification in the tank circuit is that one more capacitor C_3 is introduced in series with the inductance as shown in the Fig. 4.38.

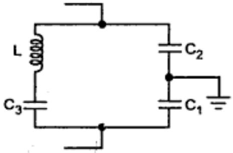


Fig. 4.38 Modified tank circuit

The value of C_3 is much smaller than the values of C_1 and C_2. Now the equivalent capacitance becomes,

$$\frac{1}{C_{eq}} = \frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3} \quad \text{... (1)}$$

While the oscillator frequency is given by the same expression as,

$$\boxed{f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}} \quad \text{... (2)}$$

Suppose $C_1 = C_2 = 0.001\ \mu F$, $L = 15\ \mu H$ and the new capacitor $C_3 = 50$ pF

$$\text{so,} \quad \frac{1}{C_{eq}} = \frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}$$

$$\therefore \quad C_{eq} = 4.545\times10^{-11}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}$$

$$= \frac{1}{2\pi\sqrt{15\times10^{-6}\times4.545\times50\times10^{-11}}}$$

$$= 6.09\text{ MHz}$$

If C_1 and C_2 are neglected then $C_{eq} = C_3$

$$\therefore \qquad f = \frac{1}{2\pi\sqrt{L\,C_3}} = \frac{1}{2\pi\sqrt{15\times10^{-6}\times50\times10^{-12}}} = 5.82 \text{ MHz}$$

The frequencies are almost same, hence in practice the C_1, C_2 values are neglected and C_3 is assumed to be C_{eq}. Hence the frequency is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{L\,C_3}}} \qquad \ldots (3)$$

Now across C_3, there is no transistor parameter and hence the frequency of the Clapp oscillator is stable and accurate. The transistor and stray capacitances have no effect on C_3 hence good frequency stability is achieved in Clapp oscillator. Hence practically Clapp oscillator is preferred over Colpitts oscillator. The transistorised Clapp oscillator is shown in the Fig. 4.39.

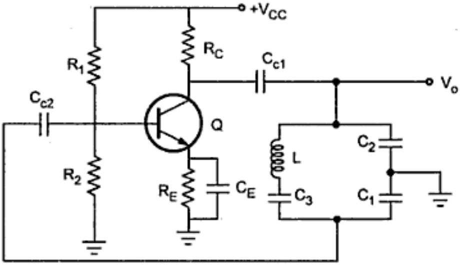


Fig. 4.39 Transistorised Clapp oscillator

Another advantage of C_3 is that it can be kept variable. As frequency is dependent on C_3, the frequency can be varied in the desired range.

4.11.1 Derivation of Frequency of Oscillations

The derivation is similar to the Colpitts oscillator with C_3 in series with L in the equivalent circuit of transistorised Clapp oscillator. The equivalent circuit is shown in the Fig. 4.40.

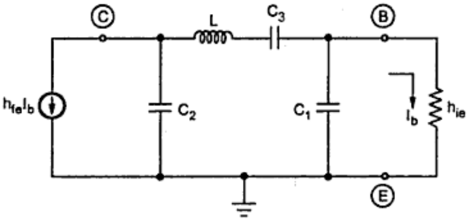


Fig. 4.40

Converting current source to voltage source we get the equivalent circuit as shown in the Fig. 4.41.

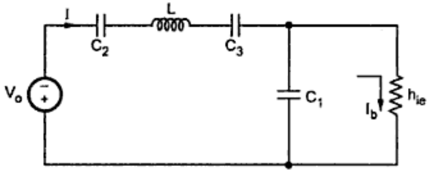


Fig. 4.41

$$V_o = h_{fe}\, I_b\, X_{C_2}$$

$$= h_{fe}\, I_b \cdot \frac{1}{j\omega C_2} \qquad \ldots (4)$$

$$\therefore \qquad I = \frac{-V_o}{[X_{C_2} + X_{C_3} + X_L] + [X_{C_1} \| h_{ie}]} \qquad \ldots (5)$$

The negative sign as the direction of I is assumed opposite to that which voltage source will force the current I through the circuit.

$$X_{C_2} + X_{C_3} + X_L = \frac{1}{j\omega C_2} + \frac{1}{j\omega C_3} + j\omega L$$

$$X_{C_1} \| h_{ie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\frac{1}{j\omega C_1} + h_{ie}}$$

$$\therefore \qquad I = \frac{-h_{fe} I_b \cdot \frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2}+\frac{1}{j\omega C_3}+j\omega L+\left[\frac{\frac{1}{j\omega C_1} h_{ie}}{\frac{1}{j\omega C_1}+h_{ie}}\right]} \qquad \ldots(6)$$

Replacing $j\omega$ by s,

$$I = \frac{-h_{fe}\, I_b \cdot \frac{1}{s\, C_2}}{\frac{1}{s\, C_2}+\frac{1}{s\, C_3}+sL+\left[\frac{\frac{h_{ie}}{s\, C_1}}{\frac{1}{s\, C_1}+h_{ie}}\right]} \qquad \ldots (7)$$

$$= \frac{-h_{fe}\, I_b}{1+\frac{C_2}{C_3}+s^2\, L\, C_2+\frac{s\, C_2\, h_{ie}}{(1+s\, C_1\, h_{ie})}} \qquad \text{...multiplying by } sC_2 \text{ to denominator}$$

$$= \frac{-h_{fe}\, I_b \cdot C_3}{C_3+C_2+s^2\, L\, C_2\, C_3+\frac{s\, C_2\, C_3\, h_{ie}}{(1+s\, C_1\, h_{ie})}}$$

$$= \frac{-h_{fe}\, I_b\, C_3\, (1+s\, C_1\, h_{ie})}{\begin{array}{l} C_3+sC_1\, C_3\, h_{ie}+C_2+sC_1\, C_2\, h_{ie}+s^2\, L\, C_2\, C_3 \\ +s^3\, L\, C_1\, C_2\, C_3\, h_{ie}+s\, C_2\, C_3\, h_{ie} \end{array}}$$

$$\therefore \qquad I = \frac{-h_{fe}\, I_b\, C_3\, (1+s\, C_1\, h_{ie})}{\begin{array}{l} s^3\, LC_1\, C_2\, C_3\, h_{ie}+s^2\, LC_2\, C_3 \\ +s\, h_{ie}\, [C_2\, C_3+C_1 C_2+C_1 C_3]+C_2+C_3 \end{array}} \qquad \ldots (8)$$

$$\therefore \qquad I_b = I \times \frac{X_{C_1}}{X_{C_1}+h_{ie}} = \frac{I \times \frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1}+h_{ie}} = \frac{I \times \frac{1}{sC_1}}{\frac{1}{sC_1}+h_{ie}}$$

$$\therefore \qquad I_b = \frac{I}{(1+s\, C_1\, h_{ie})} \qquad \ldots (9)$$

Substituting I,

$$I_b = \frac{-h_{fe}\, I_b\, C_3\, (1+s\, C_1\, h_{ie})}{\begin{array}{l} s^3\, L\, C_1\, C_2 C_3\, h_{ie}+s^2\, L\, C_2\, C_3 \\ +s\, h_{ie}\, [C_2\, C_3+C_1\, C_2+C_1\, C_3]+C_2+C_3 \end{array}} \times \frac{1}{(1+s\, C_1\, h_{ie})}$$

$$\therefore \qquad 1 = \frac{-h_{fe} C_3}{\begin{array}{l} s^3 L C_1 C_2 C_3 h_{ie} + s^2 L C_2 C_3 \\ + s h_{ie} [C_1 C_2 + C_2 C_3 + C_3 C_1] + C_2 + C_3 \end{array}}$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = -j\omega^3$

$$1 = \frac{-h_{fe} C_3}{\begin{array}{l} -j\omega^3 L C_1 C_2 C_3 h_{ie} - \omega^2 L C_2 C_3 \\ + j\omega h_{ie} [C_1 C_2 + C_2 C_3 + C_3 C_1] + C_2 + C_3 \end{array}}$$

$$\therefore \quad 1 = \frac{-h_{fe} C_3}{C_2 + C_3 - \omega^2 L C_2 C_3 + j\omega h_{ie} \{[C_1 C_2 + C_2 C_3 + C_3 C_1] - \omega^2 L C_1 C_2 C_3\}} \qquad \text{... (10)}$$

As there is no imaginary part in numerator, to satisfy Barkhausen criterion, imaginary part in the denominator must be zero. But ω and h_{ie} are not zero hence,

$$\therefore \quad C_1C_2 + C_2C_3 + C_3C_1 - \omega^2 L C_1 C_2 C_3 = 0$$

$$\therefore \qquad \omega^2 = \frac{C_1 C_2 + C_2 C_3 + C_3 C_1}{L C_1 C_2 C_3}$$

$$\therefore \qquad \omega^2 = \frac{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}{L} = \frac{\frac{1}{C_{eq}}}{L}$$

$$\therefore \qquad \omega^2 = \frac{1}{L C_{eq}}$$

$$\therefore \qquad \boxed{\omega = \frac{1}{\sqrt{L C_{eq}}}} \qquad \text{... (11)}$$

$$\therefore \qquad \boxed{f = \frac{1}{2\pi\sqrt{L C_{eq}}}} \qquad \text{... (12)}$$

where $\dfrac{1}{C_{eq}} = \dfrac{1}{C_1} + \dfrac{1}{C_2} + \dfrac{1}{C_3}$

But as $C_3 << C_1$ and C_2, $C_{eq} = C_3$

$$\therefore \qquad \boxed{f = \frac{1}{2\pi\sqrt{L C_3}}} \qquad \text{... (13)}$$

This is the required frequency of oscillations for the Clapp oscillator.

4.11.2 Advantages

1. The frequency is stable and accurate.
2. The good frequency stability.
3. The stray capacitances have no effect on C_3 which decides the frequency.
4. Keeping C_3 variable, frequency can be varied in the desired range.

4.12 Frequency Stability of Oscillator

For an oscillator, the frequency of the oscillations must remain constant. The analysis of the dependence of the oscillating frequency on the various factors like stray capacitance, temperature etc. is called as the frequency stability analysis.

The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long a time as possible is called frequency stability of an oscillator.

In a transistorised Colpitts oscillator or Hartley oscillator, the base-collector junction is reverse biased and there exists an internal capacitance which is dominant at high frequencies. This capacitance affects the value of capacitance in the tank circuit and hence the oscillating frequency.

Similarly the transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. Hence practically the circuits cannot provide stable frequency.

In general following are the factors which affect the frequency stability of an oscillator :

1. Due to the changes in temperature, the values of the components of tank circuit get affected. So changes in the values of inductors and capacitors due to the changes in the temperature is the main cause due to which frequency does not remain stable.
2. Due to the changes in temperature, the parameters of the active device used like BJT, FET get affected which inturn affect the frequency.
3. The variation in the power supply is another factor affecting the frequency.
4. The changes in the atmospheric conditions, aging and unstable transistor parameters affect the frequency.
5. The changes in the load connected, affect the effective resistance of the tank circuit.
6. The capacitive effect in transistor and stray capacitances, affect the capacitance of the tank circuit and hence the frequency.

The variation of frequency with temperature is given by the factor denoted as S.

$$\boxed{S_{\omega},T = \frac{\Delta\omega/\omega_r}{\Delta T/T_r} \text{ parts per million per } {}^{\circ}C} \quad \dots (1)$$

where ω_r = desired frequency

T_r = operating temperature

$\Delta\omega$ = change in frequency

ΔT = change in temperature

The frequency stability is defined as,

$$\boxed{S_\omega = \frac{d\theta}{d\omega}} \quad \ldots (2)$$

where $d\theta$ = phase shift introduced for a small frequency change in desired frequency f_r.

Key Point: *Larger the value of $d\theta/d\omega$, more stable is the oscillator.*

The frequency stability can be improved by the following modifications :

1. Enclosing the circuit in a constant temperature chamber.
2. Maintaining constant voltage by using the zener diodes.
3. The load effect is reduced by coupling the oscillator to the load loosely or with the help of a circuit having high input impedance and low output impedance.

4.13 Crystal Oscillators

The crystals are either naturally occurring or synthetically manufactured, exhibiting the **piezoelectric effect**. The piezoelectric effect means under the influence of the mechanical pressure, the voltage gets generated across the opposite faces of the crystal. If the mechanical force is applied in such a way to force the crystal to vibrate, the a.c. voltage gets generated across it. Conversely, if the crystal is subjected to a.c. voltage, it vibrates causing mechanical distortion in the crystal shape. Every crystal has its own resonating frequency depending on its cut. So under the influence of the mechanical vibrations, the crystal generates an electrical signal of very constant frequency. The crystal has a greater stability in holding the constant frequency. A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as its resonant tank circuit. The crystal oscillators are preferred when greater frequency stability is required. Hence the crystals are used in watches, communication transmitters and receivers etc.

The main substances exhibiting the piezoelectric effect are quartz, Rochelle salt and tourmaline. Rochelle salts have the greatest piezoelectric activity. For a given a.c. voltage, they vibrate more than quartz or tourmaline. Hence these are preferred in making microphones associated with portable tape recorders, headsets, loudspeakers etc. Rochelle salt is mechanically weakest of the three and break very easily. Tourmaline shows least piezoelectric effect but mechanically strongest. The tourmaline is most expensive and hence its use is rare in practice Quartz is a compromise between the piezoelectric activity of

Rochelle salts and the strength of the tourmaline. **Quartz** is inexpensive and easily available in nature and hence very commonly used in the crystal oscillators.

Key Point: *Quartz is widely used for RF oscillators and the filters.*

4.13.1 Constructional Details

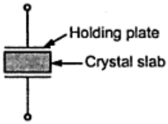


Fig. 4.42 Symbolic representation of a crystal

The natural shape of a quartz crystal is a hexagonal prism. But for its practical use, it is cut to the rectangular slab. This slab is then mounted between the two metal plates.

The symbolic representation of such a practical crystal is shown in the Fig. 4.42. The metal plates are called holding plates, as they hold the crystal slab in between them.

4.13.2 A.C. Equivalent Circuit

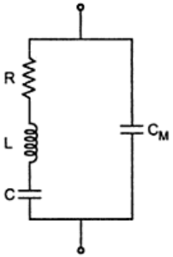


Fig. 4.43 A.C. equivalent circuit of a crystal

When the crystal is not vibrating, it is equivalent to a capacitance due to the mechanical mounting of the crystal. Such a capacitance existing due to the two metal plates separated by a dielectric like crystal slab, is called **mounting capacitance** denoted as C_M or C'.

When it is vibrating, there are internal frictional losses which are denoted by a resistance R. While the mass of the crystal, which is indication of its inertia is represented by an inductance L. In vibrating condition, it is having some stiffness, which is represented by a capacitor C. The mounting capacitance is a shunt capacitance. And hence the overall equivalent circuit of a crystal can be shown as in the Fig. 4.43.

RLC forms a resonating circuit. The expression for the resonating frequency f_r is,

$$\boxed{f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}}} \quad \text{... (1)}$$

Where Q = quality factor of crystal

$$\therefore \quad \boxed{Q = \frac{\omega L}{R}} \quad \text{... (2)}$$

The Q factor of the crystal is very high, typically 20,000. Value of Q upto 10^6 also can be achieved. Hence $\sqrt{\frac{Q^2}{1+Q^2}}$ factor approaches to unit and we get the resonating frequency as,

$$\boxed{f_r = \frac{1}{2\pi\sqrt{LC}}} \quad \text{... (3)}$$

The crystal frequency is infact inversely proportional to the thickness of the crystal.

$$\boxed{f \propto \frac{1}{t}}$$ where t = thickness

So to have very high frequencies, thickness of the crystal should be very small. But it makes the crystal mechanically weak and hence it may get damaged, under the vibrations. Hence practically crystal oscillators are used upto 200 or 300 kHz only.

The crystal has two resonating frequencies, series resonant frequency and parallel resonant frequency.

4.13.3 Series and Parallel Resonance

One resonant condition occurs when the reactances of series RLC leg are equal i.e. $X_L = X_C$. This is nothing but the series resonance. The impedance offered by this branch, under resonant condition is minimum which is resistance R. The series resonance frequency is same as the resonating frequency given by the equation (3).

$$\boxed{f_s = \frac{1}{2\pi\sqrt{LC}}} \quad \text{... (4)}$$

The other resonant condition occurs when the reactances of series resonant leg equals the reactance of the mounting capacitor C_M. This is parallel resonance or antiresonance condition.

Under this condition the impedance offered by the crystal to the external circuit is maximum.

Under parallel resonance, the equivalent capacitance is,

$$C_{eq} = \frac{C_M C}{C_M + C} \quad \text{... (5)}$$

Hence the parallel resonating frequency is given by,

$$\boxed{f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}} \quad \text{... (6)}$$

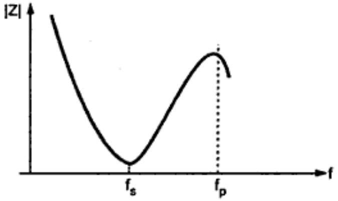


Fig. 4.44 (a) Crystal impedance versus frequency

When the crystal capacitance C is much smaller than C_M, then the Fig. 4.44 (a) shows the behaviour of crystal impedance versus frequency.

Generally values of f_s and f_p are very close to each other and practically it can be said that there exists only one resonating frequency for a crystal.

The higher value of Q is the main advantage of crystal. Due to high Q of a resonant circuit, it provides very good frequency stability.

If we neglect the resistance R, the impedance of the crystal is a reactance jX which depends on the frequency as,

$$jX = -\frac{j}{\omega C_M} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

where ω_s = series resonant frequency

ω_p = parallel resonant frequency

The sketch of reactance against frequency is shown in the Fig. 4.44 (b).

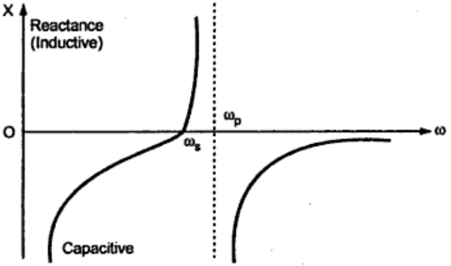


Fig. 4.44 (b) The reactance versus frequency

The oscillating frequency lies between ω_s and ω_p.

4.13.4 Crystal Stability

The frequency of the crystal tends to change slightly with time due to temperature, aging etc.

i) Temperature stability : It is defined as the change in the frequency per degree change in the temperature. This is Hz/MHz/°C. For 1°C change in the temperature, the frequency changes by 10 to 12 Hz in MHz. This is negligibly small. So for all practical purposes it is treated to be constant. But if this much change is also not acceptable then the crystal is kept in box where temperature is maintained constant, called constant temperature oven or constant temperature box.

ii) Long term stability : It is basically due to aging of the crystal material. Aging rates are 2×10^{-8} per year, for a quartz crystal. This is also negligibly small.

iii) Short term stability : In a quartz crystal, the frequency drift with time is, typically less than 1 part in 10^6 i.e. 0.0001° % per day. This is also very small.

Key Point : *Overall crystal has good frequency stability. Hence it is used in computers, counters, basic timing devices in electronic wrist watches, etc.*

4.13.5 Pierce Crystal Oscillator

The **Colpitts** oscillator can be modified by using the crystal to behave as an inductor. The circuit is called Pierce crystal oscillator. The crystal behaves as an inductor for a frequency slightly higher than the series resonance frequency f_s. The two capacitors C_1, C_2 required in the tank circuit along with an inductor are used, as they are used in **Colpitts** oscillator circuit. As only inductor gets replaced by the crystal, which behaves as an inductor, the basic working principle of Pierce crystal oscillator is same as that of **Colpitts** oscillator. The practical transistorised Pierce crystal oscillator circuit is shown in the Fig. 4.45.

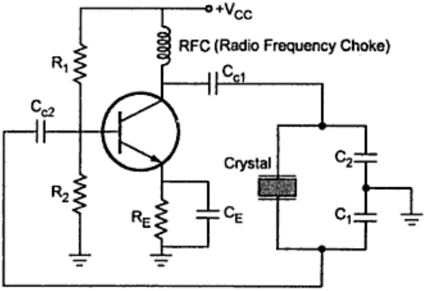
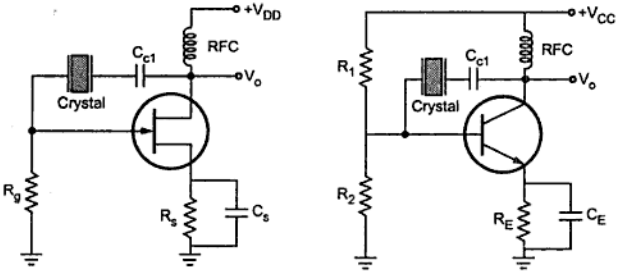


Fig. 4.45 Pierce crystal oscillator

The resistances R_1, R_2, R_E provide d.c. bias while the capacitor C_E is emitter bypass capacitor. RFC (Radio Frequency Choke) provides isolation between a.c. and d.c. operation. C_{c1} and C_{c2} are coupling capacitors.

The resulting circuit frequency is set by the series resonant frequency of the crystal, Change in the supply voltages, temperature, transistor parameters have no effect on the circuit operating conditions and hence good frequency stability is obtained.

The oscillator circuit can be modified by using the internal capacitors of the transistor used instead of C_1 and C_2. The separate capacitors C_1, C_2 are not required in such circuit. Such circuits using FET and transistor are shown in the Fig. 4.46 (a) and (b).



(a) Using FET **(b) Using Transistor**

Fig. 4.46 Pierce crystal oscillator

4.13.6 Miller Crystal Oscillator

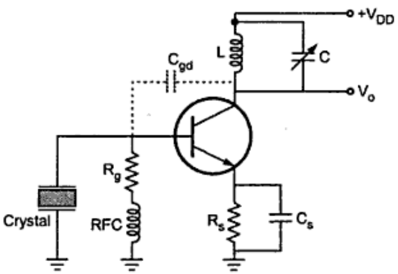


Fig. 4.47 Miller crystal oscillator

Similar to the modifications in Colpitts oscillator, the Hartley oscillator circuit can be modified, to get Miller crystal oscillator. In Hartley oscillator circuit, two inductors and one capacitor is required in the tank circuit. One inductor is replaced by the crystal which acts as an inductor for the frequencies slightly greater than the series resonant frequency. The transistorised Miller crystal oscillator circuit is shown in the Fig. 4.47.

The tuned circuit of L_1 and C is offtuned to behave as an inductor i.e. L_1. The crystal behaves as other inductance L_2 between base and ground. The internal capacitance of the transistor acts as a capacitor required to fulfill the elements of the tank circuit. The crystal decides the operating frequency of the oscillator.

➡ **Example 4.10 :** *A crystal L = 0.4 H, C = 0.085 pF and C_M = 1 pF with R = 5 kΩ. Find*

i) Series resonant frequency

ii) Parallel resonant frequency

iii) By what percent does the parallel resonant frequency exceed the series resonant frequency ?

iv) Find the Q factor of the crystal.

Solution : i)

$$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.4\times 0.085\times 10^{-12}}}$$

$$= \mathbf{0.856\ MHz}$$

ii)

$$C_{eq} = \frac{CC_M}{C+C_M} = \frac{0.085\times 1}{0.085+1} = 0.078 \text{ pF}$$

$$\therefore \quad f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.4\times 0.078\times 10^{-12}}} = \mathbf{0.899\ MHz}$$

iii)

$$\%\text{ increase} = \frac{0.899-0.856}{0.856}\times 100 = \mathbf{5.023\ \%}$$

iv)

$$Q = \frac{\omega_s L}{R} = \frac{2\pi f_s L}{R} = \frac{2\pi\times 0.856\times 10^6\times 0.4}{5\times 10^3}$$

$$= \mathbf{430.272}$$

➡ **Example 4.11 :** *A crystal has L = 2 H, C = 0.01 pF and R = 2 kΩ. Its mounting capacitance is 2 pF. Calculate its series and parallel resonating frequency.*

Solution :

$$C_M = 2 \text{ pF}$$

Now

$$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{\sqrt{2\times 0.01\times 10^{-12}}} = \mathbf{1.125\ MHz}$$

$$C_{eq} = \frac{C_M C}{C_M + C} = \frac{2\times 10^{-12}\times 0.01\times 10^{-12}}{2\times 10^{-12}+0.01\times 10^{-12}} = 9.95\times 10^{-15} \text{ F}$$

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{\sqrt{2\times 9.95\times 10^{-15}}}$$

$$= \mathbf{1.128\ MHz}$$

So f_s and f_p values are almost same.

Examples with Solutions

Example 4.12 : *In a certain oscillator circuit, the gain of the amplifier is* $\left[\frac{-16\times10^{6}}{j\omega}\right]$ *and the feedback factor of the feedback network is* $\frac{10^{3}}{[2\times10^{3}+j\omega]^{2}}$*. Verify the Barkhausen Criterion for the sustained oscillations. Also find the frequency at which circuit will oscillate.*

Solution : From the given information we can write,

$$A = -\frac{16\times10^{6}}{j\omega} \text{ and } \beta = \frac{10^{3}}{[2\times10^{3}+j\omega]^{2}}$$

To verify the Barkhausen condition means to verify whether $|A\beta| = 1$ at a frequency for which $\angle A\beta = 0°$. Let us express, $A\beta$ in its rectangular form.

$$A\beta = -\frac{16\times10^{6}\times10^{3}}{j\omega[2\times10^{3}+j\omega]^{2}} = -\frac{16\times10^{9}}{j\omega[4\times10^{6}+4\times10^{3}j\omega+(j\omega)^{2}]}$$

$$= -\frac{16\times10^{9}}{j\omega\left[4\times10^{6}+j\omega4\times10^{3}-\omega^{2}\right]} \quad \text{as } j^{2} = -1$$

$$= -\frac{16\times10^{9}}{4\times10^{6}\,j\omega+j^{2}\omega^{2}\,4\times10^{3}-j\omega^{3}}$$

$$= -\frac{16\times10^{9}}{j\omega[4\times10^{6}-\omega^{2}]-[\omega^{2}\times4\times10^{3}]}$$

Rationalising the denominator function we get,

$$A\beta = -\frac{16\times10^{9}\,[-4\times10^{3}\,\omega^{2}-j\omega(4\times10^{6}-\omega^{2})]}{\{(-4\times10^{3}\,\omega^{2})+j\omega(4\times10^{6}-\omega^{2})\}\{-(4\times10^{3}\,\omega^{2})-j\omega(4\times10^{6}-\omega^{2})\}}$$

Using $(a + b)(a - b) = a^{2} - b^{2}$ in the denominator,

$$A\beta = \frac{+16\times10^{9}\,[4\times10^{3}\,\omega^{2}+j\omega(4\times10^{6}-\omega^{2})]}{(-4\times10^{3}\,\omega^{2})^{2}-[j\omega(4\times10^{6}-\omega^{2})]^{2}}$$

$$= \frac{16\times10^{9}\,[4\times10^{3}\,\omega^{2}+j\omega(4\times10^{6}-\omega^{2})]}{16\times10^{6}\;\omega^{4}+\omega^{2}\,(4\times10^{6}-\omega^{2})^{2}}$$

Now to have $\angle A\beta = 0°$, the imaginary part of $A\beta$ must be zero. This is possible when,

$$\therefore \quad \omega(4\times10^6-\omega^2) = 0$$

$$\therefore \quad \omega = 0 \text{ or } 4\times10^6-\omega^2 = 0$$

$$\therefore \quad \omega^2 = 4\times10^6 \qquad \text{Neglecting zero value of frequency}$$

$$\therefore \quad \omega = \mathbf{2\times10^3 \text{ rad/sec}}$$

At this frequency $|A\beta|$ can be obtained as,

$$|A\beta| = \frac{16\times10^9\,[4\times10^3\,\omega^2]}{16\times10^6\ \ \omega^4+\omega^2\,(4\times10^6-\omega^2)^2} \quad \text{at } \omega = 2\times10^3$$

$$= \frac{16\times10^9\,[4\times10^3\times4\times10^6]}{16\times10^6\times16\times10^{12}+4\times10^6\,[4\times10^6-4\times10^6]^2}$$

$$= \frac{2.56\times10^{20}}{2.56\times10^{20}+0} = \mathbf{1}$$

$\therefore$ At $\omega = 2\times10^3$ rad/sec, $\angle A\beta = 0°$ as imaginary part is zero while $|A\beta| = 1$. Thus Barkhausen Criterion is satisfied.

The frequency at which circuit will oscillate is the value of ω for which $|A\beta| = 1$ and $\angle A\beta = 0°$ at the same time

i.e. $\quad \omega = 2\times10^3$ rad/sec.

But $\quad \omega = 2\pi f$

$$\therefore \quad f = \frac{\omega}{2\pi} = \frac{2\times10^3}{2\pi} = \mathbf{318.309 \text{ Hz}}$$

Example 4.13 : *The frequency sensitive arms of the Wien bridge oscillator uses $C_1 = C_2 = 0.001\ \mu F$ and $R_1 = 10\ k\Omega$ while R_2 is kept variable. The frequency is to be varied from 20 kHz to 70 kHz by varying R_2. Find the minimum and maximum values of R_2.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

For $\quad f = 20$ kHz,

$$20\times10^3 = \frac{1}{2\pi\sqrt{10\times10^3\times R_2\times(0.001\times10^{-6})^2}}$$

$$\therefore \quad R_2 = \mathbf{6.33\ k\Omega}$$

For $\quad f = 70$ kHz

$$70 \times 10^3 = \frac{1}{2\pi\sqrt{10\times10^3\times R_2\times(0.001\times10^{-6})^2}}$$

$$\therefore \quad R_2 = \mathbf{0.516\ k\Omega}$$

So minimum value of R_2 is 0.516 kΩ while the maximum value of R_2 is 6.33 kΩ.

➠ **Example 4.14 :** *For phase shift oscillator, the feedback network uses R = 6 kΩ and C = 1500 pF. The transistorised amplifier used, has a collector resistance of 18 kΩ. Calculate the frequency of oscillations and minimum value of h_{fe} of the transistor.*

Solution : R = 6 kΩ, C = 1500 pF, R_C = 18 kΩ

Now $$K = \frac{R_C}{R} = \frac{18}{6} = 3$$

$$\therefore \quad f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$$= \frac{1}{2\pi\times6\times10^3\times1500\times10^{-12}\sqrt{6+12}}$$

$$= \mathbf{4.168\ kHz}$$

$$(h_{fe})_{min} = 4K + 23 + \frac{29}{K}$$

$$= 4 \times 3 + 23 + \frac{29}{3}$$

$$= \mathbf{44.67}$$

➠ **Example 4.15 :** *In a Wien bridge oscillator $R_1 = R_2 = 100$ kΩ and the ganged variable capacitor has a range from 50 pF to 500 pF. Find the range of the frequency of the oscillations possible.*

If the frequency desired is 50 kHz more than the maximum frequency calculated above, find the value of the resistance to be connected in parallel with 100 kΩ.

Solution : For a Wien bridge oscillator,

$$f = \frac{1}{2\pi RC}$$

$$\therefore \quad f_{max} = \frac{1}{2\pi\times100\times10^3\times50\times10^{-12}}$$

$$= \mathbf{31.83\ kHz}$$

and $$f_{min} = \frac{1}{2\pi\times100\times10^3\times500\times10^{-12}}$$

$$= \textbf{3.183 kHz}$$

Now $$f_{new} = f_{max} + 50 \times 10^3 = 31.83 \times 10^3 + 50 \times 10^3$$

$$= \textbf{81.83 kHz}$$

The corresponding R = R′ with an additional resistance R_x in parallel.

$$\therefore \quad f = \frac{1}{2\pi R'C}$$

$$\therefore \quad 81.83 \times 10^3 = \frac{1}{2\pi R' \times 50 \times 10^{-12}}$$

$$\therefore \quad R' = 38.89 \text{ K}\Omega$$

$$\therefore \quad R' = \frac{R \times R_x}{R + R_x}$$

$$\therefore \quad 38.89 = \frac{100 R_x}{100 + R_x}$$

$$\therefore \quad R_x = \textbf{63.64 k}\boldsymbol{\Omega} \qquad \text{... in parallel with 100 k}\Omega$$

Example 4.16 : *A Hartley oscillator circuit has C = 500 pF, L_1 = 20 mH and L_2 = 5 mH. Find the frequency of oscillations.*

Solution : For a Hartley oscillator the frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} \qquad \text{where } L_{eq} = L_1 + L_2$$

$$\therefore \quad L_{eq} = 20 + 5$$

$$= 25 \text{ mH}$$

$$\therefore \quad f = \frac{2}{2\pi\sqrt{25 \times 10^{-3} \times 500 \times 10^{-12}}}$$

$$= \textbf{45.01 kHz}$$

Example 4.17 : *In a Hartley Oscillator, L_1 = 15 mH and C = 50 pF. Calculate L_2 for a frequency of 168 kHz. The mutual inductance between L_1 and L_2 is 5 μH. Also find the required gain of the transistor to be used for the oscillations.*

Solution : For a Hartley oscillator,

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} \qquad \text{where } L_{eq} = L_1 + L_2 + 2M$$

$$\therefore \quad 168\times10^{3} = \frac{1}{2\pi\sqrt{L_{eq}\times50\times10^{-12}}}$$

$$\therefore \quad L_{eq} = 17.95 \text{ mH}$$

$$\therefore \quad 17.95\times10^{-3} = 15\times10^{-3}+L_2+5\times10^{-6}$$

$$\therefore \quad L_2 = \mathbf{2.945 \text{ mH}}$$

Now

$$h_{fe} = \frac{L_1+M}{L_2+M}$$

$$= \frac{15\times10^{-3}+5\times10^{-6}}{2.945\times10^{-3}+5\times10^{-6}}$$

$$= \mathbf{5.08}$$

Example 4.18 : *A Colpitts oscillator is shown in the Fig. 4.48. What is approximate frequency ? What will be the new frequency if the value of L is doubled ? What should be the inductance, to double the frequency ?*

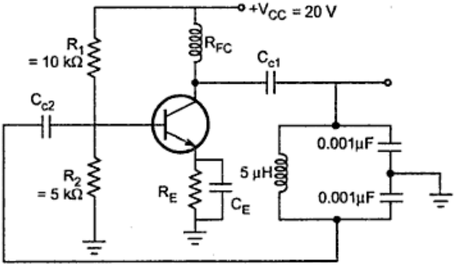


Fig. 4.48

Solution : For a Colpitts oscillator,

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}$$

where

$$C_{eq} = \frac{C_1C_2}{C_1+C_2} \text{ but } C_1 = C_2 = 0.001\ \mu\text{F}$$

$$\therefore \quad C_{eq} = \frac{0.001\times10^{-6}\times0.001\times10^{-6}}{0.001\times10^{-6}+0.001\times10^{-6}} = 5\times10^{-10}\text{ F}$$

$$L = 5\times10^{-6}\ \text{H}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{5\times10^{-6}\times5\times10^{-10}}} = \mathbf{3.183\ MHz}$$

Now L is doubled i.e. 10 μH

$$\therefore \quad f = \frac{1}{2\pi\sqrt{10\times10^{-6}\times5\times10^{-10}}} = \mathbf{2.25\ MHz}$$

$$\text{New frequency} = 2\times 3.183 = 6.366\ \text{MHz}$$

$$\therefore \quad 6.366\times10^{6} = \frac{1}{2\pi\sqrt{L\times5\times10^{-10}}}$$

$$\therefore \quad L = \mathbf{1.25\ \mu H}$$

Example 4.19 : *In the above problem if 63 pF capacitor is connected in series with 5 μH inductor, to make it as Clapp oscillator. What is the new frequency of oscillation ?*

Solution : For a Clapp oscillator,

$$f = \frac{1}{2\pi\sqrt{LC_3}}$$

where $C_3 = 63$ pF

$$\therefore \quad f = \frac{1}{2\pi\sqrt{5\times10^{-6}\times63\times10^{-12}}}$$

$$= \mathbf{8.967\ MHz}$$

Example 4.20 : *Find the resistance R and h_{fe} for the transistor to provide a resonating frequency of 5 kHz of a transistorised phase shift oscillator. The biasing resistance are 25 kΩ and 47 kΩ. The load resistance is 10 kΩ. The capacitor in the tank circuit is 1000 pF while h_{ie} of the transistor is 2 kΩ.*

Solution : Referring to equation (1) of section 4.5.3, the input impedance is given by,

$$R_i' = R_1 \parallel R_2 \parallel h_{ie}$$

Now $R_1 = 25\ \text{k}\Omega,\ R_2 = 47\ \text{k}\Omega,\ \text{and}\ h_{ie} = 2\ \text{k}\Omega$

$$\therefore \quad R_i' = \frac{1}{\frac{1}{25\times10^{3}}+\frac{1}{47\times10^{3}}+\frac{1}{2\times10^{3}}}$$

$$= 1.7816\ \text{k}\Omega$$

$$K = \frac{R_C}{R}$$

Now $R_C = 10\ \text{k}\Omega$ ...given

Now $$f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$\therefore$ $$5 \times 10^3 = \frac{1}{2\pi R \times 1000 \times 10^{-12} \times \sqrt{6+4K}}$$

$\therefore$ $$R\sqrt{6+4K} = 31830.989$$

Now $$K = \frac{R_C}{R} = \frac{10 \times 10^3}{R}$$

$\therefore$ $$R\sqrt{6+\frac{4 \times 10 \times 10^3}{R}} = 31830.989$$

$\therefore$ $$R^2\left(6+\frac{40 \times 10^3}{R}\right) = (31830.989)^2$$

$\therefore$ $$R^2\frac{[6R+40 \times 10^3]}{R} = (31830.989)^2$$

$$6R^2 + 40 \times 10^3 R - (31830.989)^2 = 0$$

$\therefore$ $$R = \frac{-40 \times 10^3 \pm \sqrt{(40 \times 10^3)^2 + 4 \times 6 \times (31830.989)^2}}{2 \times 6}$$

$= \mathbf{16.74\ k\Omega}$ Neglecting negative value

$\therefore$ $$K = \frac{R_C}{R} = \frac{10}{16.74} = \mathbf{0.5973}$$

$\therefore$ $$h_{fe} \geq 4K + 23 + \frac{29}{K}$$

$$\geq 4 \times 0.5973 + 23 + \frac{29}{0.5973} \geq \mathbf{73.94}$$

Example 4.21 : *Calculate the component values of the Wien bridge suitable to be used in the oscillator to vary the frequency from 100 Hz to 10 kHz in the two ranges.*

Solution : The frequency is given by,

$$f = \frac{1}{2\pi RC}$$

Let the resistance value to be selected as,

$$R_1 = R_2 = R = 50\ \text{k}\Omega$$

$$f_{min} = \frac{1}{2\pi\times 50\times 10^3\times C}$$

$$C = \frac{1}{2\pi\times 50\times 10^3\times 100}$$

$$= \mathbf{31.83\ nF}$$

And $$f_{max} = \frac{1}{2\pi\times 50\times 10^3\times C}$$

$$C = \frac{1}{2\pi\times 50\times 10^3\times 10\times 10^3} = 318.31\ \text{pF}$$

$$= \mathbf{0.318\ nF}$$

Thus to vary the frequency from 100 Hz to 10 kHz, the capacitor range should be selected as 0.318 nF to 31.83 nF.

Similarly keeping the capacitor value constant, the range of the resistance values can be obtained.

Example 4.22 : *In Colpitts oscillator using FET, the frequency of oscillations is observed to be 2.5 MHz. Oscillator uses :* $L = 10\ \mu H$, $C_1 = 0.02\ \mu F$.

Find : i) Value of C_2 *ii) If L is doubled, the new value of frequency of oscillations.*

Solution : $f = 2.5$ MHz, $L = 10\ \mu$H, $C_1 = 0.02\ \mu$F

For Colpitts oscillator, the frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}$$

$$\therefore \quad 2.5\times 10^6 = \frac{1}{2\pi\sqrt{10\times 10^{-6}\times C_{eq}}}$$

$$\therefore \quad C_{eq} = 405.284\ \text{pF}$$

i) But $$C_{eq} = \frac{C_1\,C_2}{C_1+C_2}$$

$$\therefore \quad 405.284\times 10^{-12} = \frac{0.02\times 10^{-6}\ C_2}{0.02\times 10^{-6}+C_2}$$

$$\therefore \quad 0.02\times 10^{-6}+C_2 = 49.348\ C_2$$

$\therefore \qquad C_2 = \mathbf{0.4136\ nF}$

ii) $\qquad L = 2\times10 = 20\ \mu H$

and $\qquad C_{eq} = 405.284\ pF$

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{20\times10^{-6}\times405.284\times10^{-12}}}$$

$$= \mathbf{1.7677\ MHz}$$

Example 4.23 : *A crystal has L = 0.33 H, C = 0.065 pF and* C_M *= 1 pF with* $R = 5.5\ k\Omega$*. Find*

i) Series resonant frequency.

ii) Parallel resonant frequency.

iii) By what percent does the parallel resonant frequency exceed the series resonant frequency ?

iv) Find the Q factor of the crystal.

Solution : i)

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.33\times0.065\times10^{-12}}}$$

$$= \mathbf{1.087\ MHz}$$

ii)

$$C_{eq} = \frac{CC_M}{C+C_M} = \frac{0.065\times1}{0.065+1} = \mathbf{0.061\ pF}$$

$$\therefore \qquad f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.33\times0.061\times10^{-12}}}$$

$$= \mathbf{1.121\ MHz}$$

iii)

$$\%\ \text{increase} = \frac{1.121-1.087}{1.087}\times100 = \mathbf{3.127\ \%}$$

iv)

$$Q = \frac{\omega_x L}{R} = \frac{2\pi f_s L}{R}$$

$$= \frac{2\pi\times1.087\times10^6\times0.33}{5.5\times10^3}$$

$$= \mathbf{409.789}$$

➡ **Example 4.24 :** *A FET Hartley oscillator circuit uses coupled coils in the tank circuit, each with inductance of 0.1 mH and mutual inductance of 0.025 mH. The circuit uses a fixed capacitor of 100 pF in series with a variable capacitor of 100 pF (trimmer) :*

(i) Calculate % change in frequency when direction of coupling between coils is reversed, trimmer capacitance set to zero.

(ii) Repeat calculations in part (i) when trimmer capacitance is changed from 0 to 100 pF, assume any one direction of coupling.

Solution : $L_1 = 0.1$ mH, $L_2 = 0.1$ mH, M = 0.025 mH, C = 100 pF

(i) Assume one particular coupling direction for which,

$$L_{eq} = L_1 + L_2 + 2M = 0.25 \text{ mH}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L_{eq}\,C}} = \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times100\times10^{-12}}}$$

$$= 1.00658 \text{ MHz}$$

Let the direction of coupling is reversed,

$$L_{eq} = L_1 + L_2 - 2M = 0.15 \text{ mH}$$

$$\therefore \quad f' = \frac{1}{2\pi\sqrt{L_{eq}\,C}} = \frac{1}{2\pi\sqrt{0.15\times10^{-3}\times100\times10^{-12}}} = 1.2994 \text{ MHz}$$

$$\therefore \quad \% \text{ change} = \frac{f'-f}{f}\times 100 = \frac{1.2994-1.00658}{1.00658}\times100 = \mathbf{29.09\ \%}$$

(ii) Let us assume direction of coupling such that,

$$L_{eq} = L_1 + L_2 + 2M = 0.25 \text{ mH}$$

$$C_t = \text{Trim capacitor} = 100 \text{ pF}$$

$$\therefore \quad C_{eq} = \frac{C\times C_t}{C+C_t} = 50 \text{ pF}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L_{eq}\,C_{eq}}} = \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times50\times10^{-12}}}$$

$$= 1.4235 \text{ MHz}$$

If now direction of coupling is reversed,

$$L_{eq} = L_1 + L_2 - 2M = 0.15 \text{ mH}$$

$$\therefore \quad f' = \frac{1}{2\pi\sqrt{L_{eq}\, C_{eq}}} = \frac{1}{2\pi\sqrt{0.15\times10^{-3}\times50\times10^{-12}}}$$

$$= 1.83776 \text{ MHz}$$

$$\therefore \quad \% \text{ change} = \frac{f'-f}{f}\times 100 = \frac{1.83776-1.4235}{1.4235}\times100$$

$$= \mathbf{29.101\ \%}$$

Example 4.25 : *Design a RC phase shift oscillator to generate 5 kHz sine wave with 20 V peak to peak amplitude. Draw the designed circuit. Assume h_{fe} = 150.*

Solution : For RC phase shift oscillator,

$$h_{fe} = 4K + 23 + \frac{29}{K} \qquad \text{... given } h_{fe} = 150$$

$$\therefore \quad 150 = 4K + 23 + \frac{29}{K}$$

$$\therefore \quad 4K^2 - 127\,K + 29 = 0$$

$$\therefore \quad K = 31.52\ ,\ 0.23$$

$$f = \frac{1}{2\pi R C\sqrt{6+4K}} \qquad \text{... given f = 5 kHz}$$

$$\therefore \text{Choose} \quad C = 1000 \text{ pF}$$

$$\therefore \quad 5\times10^3 = \frac{1}{2\pi R\times1000\times10^{-12}\times\sqrt{6+4\times0.23}}$$

$$\therefore \quad R = 12.1 \text{ k}\Omega \approx \mathbf{12\ k\Omega}$$

$$K = \frac{R_C}{R} \quad \text{i.e. } R_C = KR = \mathbf{2.7\ k\Omega}$$

Neglecting effect of biasing resistances assuming them to be large and selecting transistor with h_{ie} = 2 kΩ ,

$$R_i' = h_{ie} = 2 \text{ k}\Omega$$

∴ Last resistance in phase shift network

$$R_3 = R - R_i' = 12 - 2 = \mathbf{10\ k\Omega}$$

Using the **back to back** connected zener diodes of 9.3 V (Vz) each at the output of emitter follower and using this at the output of the oscillator, the output amplitude can be controlled to 10 V i.e. 20 V peak to peak. The zener diode 9.3 V and forward biased diode of 0.7 V gives total 10 V.

The designed circuit is as shown in the Fig. 4.49.

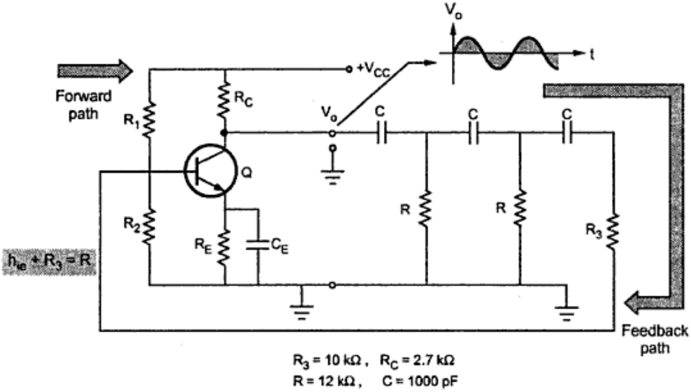

V_o
t
+V_CC
Forward path
R_1
R_C
V_o
C
C
C
Q
R
R
R_3
R_2
R_E
C_E
h_ie + R_3 = R
Feedback path
R_3 = 10 kΩ, R_C = 2.7 kΩ
R = 12 kΩ, C = 1000 pF

Fig. 4.49 Transistorised RC phase shift oscillator

Example 4.26 : *In a Hartley oscillator* $L_1 = 20\ \mu H$, $L_2 = 2\ mH$ *and C is variable. Find the range of C if frequency is to be varied from 1 MHz to 2.5 MHz. Neglect mutual inductance.*

Solution : $L_1 = 20\ \mu\text{H}$, $L_2 = 2\ \text{mH}$

$$\therefore \quad L_{eq} = L_1 + L_2 = 20\times10^{-6} + 2\times10^{-3} = 2.002\times10^{-3}\ \text{H}$$

For $f = f_{max} = 2.5$ MHz.

$$f = \frac{1}{2\pi\sqrt{C\times L_{eq}}}$$

$$\therefore \quad 2.5\times10^{6} = \frac{1}{2\pi\sqrt{C\times2.002\times10^{-3}}}$$

$$\therefore \quad C = \mathbf{2.0244\ pF}$$

For $f = f_{min} = 1$ MHz.

$$1\times10^{6} = \frac{1}{2\pi\sqrt{C\times2.002\times10^{-3}}}$$

$$\therefore \quad C = \mathbf{12.6525\ pF}$$

Thus C must be varied from 2.0244 pF to 12.6525 pF.

Example 4.27 : *A quartz crystal has the following constants, L = 50 mH, C_1 = 0.02 pF, R = 500 Ω and C_2 = 12 pF. Find the values of f_s and f_p. If the external capacitance across the crystal changes from 5 pF to 6 pF, find the change in frequency of oscillations.*

Solution : L = 50 mH, C_1 = 0.02 pF, R = 500 Ω, C_2 = 12 pF

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.02 \times 12 \times 10^{-12} \times 10^{-12}}{[0.02 + 12] \times 10^{-12}}$$

$$= 0.01996 \text{ pF}$$

$$\therefore \quad f_s = \frac{1}{2\pi\sqrt{L C_1}} = \frac{1}{2\pi\sqrt{50 \times 10^{-3} \times 0.02 \times 10^{-12}}}$$

$$= \mathbf{5.0329 \text{ MHz}}$$

and

$$f_p = \frac{1}{2\pi\sqrt{L C_{eq}}} = \frac{1}{2\pi\sqrt{50 \times 10^{-3} \times 0.01996 \times 10^{-12}}}$$

$$= \mathbf{5.0379 \text{ MHz}}$$

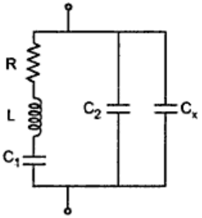


Fig. 4.50

Let C_s = 5 pF connected across the crystal.

$$\therefore \quad C_2' = C_2 + C_x$$

$$= 12 + 5$$

$$= 17 \text{ pF}$$

$$\therefore \quad C_{eq}' = \frac{C_1 C_2'}{C_1 + C_2'}$$

$$= 0.019976 \text{ pF}$$

$$\therefore \quad f_p' = \frac{1}{2\pi\sqrt{L C_{eq}'}}$$

$$= 5.03588 \text{ MHz}$$

New C_x = 6 pF is connected then,

$$C_2'' = C_2 + C_x = 12 + 6$$

$$= 18 \text{ pF}$$

$$\therefore \quad C_{eq}'' = \frac{C_1 C_2''}{C_1 + C_2''} = 0.0199778 \text{ pF}$$

$$\therefore \qquad f''_p = \frac{1}{2\pi\sqrt{L\,C''_{eq}}} = 5.035716 \text{ MHz}$$

$$\therefore \qquad \text{Change} = f'_p - f''_p = (5.03588 - 5.035716) \times 10^6$$

$$= \mathbf{164\ Hz}$$

Review Questions

1. *What is the Barkhausen criterion for the feedback oscillators?*
2. *Explain the classification of the feedback oscillators.*
3. *Classify various oscillators based on output waveforms circuit components, operating frequencies and feedback used.*
4. *Draw a neat circuit diagram of a phase shift oscillator using BJT. Derive an expression for its frequency of oscillations. Determine the minimum 'h_{fe}' for the transistor.*
5. *Draw the Wien bridge oscillator using BJT. Show that the gain of the amplifier must be at least 3 for the oscillations to occur.*
6. *Why the negative feedback is incorporated in the Wien bridge oscillator circuit ?*
7. *What is the type of feedback incorporated in the Wien bridge oscillator circuit ? Explain its working.*
8. *Discuss and explain the basic circuit of an LC oscillator and derive the condition for the oscillations.*
9. *Why the LC oscillators are not suitable for low frequency applications. ? Explain the principle of working of basic LC oscillators.*
10. *Write the short notes on :*
    - *a. LC oscillators* *b. RC oscillators*
    - *c. Colpitts Oscillator* *d. Hartley Oscillator*
11. *Explain the working of Heratley Oscillator. Derive the formula for the frequency.*
12. *Derive an expression for frequency of oscillation of Hartley oscillator using BJT.*
13. *Derive an expression for frequency of oscillation of Hartley oscillator using transistor.*
14. *Explain the working of Colpitts Oscillator. State the formula for the frequency.*
15. *Derive an expression for frequency of oscillation of transistorized Colpitts oscillator..*
16. *Why are RC oscillators preferred for the generation of low frequencies ?*
17. *Derive an expression for the frequency of oscillations of RC-phase shift oscillators using BJT.*
18. *Explain the working of Clapp Oscillator.*
19. *What is Piezoelectric effect ? Draw and explain a.c. equivalent circuit of a crystal.*
20. *What is Piezoelectric effect ? Explain the working of Crystal Oscillator.*

21. *How frequency stability can be improved in the oscillators ?*

22. *What are the factors that affect the frequency stability of an oscillator. How frequency stability can be improved in oscillators.*

23. *Explain the working of Pierce crystal oscillator.*

24. *Explain the working of Miller crystal oscillator.*

25. *Where does the starting voltage for an oscillator come from ?*

26. *Find C and* h_{fe} *of a transistor to provide a resonating frequency of 10 kHz of a transistor phase shift oscillator.* $R_1 = 24\ \text{k}\Omega$, $R_2 = 68\ \text{k}\Omega$, $R_C = 18\ \text{k}\Omega$, $R = 6.8\ \text{k}\Omega$ *and* $h_{ie} = 2\ \text{k}\Omega$.

    (Ans. : 575 pF, ≥ 44.543)

27. *A crystal has* $L = 0.1$ H, $C = 0.01$ pF, $R = 10\ \text{K}\Omega$ *and* $C_M = 1$ pF. *Find*

    a. Series resonance frequency b. Q factor **(Ans. : 5.03 MHz, 5.05 MHz, 316.04)**

28. *In a Colpitts oscillator* $C_1 = 0.00\ \mu F$ *and* $C_1 = 0.01\ \mu F$ *and* $L = 5\ \mu H$

    a. Calculate frequency of oscillations. b. If L is doubled, find the new frequency.

    c. Find L, to double the frequency in (a). **(Ans. : 2.36 MHz, 1.67 MHz, 1.25 μH)**

29. *A crystal oscillator has* $L = 0.4$ H, $C = 0.085$ pF *and Mounting capacitance* $C_M = 1$ pF *with* $R = 5\ \text{k}\Omega$. *Find series and parallel resonant frequencies. By what percent does the parallel resonant frequencies. By what percent does the parallel resonant frequency exceed the series resonant frequency ? Also find the Q-factor of the crystal.*

30. *What type of feedback is employed in oscillators ? And what are its advantages ? Discuss the conditions for sustaining oscillations.*

31. *Find the capacitor C and* h_{fe} *for the transistor to provide a resonating frequency of 10 kHz of transistorized phase-shift oscillator. Assume* $R_1 = 25\ \text{k}\Omega$, $R_2 = 60\ \text{k}\Omega$, $R_C = 40\ \text{k}\Omega$, $R = 7.1\ \text{k}\Omega$ *and* $h_{fe} = 1.8\ \text{k}\Omega$

□□□

5

Combinational Logic Circuits

5.1 Introduction

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called **combinational logic**. In combinational logic, the output variables are at all times dependent on the combination of input variables.

A combinational circuit consists of input variables, logic gates, and output variables. The logic gates accept signals from the input variables and generate output signals. This process transforms binary information from the given input data to the required output data. Fig. 5.1 shows the block diagram of a combinational circuit. As shown in Fig. 5.1, the combinational circuit accepts n-input binary variables and generates output variables depending on the logical combination of gates.

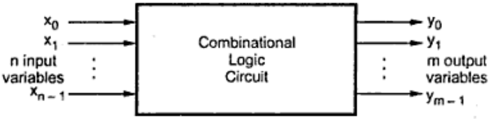


Fig. 5.1 Block diagram of a combinational circuit

In the combinational circuit, let X be the set of n input variables $\{x_0, x_1, \ldots, x_{n-1}\}$, and Y be the set of m output variables $\{y_0, y_1, \ldots, y_{m-1}\}$. The combinational function F, operate on the set X, to produce the output variable set, Y. The output is thus related to input as

$$Y = F(X)$$

5.2 Design Procedure

The design of combinational circuits starts from the outline of the problem statement and ends in a logic circuit diagram or a set of Boolean functions from which the logic diagram can be easily obtained. The design procedure of the combinational circuit involves following steps :

1. The problem definition.
2. The determination of number of available input variables and required output variables.
3. Assigning letter symbols to input and output variables.
4. The derivation of truth table indicating the relationships between input and output variables.
5. Obtain simplified Boolean expression for each output.
6. Obtain the logic diagram.

The Fig. 5.2 shows the sequence of design steps of combinational circuits.

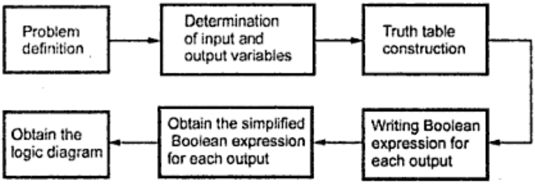

Problem definition
Determination of input and output variables
Truth table construction
Writing Boolean expression for each output
Obtain the simplified Boolean expression for each output
Obtain the logic diagram

Fig. 5.2 Typical combinational logic design sequence

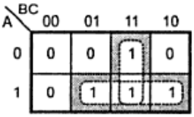
Example 5.1 : *Design a combinational logic circuit with three input variables that will produce a logic 1 output when more than one input variables are logic 1.*

Solution : Given problem specifies that there are three input variables and one output variable. We assign A, B and C letter symbols to three input variables and assign Y letter symbol to one output variable. The relationship between input variables and output variable can be tabulated as shown in truth Table 5.1.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 5.1 Truth table

Now we obtain the simplified Boolean expression for output variable Y using K-map simplification.



A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Fig. 5.3

$$\therefore \quad Y = AC + BC + AB$$

Logic diagram

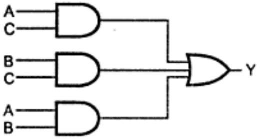


Fig. 5.4

In this chapter we are going to study various combinational circuits using above illustrated design method. This method of designing combinational logic circuits is a traditional method.

The traditional method of combinational circuit design involves simplification and realization of circuit using logic gates. This method of designing combinational circuit is effective for small circuit. When circuit complexity is more, more number of gates are required with more number of wires between them. Designing of such circuits may be time consuming and less reliable.

To avoid these problems several combinational circuits available in the integrated circuits are employed extensively in the design of digital systems. The integrated circuits can be classified using four levels of integration : small-(SSI), medium-(MSI), large-(LSI), and very large-(VLSI) scale integration. Most of the combinational circuits available in the integrated circuits are classified as MSI components. MSI components perform specific digital functions commonly needed in the design of digital systems, such as multiplexing, demultiplexing, addition, parity generation and checking, parity encoding, decoding, comparison, etc. MSI components significantly reduce IC package count thereby reducing the system cost. Along with the design simplification they reduce the number of external wire connections improving the reliability of the system.

In this chapter, we design some circuits using traditional design and then introduce some of LSI and MSI components such as adders, multiplexers, demultiplexers, decoders encoders and comparators to implement combinational circuits.

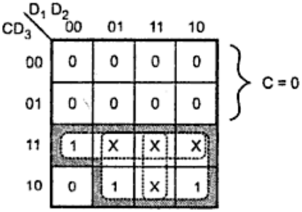
➡ **Example 5.2 :** *Design a cricuit that has one control line C and three data lines* D_1, D_2, D_3. *When the control line is high, the circuit is to detect when one of the data lines has a 1 on it. No more than one data line will ever have a 1 on it. When the control line is low, the circuit will output a 0, regardless of what is on the data lines.*

Solution : The truth table for the given problem is as shown below.

C	D_3	D_2	D_1	Output
0	x	x	x	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1

Table 5.2 Truth table for given problem

K-map simplification



$D_1 D_2$
CD_3
00
01
11
10
00
01
11
10
0 0 0 0
0 0 0 0
1 X X X
0 1 X 1
C = 0

Fig. 5.5

$\therefore$ $$Y = CD_3 + CD_2 + CD_1$$

Logic diagram

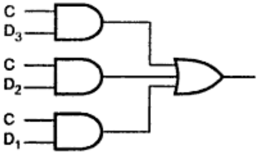


Fig. 5.6

Example 5.3 : *Design a combinational circuit that multiplies by 5 an input decimal digit represented in BCD. The output is also in BCD. Show that the outputs can be obtained from the input lines without using any logic gates.*

Solution : Truth table

Input				Output							
Decimal Digit				Digit 1				Digit 0			
A	B	C	D	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	1	0	1
0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	1	0	1	0	1
0	1	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0	0	0	0
0	1	1	1	0	0	1	1	0	1	0	1
1	0	0	0	0	1	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	1	0	1

Here, $Y_0 = D$, $Y_1 = 0$, $Y_2 = D$, $Y_3 = 0$, $Y_4 = C$, $Y_5 = B$, $Y_6 = A$ and $Y_7 = 0$. Therefore, the given circuit can be obtained from the input lines without using any **logic gates.**

➠ **Example 5.4 :** *Fig. 5.7 shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition and the head lights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following condition exists :*

The headlights are ON while the ignition is OFF.

The door is open while the ignition is ON.

Implement the logic circuit using only NAND gates. (See Fig. 5.7 on next page).

Solution : Let us consider D for Door, I for Ignition, L for Light. Then conditions to activate the alarm are :

1. The headlights are ON while the ignition is OFF.
   i.e. L = 1 I = 0 and D may be anything.
2. The door is open while the ignition is ON
   i.e. D = 1, I = 1, L may be anything.

Also alarm will sound if logic circuit output is zero.

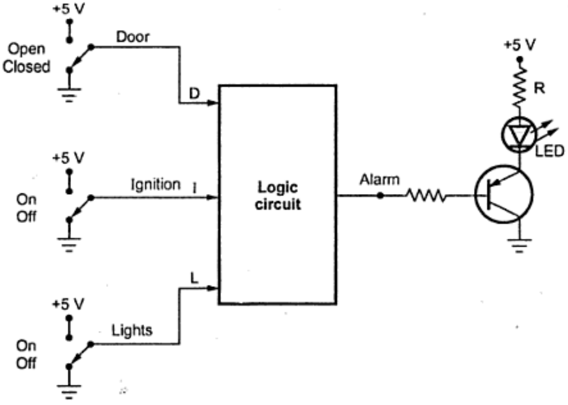

+5 V
Open
Closed
Door
D
+5 V
On
Off
Ignition
I
Logic circuit
Alarm
+5 V
R
LED
L
+5 V
Lights
On
Off

Fig. 5.7

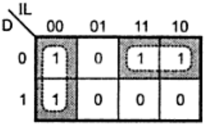
Therefore, output for above condition is zero and for rest of the condition it is 1 which is summarized in the following table.

D	I	L	Y
0	0	0	1
X	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	1	X	0

∴ K-map for logic circuit.

$$\text{Output} = Y = \bar{I}\,\bar{L} + \bar{D}\,I$$

As AND-OR logic can be directly replaced by NAND-NAND, logic circuit using only NAND gates is



D \ IL	00	01	11	10
0	1	0	1	1
1	1	0	0	0

Fig. 5.8

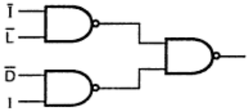

$\bar{I}$
$\bar{L}$
$\bar{D}$
I

Fig. 5.9 Inverted input replace with NAND

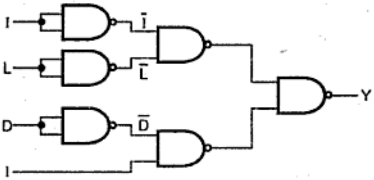


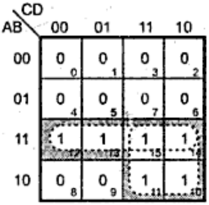
Fig. 5.10

Example 5.5 : *Design circuit to detect invalid BCD number and implement using NAND gate only.*

Solution : Truth table

Dec	A	B	C	D	Output Y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

K-map Simplification



AB \ CD	00	01	11	10
00	0_{0}	0_{1}	0_{3}	0_{2}
01	0_{4}	0_{5}	0_{7}	0_{6}
11	1_{12}	1_{13}	1_{15}	1_{14}
10	0_{8}	0_{9}	1_{11}	1_{10}

Y = AB + AC

Logic diagram

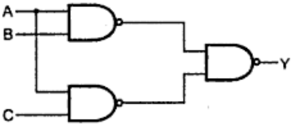


Fig. 5.11

AND-OR logic can be directly implemented by NAND-NAND logic.

Example 5.6 : *A panel light in the control room at the launching of a satellite is to go ON if and only if the pressure in both fuel and oxidizer tanks is equal to or above a required minimum and there are 10 minutes or less to lift off, or if the pressure in the oxidizer tank is equal to or above a required minimum and the pressure in fuel tank is below a required minimum but there are more than 10 minutes to lift off, or if the pressure in the oxidizer tank is below a required minimum but there are more than 10 minutes to lift off. Design a two level gate combinational circuit to control panel light.*

Solution :

Input 1 → Pressure in fuel tank

Input 2 → Pressure in oxidizer tank.

Input = 1 Indicates pressure is equal to or above the required minimum

= 0 Otherwise

Input 3 → From timer

if input 3 = 1 Indicates that there are less than or exactly 10 minutes for lift off.

= 0 Otherwise

Output → Panel light, if light goes on then

Output = 1,

else output = 0

Truth table

Let input 1 = A, input 2 = B, input 3 = C.

Inputs			Output
A	B	C	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

K-map simplification :

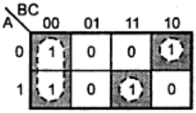


Fig. 5.12

$$\begin{aligned} y &= ABC+\overline{A}B\overline{C}+\overline{B}\,\overline{C} \\ &= ABC+\overline{C}\,(\overline{B}+\overline{A}B) \\ &= ABC+\overline{C}\,(\overline{B}+\overline{A}) && [\because \overline{A}+\overline{A}\,B = A+B] \\ &= ABC+\overline{C}\,(\overline{AB}) \\ &= \overline{AB\oplus C} \end{aligned}$$

Logic circuit :

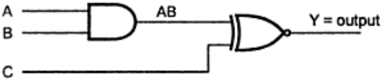


Fig. 5.13

5.3 Multiplexers

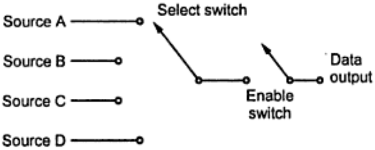
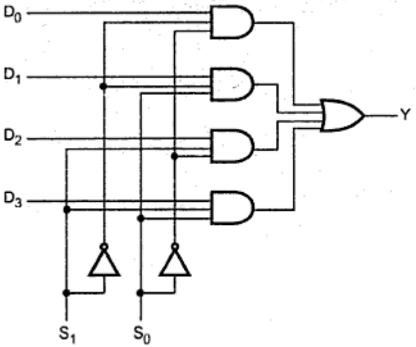


Fig. 5.14 Analog selector switch

Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single output line, as shown in the Fig. 5.14. The basic multiplexer has several data-input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

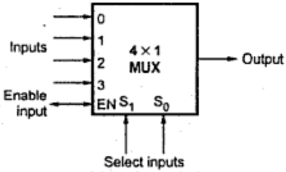
Fig. 5.15 (a) shows 4-to-1 line multiplexer. Each of the four lines, D_0 to D_3, is applied to one input of an AND gate. Selectiort lines are decoded to select a particular AND gate.



(a) Logic diagram

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

(b) Function table



(c) Logic symbol

Fig. 5.15 4 to 1 line multiplexer

For example, when $S_1S_0 = 0\ 1$, the AND gate associated with data input D_1 has two of its inputs equal to 1 and the third input connected to D_1. The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0. The OR gate output is now equal to the value of D_1, thus we can say data bit D_1 is routed to the output when $S_1\ S_0 = 0\ 1$.

In some cases, two or more multiplexers are enclosed within one IC package, as shown in the Fig. 5.16. The Fig. 5.16 shows quadruple 2 to 1 line multiplexer, i.e. four multiplexers, each capable of selecting one of two input lines. Output Y_1 can be selected to be equal to either A_1 or B_1. Similarly output Y_2 may have the value of A_2 or B_2, and so on. The selection line S selects one of two lines in all four multiplexers. The control input E enables the multiplexers in the 0 state and disables them in the 1 state. When E = 1, outputs have all 0's, regardless of the value of S. (See Fig. 5.16 on next page.)

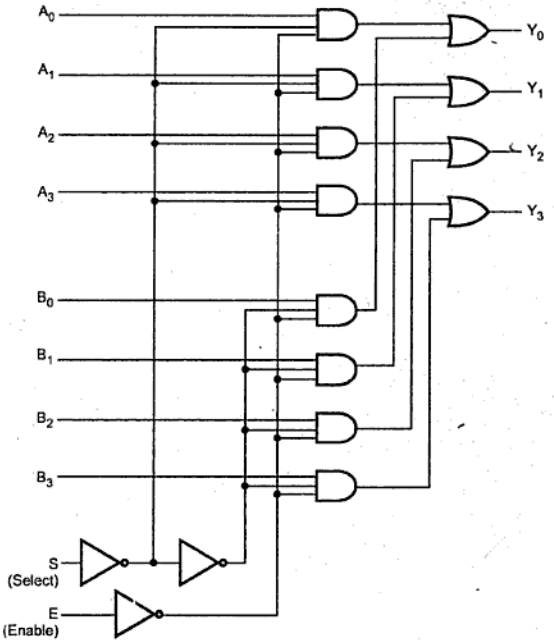


Fig. 5.16 Quadruple 2 to 1 line multiplexer

Function table

E	S	Output Y
1	X	All 0s
0	0	Select A
0	1	Select B

5.3.1 The 74XX151 8 to 1 Multiplexer

The 74XX151 is a 8 to 1 multiplexer. It has eight inputs. It provides two outputs, one is active high, the other is active low. The Fig. 5.17 shows the logic symbol for 74XX151. As shown in the logic symbol, there are three select inputs C, B and A which select one of the eight inputs. The 74XX151 is provided with active low enable input.

The Table 5.3 shows the truth table for 74XX151. In this truth table for each input combinations output is not specified in 1s and 0s. Because, we know that, multiplexer is a

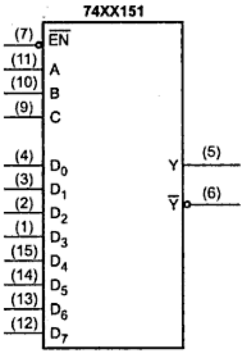

74XX151
(7)
$\overline{EN}$
(11)
A
(10)
B
(9)
C
(4)
D_0
(3)
D_1
(2)
D_2
(1)
D_3
(15)
D_4
(14)
D_5
(13)
D_6
(12)
D_7
Y
(5)
$\overline{Y}$
(6)

Fig. 5.17 Logic symbol for 74XX151, 8 to 1 multiplexer

data switch, it does not generate any data of its own, but it simply passes external input data from the selected input to the output. Therefore, the two output column represent data by D_n and $\overline{D}_n$.

Input				Outputs	
Select			Enable		
C	B	A	$\overline{EN}$	Y	$\overline{Y}$
x	x	x	1	0	1
0	0	0	0	D_0	$\overline{D}_0$
0	0	1	0	D_1	$\overline{D}_1$
0	1	0	0	D_2	$\overline{D}_2$
0	1	1	0	D_3	$\overline{D}_3$
1	0	0	0	D_4	$\overline{D}_4$
1	0	1	0	D_5	$\overline{D}_5$
1	1	0	0	D_6	$\overline{D}_6$
1	1	1	0	D_7	$\overline{D}_7$

Table 5.3 Truth table for 74XX151, 8 to 1 multiplexer

5.3.2 The 74XX157 Quad 2-Input Multiplexer

The IC 74XX157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common select input (S). The Enable input ($\bar{E}$) is active low. When $\bar{E}$ is high, all of the outputs (Y) are forced low regardless of all other input conditions.

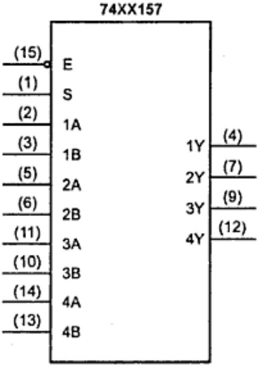


Fig. 5.18 Logic symbol for IC 74XX157

Moving data from two groups of register to four common output buses is a common use of IC 74XX157. The state of the select input determines the particular register from whih the data comes. Fig. 5.18 shows logic symbol for IC 74XX157.

The truth table for 74XX157 is shown in Table 5.4.

Inputs		Outputs			
$\bar{E}$	S	1Y	2Y	3Y	4Y
1	x	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

Table 5.4 Truth table for 74XX157

5.3.3 The 74XX153 Dual 4 to 1 Multiplexer

The 74XX153 is a dual 4 to 1 multiplexer. Fig. 5.19 shows the logic symbol for 74XX153. It contains two identical and independent 4 to 1 multiplexers. Each multiplexer has separate enable inputs. The Table 5.5 shows the truth table for 74XX153.

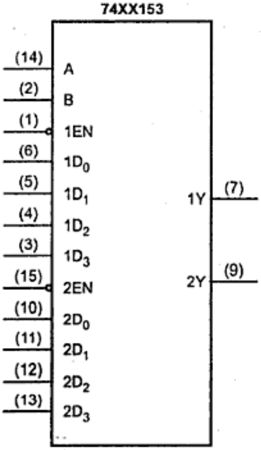

74XX153
(14) A
(2) B
(1) 1EN
(6) 1D0
(5) 1D1
(4) 1D2
(3) 1D3
(15) 2EN
(10) 2D0
(11) 2D1
(12) 2D2
(13) 2D3
1Y (7)
2Y (9)

Fig. 5.19 Logic symbol for 74XX153

Inputs				Outputs	
1EN	2EN	B	A	1Y	2Y
0	0	0	0	$1D_0$	$2D_0$
0	0	0	1	$1D_1$	$2D_1$
0	0	1	0	$1D_2$	$2D_2$
0	0	1	1	$1D_3$	$2D_3$
0	1	0	0	$1D_0$	0
0	1	0	1	$1D_1$	0

0	1	1	0	$1D_2$	0
0	1	1	1	$1D_3$	0
1	0	0	0	0	$2D_0$
1	0	0	1	0	$2D_1$
1	0	1	0	0	$2D_2$
1	0	1	1	0	$2D_3$
1	1	x	x	0	0

Table 5.5 Truth table for 74XX153, dual 4 to 1 multiplexer

5.3.4 Expanding Multiplexers

Several digital multiplexer ICs are available such as 74150 (16 to 1), 74151 (8 to 1), 74157 (Dual 2 input) and 74153 (Dual 4 to 1) multiplexer. It is possible to expand the range of inputs for multiplexer beyond the available range in the integrated circuits. This can be accomplished by interconnecting several multiplexers. For example, two 74XX151, 8 to 1 multiplexers can be used together to form a 16 to 1 multiplexer, two 74XX150, 16 to 1 multiplexers can be used together to form a 32 to 1 multiplexer and so on.

➠ **Example 5.7 :** *Design 32 to 1 multiplexer using two 74LS150.*

Solution : Fig. 5.20 shows a 32 to 1 multiplexer using two 74LS150 ICs.

See Fig. 5.20 on page 5 - 16.

➠ **Example 5.8 :** *Design 32 to 1 multiplexer using four 8 to 1 multiplexers and 2 to 4 decoder.*

Solution : Fig. 5.21 shows the 32 to 1 multiplexer using four 8 to 1 multiplexer and one 2 to 4 decoder.

See Fig. 5.21 on page 5 - 17.

5.3.5 Implementation of Combinational Logic using MUX

A multiplexer consists of a set of AND gates whose outputs are connected to single OR gate. (Refer Fig. 5.21). Because of this construction any Boolean function in a SOP form can be easily realized using multiplexer. Each AND gate in the multiplexer represents a minterm. In 8 to 1 multiplexer, there are 3 select inputs and 2^3 minterms. By connecting the function variables directly to the select inputs, a multiplexer can be made to select the AND gate that corresponds to the minterm in the function. If a minterm exists in a function, we have to connect the AND gate data input to logic 1; otherwise we have to connect it to logic 0. This is illustrated in the following example.

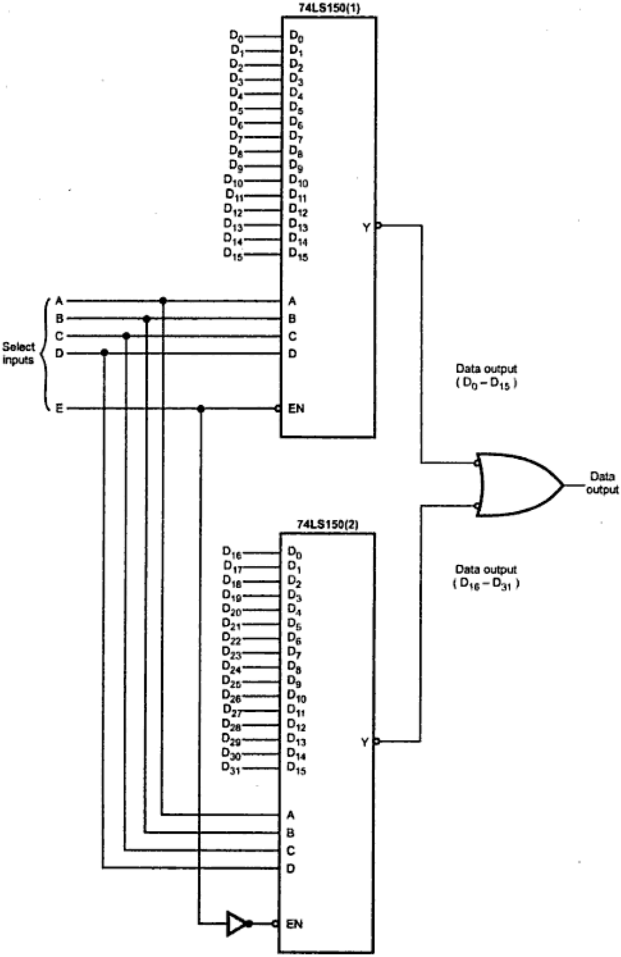

74LS150(1)
D0 – D15
A
B
C
D
E
Select inputs
EN
Y
Data output (D0 – D15)
Data output
74LS150(2)
D16 – D31
Data output (D16 – D31)

Fig. 5.20 32 to 1 multiplexer using two 74LS150 ICs

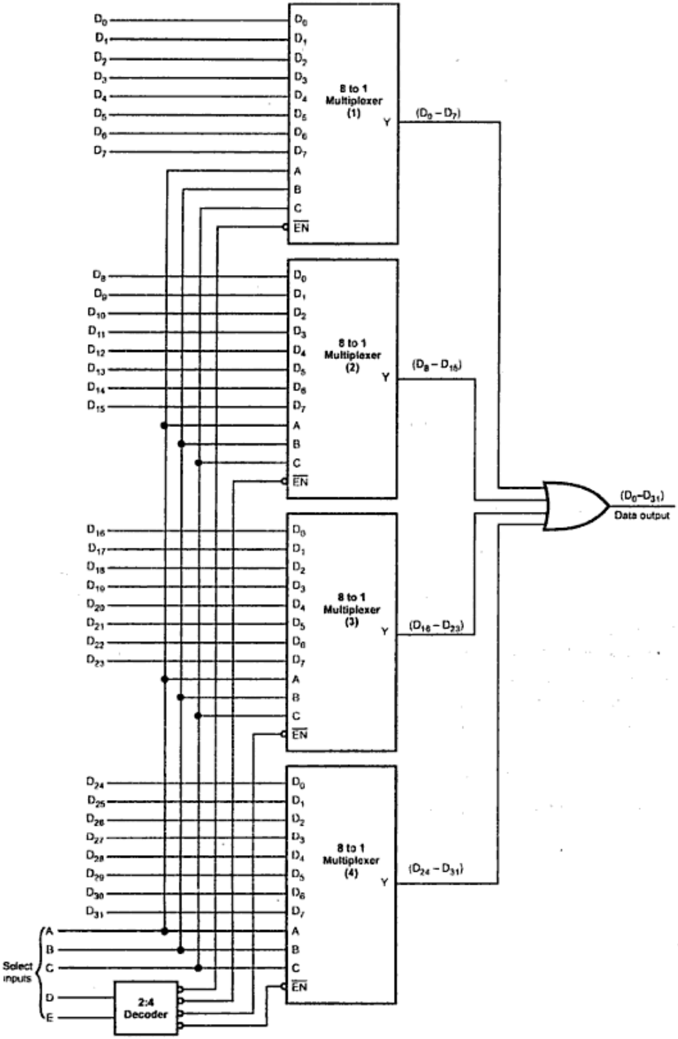

8 to 1
Multiplexer
(1)
8 to 1
Multiplexer
(2)
8 to 1
Multiplexer
(3)
8 to 1
Multiplexer
(4)
D_0 … D_{31}
A
B
C
$\overline{EN}$
Y
$(D_0 - D_7)$
$(D_8 - D_{15})$
$(D_{16} - D_{23})$
$(D_{24} - D_{31})$
$(D_0 - D_{31})$
Data output
Select inputs
D
E
2:4
Decoder

Fig. 5.21

Example 5.9 : *Implement the following Boolean function using 8 : 1 multiplexer.*

$$F(A, B, C) = \sum m\,(1, 3, 5, 6)$$

Solution : The function can be implemented with a 8 to 1 multiplexer, as shown in Fig. 5.22. Three variables A, B and C are applied to the select lines. The minterms to be included (1, 3, 5 and 6) are chosen by making their corresponding input lines equal to 1. Minterms 0, 2, 4 and 7 are not included by making their input lines equal to 0.

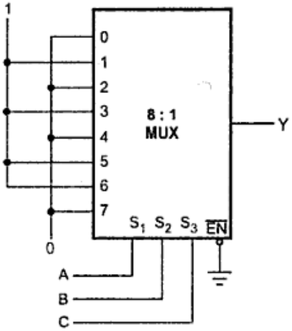


Fig. 5.22 Boolean function implementation using MUX

In the above example we have seen the method for implementing Boolean function of 3 variables with 2^3 (8) to 1 multiplexer. Similarly, we can implement any Boolean function of n variables with 2^n to 1 multiplexer. However, it is possible to do better than this. If we have Boolean function of n + 1 variables, we take n of these variables and connect them to the selection lines of a multiplexer. The remaining single variable of the function is used for the inputs of the multiplexer. In this way we can implement any Boolean function of n variables with 2^{n-1} to 1 multiplexer. Let us see one example.

Example 5.10 : *Implement the following Boolean function using 4 : 1 multiplexer.*

$$F(A, B, C) = \sum m\,(1 , 3, 5, 6)$$

Solution : Fig. 5.23 shows the implementation of function with 4 to 1 multiplexer. As mentioned earlier, here, two of the variables, B and C, are applied to the selection lines. B is connected to S_1 and C is connected to S_0. The inputs for multiplexer are derived from the implementation table.

Minterm	A	B	C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

Fig. 5.23 (a) Truth table

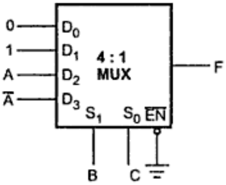


Fig. 5.23 (b) Multiplexer implementation

	D_0	D_1	D_2	D_3	
$\bar{A}$	0	①	2	③	Row 1
A	4	⑤	⑥	7	Row 2
	0	1	A	$\bar{A}$	

Fig. 5.23 (c) Implementation table

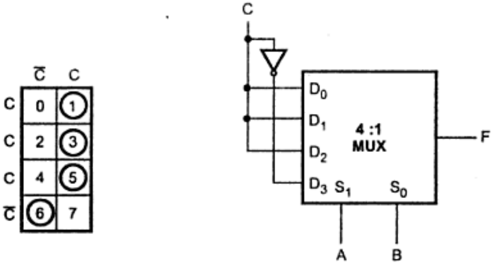
As shown in the Fig. 5.23 (c) the implementation table is nothing but the list of the inputs of the multiplexer and under them list of all the minterms in two rows. The first row lists all those minterms where A is complemented, and the second row lists all the minterms with A uncomplemented. The minterms given in the function are circled and then each column is inspected separately as follows.

- If the two minterms in a column are not circled, 0 is applied to the corresponding multiplexer input (see column 1).
- If the two minterms in a column are circled, 1 is applied to the corresponding multiplexer input (see column 2).
- If the minterm in the second row is circled and minterm in the first row is not circled, A is applied to the corresponding multiplexer input (see column 3).
- If the minterm in the first row is circled and minterm in the second row is not circled, $\bar{A}$ is applied to the corresponding multiplexer input (see column 4).

In the previous multiplexer implementation two least significant variables, i.e. B and C are connected to the select lines of the multiplexer. The multiplexer implementation is also possible by connecting most significant variables i.e. A and B (in above case) to the select lines of the multiplexer. The procedure for same is explained below.

Here, implementation table consists of two columns. The first column lists all the minterms where least significant variable is complemented ($\bar{C}$ in this case), and the second column lists all the minterms with least significant variable is uncomplemented (C in this case). The minterms given in the function are circled and then each row is inspected separately as follows.

- If the two minterms in a row are not circled, 0 is applied to corresponding multiplexer input.
- If the two minterms in a row are circled, 1 is applied to corresponding multiplexer input.
- If the minterm in the column 1 is circled, least significant variable is complemented ($\bar{C}$ in this case) and applied to the corresponding multiplexer input.
- If the minterm in the column 2 is circled, least significant variable (C in this case) is applied to the corresponding multiplexer input.



	$\bar{C}$	C
C	0	①
C	2	③
C	4	⑤
$\bar{C}$	⑥	7

(a) Implementation table **(b) Multiplexer implementation**

Fig. 5.24

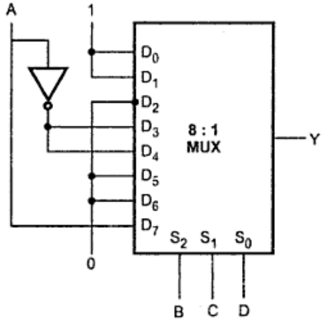
Example 5.11 : *Implement the following Boolean function using 8 : 1 MUX.*

$$F(P, Q, R, S) = \sum m(0, 1, 3, 4, 8, 9, 15)$$

Solution : Fig. 5.25 shows the implementation of given Boolean function with 8 : 1 multiplexer.

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	⓪	①	2	③	④	5	6	7
A	⑧	⑨	10	11	12	13	14	⑮
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A

(a) Implementation table



(b) Multiplexer implementation

Fig. 5.25

Example 5.12 : *Implement the following Boolean function using 4 : 1 MUX*

$$F(A, B, C, D) = \sum m\,(0, 1, 2, 4, 6, 9, 12, 14).$$

Solution : The function has four variables. To implement this function we require 8 : 1 multiplexer. i.e., two 4 : 1 multiplexers. We have already seen how to construct 8 : 1 multiplexer using two 4 : 1 multiplexers. The same concept is used here to implement given Boolean function.

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	⓪	①	②	3	④	5	⑥	7
A	8	⑨	10	11	⑫	13	⑭	15
	$\bar{A}$	1	$\bar{A}$	0	1	0	1	0

Fig. 5.26 (a) Implementation table

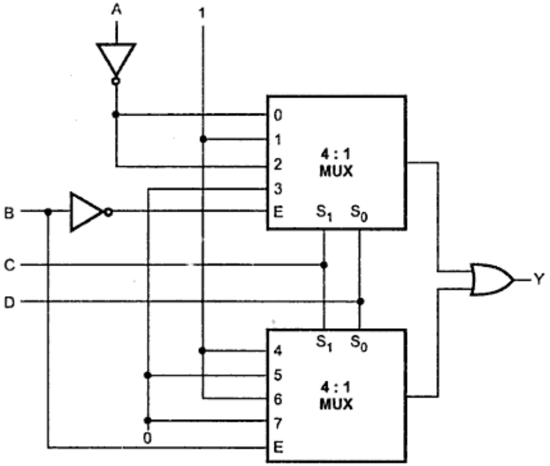


Fig. 5.26 (b) Implementation using two 4 : 1 multiplexer

➡ **Example 5.13 :** *Implement the following Boolean function using 8 : 1 multiplexer.*

$$F(A, B, C, D) = \bar{A}\ B\ \bar{D} + A\,C\,D + \bar{B}\ C\ D + \bar{A}\ \bar{C}\ D$$

Solution : The given Boolean expression is not in standard SOP form. Let us first convert this in standard SOP form.

$$\begin{aligned} F(A, B, C, D) &= \bar{A}\,B\,\bar{D}\,(C+\bar{C}) + A\,C\,D(B+\bar{B}) \\ &\quad + \bar{B}\,C\,D\,(A+\bar{A}) + \bar{A}\,\bar{C}\,D(B+\bar{B}) \\ &= \bar{A}\,B\,C\bar{D} + \bar{A}\,B\,\bar{C}\bar{D} + A\,B\,C\,D + A\bar{B}\,C\,D \\ &\quad + A\,\bar{B}\,C\,D + \bar{A}\bar{B}C\,D + \bar{A}\,B\,\bar{C}D + \bar{A}\,\bar{B}\,\bar{C}D \\ &= \bar{A}\,B\,C\bar{D} + \bar{A}\,B\,\bar{C}\bar{D} + A\,B\,C\,D + A\bar{B}\,C\,D \\ &\quad + \bar{A}\bar{B}C\,D + \bar{A}\,B\,\bar{C}D + \bar{A}\,\bar{B}\,\bar{C}D \end{aligned}$$

The truth table for this standard SOP form can be given as

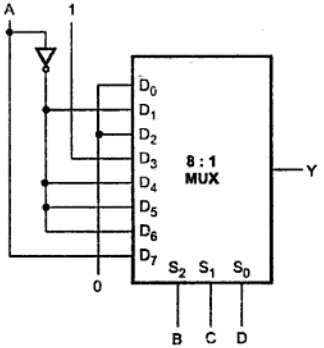
No.	Minterms	A	B	C	D	Y
0		0	0	0	0	0
1	$\bar{A}\bar{B}\bar{C}D$	0	0	0	1	1
2		0	0	1	0	0
3	$\bar{A}\bar{B}CD$	0	0	1	1	1
4	$\bar{A}B\bar{C}\bar{D}$	0	1	0	0	1
5	$\bar{A}B\bar{C}D$	0	1	0	1	1
6	$\bar{A}BC\bar{D}$	0	1	1	0	1
7		0	1	1	1	0
8		1	0	0	0	0
9		1	0	0	1	0
10		1	0	1	0	0
11	$A\bar{B}CD$	1	0	1	1	1
12		1	1	0	0	0
13		1	1	0	1	0
14		1	1	1	0	0
15	$ABCD$	1	1	1	1	1

Table 5.6 Truth table

From the truth table Boolean function can be implemented using 8 : 1 multiplexer as follows :

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	0	①	2	③	④	⑤	⑥	7
A	8	9	10	⑪	12	13	14	⑮
	0	$\bar{A}$	0	1	$\bar{A}$	$\bar{A}$	$\bar{A}$	A

(a) Implementation table



(b) Multiplexer implementation

Fig. 5.27

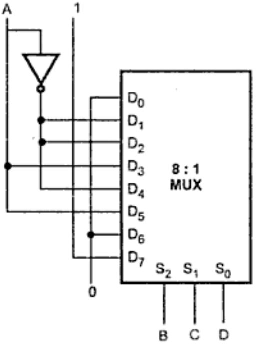
Example 5.14 : *Implement the following Boolean function with 8 : 1 multiplexer*

$F(A, B, C, D) = \pi M (0, 3, 5, 6, 8, 9, 10, 12, 14)$

Solution : Here, instead of minterms, maxterms are specified. Thus, we have to circle maxterms which are not included in the Boolean function. Fig. 5.28 shows the implementation of Boolean function with 8 : 1 multiplexer.

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	0	①	②	3	④	5	6	⑦
A	8	9	10	⑪	12	⑬	14	⑮
	0	$\bar{A}$	$\bar{A}$	A	$\bar{A}$	A	0	1

(a) Implementation table



(b) Multiplexer implementation

Fig. 5.28

Example 5.15 : *Implement the following Boolean function with 8 : 1 multiplexer.*

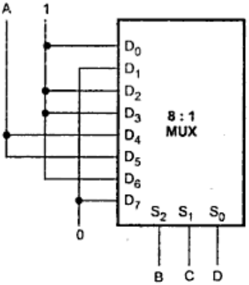
$F(A, B, C, D) = \sum m (0, 2, 6, 10, 11, 12, 13) + d (3, 8, 14)$

Solution : In the given Boolean function three don't care conditions are also specified. We know that don't care conditions can be treated as either 0s or 1s. Fig. 5.29 shows the implementation of given Boolean function using 8 : 1 multiplexer.

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	⓪	1	②	③	4	5	⑥	7
A	⑧	9	⑩	⑪	⑫	⑬	⑭	15
	1	0	1	1	A	A	1	0

Here, don't cares are treated as 1s

(a) Implementation table



(b) Implementation

Fig. 5.29

In this example, by taking don't care conditions 8 and 14 as 1s we have eliminated $\overline{A}$ term and hence the inverter.

➠ **Example 5.16 :** *An 8 × 1 multiplexer has A, B, and C connected to selection inputs S_2, S_1 and S_0 respectively. The data inputs D_0 through D_7 are as follows :*
$D_1 = D_2 = D_7 = 0$, $D_3 = D_5 = 1$, $D_0 = D_4 = D$ and $D_6 = \overline{D}$.
Determine Boolean expression.

Solution :

	$\overline{D}$	D
D	0	1
0	2	3
0	4	5
1	6	7
D	8	9
1	10	11
$\overline{D}$	12	13
0	14	15

(a)

	$\overline{D}$	D
D	0	①
0	2	3
0	4	5
1	⑥	⑦
D	8	⑨
1	⑩	⑪
$\overline{D}$	⑫	13
0	14	15

(b)

Fig. 5.30

Here, implementation table is listed for least significant bit i.e. D. The first column list all minterms with D is complemented and the second column lists all the minterms with D uncomplemented, as shown in Fig. 5.30 (a). Then according to data inputs given to the multiplexer minterms are circled applying following rules.

- If multiplexer input is 0, don't circle any minterm in the corresponding row.
- If multiplexer input 1, circle both the minterms in the corresponding row.
- If multiplexer input is D, circle the minterm belongs to column D in the corresponding row.
- If multiplexer input is $\overline{D}$, circle the minterm belongs to column $\overline{D}$ in the corresponding row.

This is illustrated in Fig. 5.30 (b). Now circled minterms can be written to get Boolean expression as follows :

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D} + \overline{A}\,B\,C\,D + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,\overline{D} + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,\overline{D}$$

Example 5.17 : *Realize* $F(w, x, y, z) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15)$ *using 4 to 1 MUX.*

Solution :

	D_0	D_1	D_2	D_3
$\bar{w}\bar{x}$	0	①	2	3
$\bar{w}x$	④	5	⑥	⑦
$w\bar{x}$	⑧	⑨	⑩	⑪
wx	12	13	14	⑮

$$D_0 = \bar{w}x + w\bar{x} = w \oplus x$$

$$D_1 = \bar{w}\bar{x} + w\bar{x} = \bar{x}$$

$$D_2 = \bar{w}x + w\bar{x} = w \oplus x$$

$$D_3 = \bar{w}x + w\bar{x} + wx = x + w\bar{x} = w + x$$

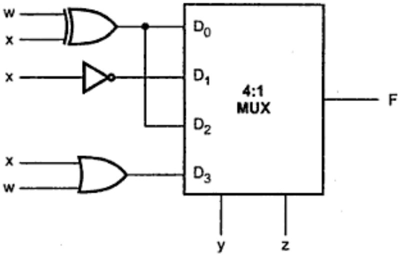


Fig. 5.31

5.3.6 Applications of Multiplexer

1. They are used as a data selector to select one out of many data inputs.
2. They can be used to implement combinational logic circuit.
3. They are used in time multiplexing systems.
4. They are used in frequency multiplexing systems.
5. They are used in A/D and D/A converter.
6. They are used in data aquisition systems.

5.4 Demultiplexers

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines. Fig. 5.32 shows 1 : 4 demultiplexer. The single input variable D_{in} has a path to all four outputs, but the input information is directed to only one of the output lines.

Enable	S_1	S_0	D_{in}	Y_0	Y_1	Y_2	Y_3
0	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

Table 5.7 Function table for 1:4 demultiplexer

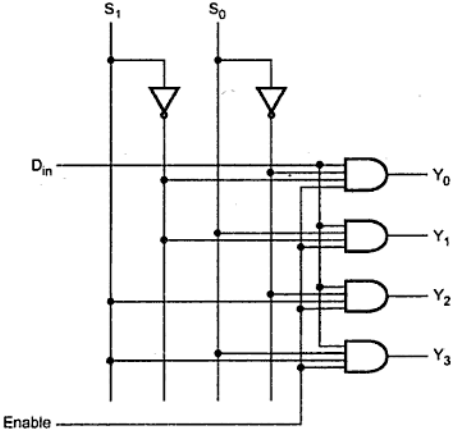


Fig. 5.32 (a) Logic diagram

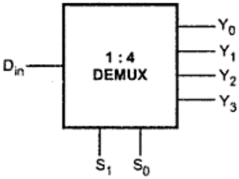

D_{in}
1 : 4
DEMUX
Y0
Y1
Y2
Y3
S1
S0

Fig. 5.32 (b) Logic symbol

Example 5.18 : *Design 1 : 8 demultiplexer using two 1 : 4 demultiplexers.*

Solution : The cascading of demultiplexers is similar to the cascading of decoder. Fig. 5.33 shows cascading of two 1 : 4 demultiplexers to form 1 : 8 demultiplexer.

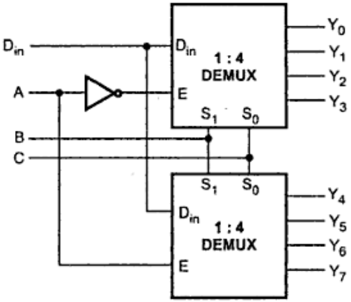

Din
A
B
C
Din
1 : 4
DEMUX
E
S1
S0
Y0
Y1
Y2
Y3
S1
S0
Din
1 : 4
DEMUX
E
Y4
Y5
Y6
Y7

Fig. 5.33 Cascading of demultiplexers

Example 5.19 : *Implement full subtractor using demultiplexer.*

Solution : Let us see the truth table of full subtractor.

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 5.8 Truth table of full subtractor

For full subtractor difference D function can be written as $D = f(A, B, C) = \sum m(1, 2, 4, 7)$ and B_{out} function can be written as

$$B_{out} = F(A, B, C) = \sum m(1, 2, 3, 7)$$

With D_{in} input 1, demultiplexer gives minterms at the output so by logically ORing required minterms we can implement Boolean functions for full subtractor. Fig. 5.34 shows the implementation of full subtractor using demultiplexer.

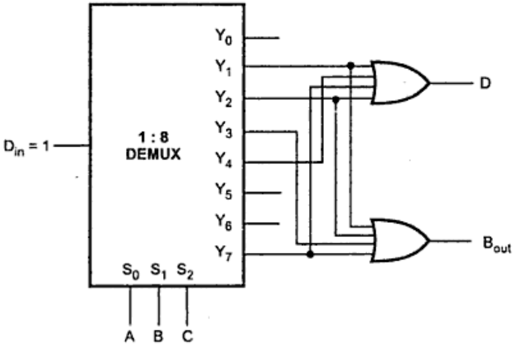


Fig. 5.34 Full subtractor using 1 : 8 demultiplexer

5.4.1 1 to 16 Demultiplexer

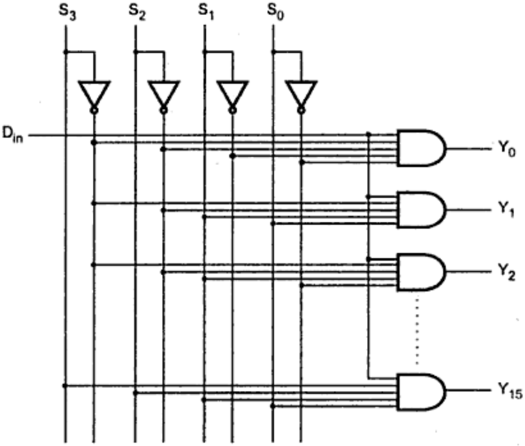


Fig. 5.35 1 : 16 demultiplexer

The Fig. 5.35 shows 1 to 16 demultiplexer. The data bit (D_{in}) has a path to all sixteen outputs. However, the input information is directed to only one of the output lines depending on the status of S_0, S_1, S_2 and S_3 lines. For example, when $S_3\ S_2\ S_1\ S_0 = 0000$, the upper AND gate is enabled while all other AND gates are disabled. Therefore, data bit D is transmitted only to the Y_0 output, giving $Y_0 = D$. If D is low, Y_0 = low and if D is high, Y_0 is high.

5.4.2 IC 74X154 (1 to 16 Demultiplexer)

The IC 74X154 accepts four active high binary address inputs and provides 16 active low outputs. It has two enable inputs : $\overline{E}_0$ and $\overline{E}_1$. These inputs must be low to enable the outputs. The Fig. 5.36 shows pin description of IC 74X154.

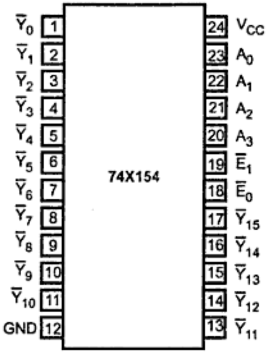

$\overline{Y}_0$ 1
$\overline{Y}_1$ 2
$\overline{Y}_2$ 3
$\overline{Y}_3$ 4
$\overline{Y}_4$ 5
$\overline{Y}_5$ 6
$\overline{Y}_6$ 7
$\overline{Y}_7$ 8
$\overline{Y}_8$ 9
$\overline{Y}_9$ 10
$\overline{Y}_{10}$ 11
GND 12
74X154
24 V_{CC}
23 A_0
22 A_1
21 A_2
20 A_3
19 $\overline{E}_1$
18 $\overline{E}_0$
17 $\overline{Y}_{15}$
16 $\overline{Y}_{14}$
15 $\overline{Y}_{13}$
14 $\overline{Y}_{12}$
13 $\overline{Y}_{11}$

Fig. 5.36 Pin description of 74X154

The IC 74X154 can be used as 1 to 16 demultiplexer by using one of the enable inputs as the multiplexer data input. When the other enable input is low, the addressed output will follow the state of the applied data. The Table 5.9 shows the function table of IC 74X154.

Inputs						**Outputs**															
($\overline{E}_1$) Enable	($\overline{E}_0$) Data	A_3	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1

0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	x	x	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	x	x	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	x	x	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 5.9 Function table of IC 74X154

Example 5.20 : *Construct 1 to 32 demultiplexer using two 74X154 ICs.*

Solution :

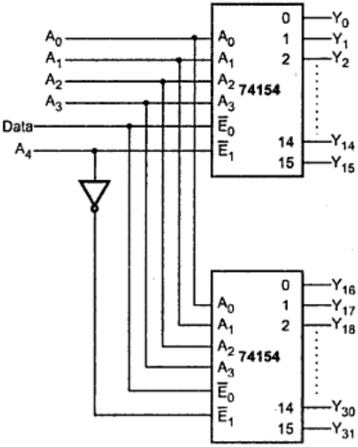


Fig. 5.37

The Fig. 5.37 shows the implementation of 1 to 32 demultiplexer using two 74X154 ICs. Here, the most significant bit of select signal (A_4) is used to enable either upper 1 to 16 demultiplexer or lower 1 to 16 demultiplexer. The data input and other select signals are connected parallel to both the demultiplexer ICs. When $A_4 = 0$, upper demultiplexer is enabled and the data input is routed to the output corresponds to the status of A_0 A_1 A_2 and A_3 lines. When $A_4 = 1$, lower multiplexer is enabled and the data input is routed to the output corresponds to the status of A_0 A_1 A_2 and A_3 lines.

5.5 Decoders

A decoder is a multiple-input, multiple-output logic circuit which converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word, i.e., there is one-to-one mapping from input code words into output code words. This one-to-one mapping can be expressed in a truth table.

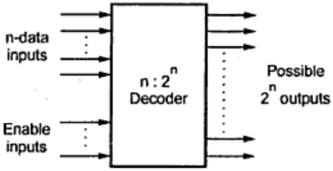


Fig. 5.38 General structure of decoder

The Fig. 5.38 shows the general structure of the decoder circuit. As shown in the Fig. 5.38, the encoded information is presented as n inputs producing 2^n possible outputs. The 2^n output values are from 0 through $2^n - 1$. Sometimes an n-bit binary code is truncated to represent fewer output values than 2^n. For example, in the BCD code, the 4-bit combinations 0000 through 1001 represent the decimal digits 0-9, and combinations 1010 through 1111 are not used. Usually, a decoder is provided with enable inputs to activate decoded output based on data inputs. When any one enable input is unasserted, all outputs of decoder are disabled.

Decoder Vs Demultiplexer

Sr. No.	Decoder	Demultiplexer
1.	Decoder is a many inputs to many outputs device.	Demultiplexer is a one input to many outputs device.
2.	There are no selection lines.	The selection of specific output line is controlled by the value of selection lines.

Multiplexer Vs Decoder

Multiplexer has several data-input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. The data of selected input line is routed to the output line. On the otherhand, decoder has n input lines and 2^n output lines. Each output line represents one minterm. Decoder activates one of the output line depending on the input combination.

Applications of Decoder

1. It can be used to implement combinational circuit.
2. It can be used to convert BCD into 7-segment code.
3. It is used in memories to select particular register.

5.5.1 Binary Decoder

A decoder which has an n-bit binary input code and a one activated output out of 2^n output code is called **binary decoder**. A binary decoder is used when it is necessary to activate exactly one of 2^n outputs based on an n-bit input value. It is similar to demultiplexer, with only one exception that it has no data input.

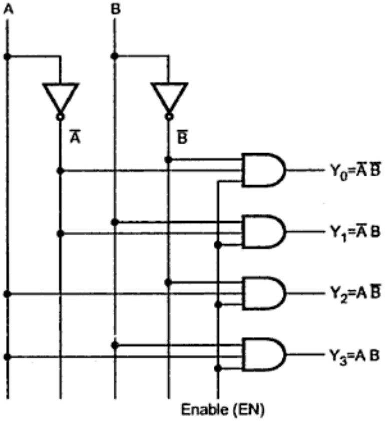


Fig. 5.39 2 to 4 line decoder

Fig. 5.39 shows 2 to 4 decoder. Here, 2 inputs are decoded into four outputs, each output representing one of the minterms of the 2 input variables. The two inverters provide the complement of the inputs, and each one of four AND gates generates one of the minterms.

The Table 5.16 shows the truth table for a 2 to 4 decoder. As shown in the truth table, if enable input is 1 (EN = 1), one, and only one, of the outputs Y_0 to Y_3, is active for a given input. The output Y_0 is active, i.e. $Y_0 = 1$ when inputs A = B = 0, the output Y_1 is active when inputs A = 0 and B = 1. If enable input is 0, i.e. EN = 0, then all the outputs are 0.

Inputs			Outputs			
EN	**A**	**B**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Table 5.10 Truth table for a 2 to 4 decoder

➡ **Example 5.21 :** *Draw the circuit for 3 to 8 decoder and explain.*

Solution : Fig. 5.40 shows 3 to 8 line decoder. Here, 3 inputs are decoded into eight outputs, each output represent one of the minterms of the 3 input variables. The three inverters provide the complement of the inputs, and each one of the eight AND gates generates one of the minterms. Enable input is provided to activate decoded output based on data inputs A, B, and C. The table shows the truth table for 3 to 8 decoder.

Inputs				Outputs							
EN	A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Table 5.11 Truth table for a 3 to 8 decoder

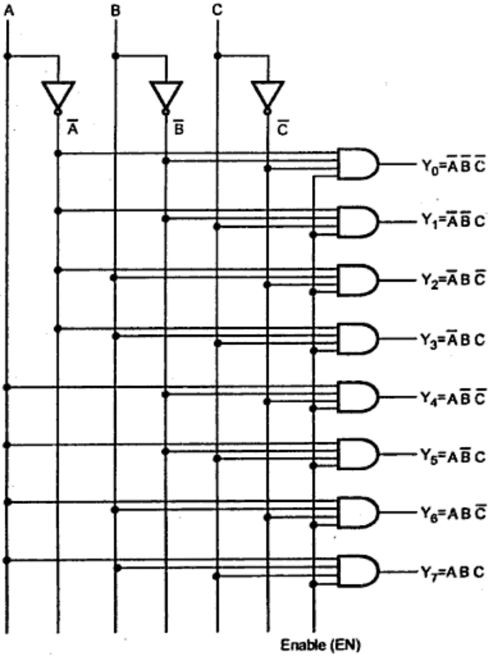

A
B
C
$\bar{A}$
$\bar{B}$
$\bar{C}$
$Y_0=\bar{A}\,\bar{B}\,\bar{C}$
$Y_1=\bar{A}\,\bar{B}\,C$
$Y_2=\bar{A}\,B\,\bar{C}$
$Y_3=\bar{A}\,B\,C$
$Y_4=A\,\bar{B}\,\bar{C}$
$Y_5=A\,\bar{B}\,C$
$Y_6=A\,B\,\bar{C}$
$Y_7=A\,B\,C$
A
B
Enable (EN)

Fig. 5.40 3 : 8 line decoder

5.5.2 The 74X138 3 to 8 Decoder

The 74X138 is a commercially available 3-to-8 decoder. It accepts three binary inputs (A, B, C) and when enabled, provides eight individual active low outputs (Y_0 - Y_7). The device has three enable inputs : two active low ($\overline{G}_{2A}, \overline{G}_{2B}$) and one active high ($G_1$). Fig. 5.41 and Table 5.12 show logic symbol and function table respectively.

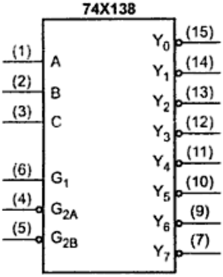


Fig. 5.41 Logic symbol

Inputs						Outputs							
G_{2B}	G_{2A}	G_1	C	B	A	$\overline{Y}_7$	$\overline{Y}_6$	$\overline{Y}_5$	$\overline{Y}_4$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	0
0	0	1	0	0	1	1	1	1	1	1	1	0	1
0	0	1	0	1	0	1	1	1	1	1	0	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	0	1	1	1	0	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1	1
0	0	1	1	1	0	1	0	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1

Table 5.12 Function table

5.5.3 The 74X139 Dual 2 to 4 Decoder

The 74X139 consists of two independent and identical 2-to-4 decoders. The enable inputs and outputs of IC 74X139 are active low. Fig. 5.42 shows the logic symbol and Table 5.12 shows the function table for IC 74X139. The Table 5.13 shows the truth table for one half of a 74X139 dual 2 to 4 decoder. The truth table for other half is same as first half.

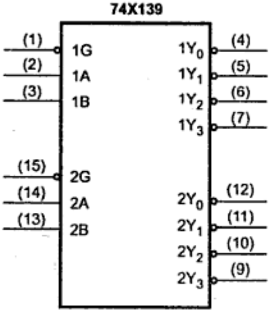

74X139
(1)
1G
(2)
1A
(3)
1B
(15)
2G
(14)
2A
(13)
2B
1Y0
(4)
1Y1
(5)
1Y2
(6)
1Y3
(7)
2Y0
(12)
2Y1
(11)
2Y2
(10)
2Y3
(9)

Fig. 5.42 Logic symbol for IC 74X139

Inputs			Outputs			
$\overline{G}$	B	A	$\overline{Y_3}$	$\overline{Y_2}$	$\overline{Y_1}$	$\overline{Y_0}$
1	x	x	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

Table 5.13 Truth table for one half of a 74X139

5.5.4 The 74X154 1 to 16 Decoder

The IC 74X154 can be used as a decoder. Here, two enable inputs are grounded to enable 74X154. When 74X154 is enabled, the output corresponds to the status of select inputs (A_3 A_2 A_1 A_0) goes low.

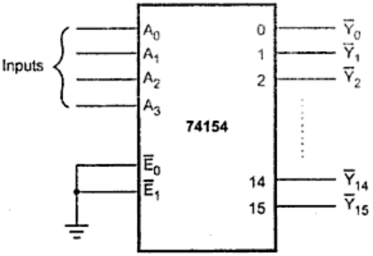

Inputs
A0
A1
A2
A3
74154
E0
E1
0
1
2
14
15
Y0
Y1
Y2
Y14
Y15

Fig. 5.43 IC 74X154 used as a 1 to 16 decoder

5.5.5 Cascading Binary Decoders

Binary decoder circuits can be connected together to form a larger decoder circuit. Fig. 5.44 shows the 4 × 16 decoder using two 3 × 8 decoders.

Here, one input line (D) is used to enable/disable the decoders. When D = 0, the top decoder is enabled and the other is disabled. Thus the bottom decoder outputs are all 1s, and the top eight outputs generate minterms 0 0 0 0 to 0 1 1 1. When D=1, the enable conditions are reversed and thus bottom decoder outputs generate minterms 1000 to 1111, while the outputs of the top decoder are all 1s.

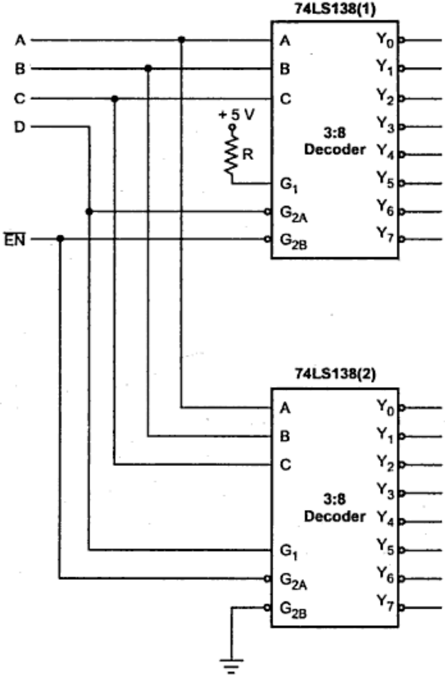


Fig. 5.44 4 : 16 decoder using two 74LS138 ICs (3 : 8 decoder)

Example 5.22 : *Design 5 to 32 decoder using one 2 to 4 and four 3 to 8 decoder ICs.*

Solution : The Fig. 5.45 shows the construction of 5 to 32 decoder using four 74LS138s and half 74LS139. The half section of 74LS139 IC is used as a 2 to 4 decoder to decode the two higher order inputs, D and E. The four outputs of this decoder are used to enable one of the four 3 to 8 decoders. The three lower order inputs A, B and C are connected in parallel to four 3 to 8 decoders. This means that the same output pin of each of the four 3 to 8 decoders is selected but only one is enabled. The remaining enable signals of four 3 to 8 decoder ICs are connected in parallel to construct enable signals for 5 to 32 decoder.

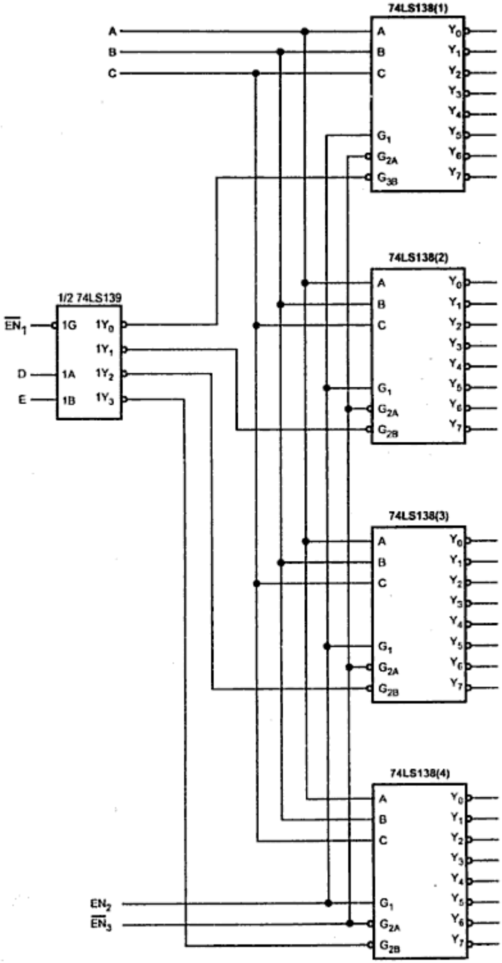

74LS138(1)
A
B
C
G$_1$
G$_{2A}$
G$_{2B}$
Y$_0$
Y$_1$
Y$_2$
Y$_3$
Y$_4$
Y$_5$
Y$_6$
Y$_7$
74LS138(2)
74LS138(3)
74LS138(4)
1/2 74LS139
$\overline{EN}_1$
1G
1A
1B
D
E
1Y$_0$
1Y$_1$
1Y$_2$
1Y$_3$
EN$_2$
$\overline{EN}_3$

Fig. 5.45 5 to 32 decoder using 74LS138 and 74LS139

Example 5.23 : *Design 4 line to 16 line decoder using 2 line to 4 line decoders.*

Solution : **4 line to 16 line decoder using 1 line to 4 line decoder.**

As shown in Fig. 5.46 five numbers of 2 : 4 decoder are required to design 4 : 16 decoder. Decoder 1 is used to enable one of the decoder 2, 3, 4 and 5. Inputs of first decoder are the A and B MSB inputs of 4 : 16 decoder. The inputs of decoder are connected together forming C and D LSB inputs of 4 : 16 decoder.

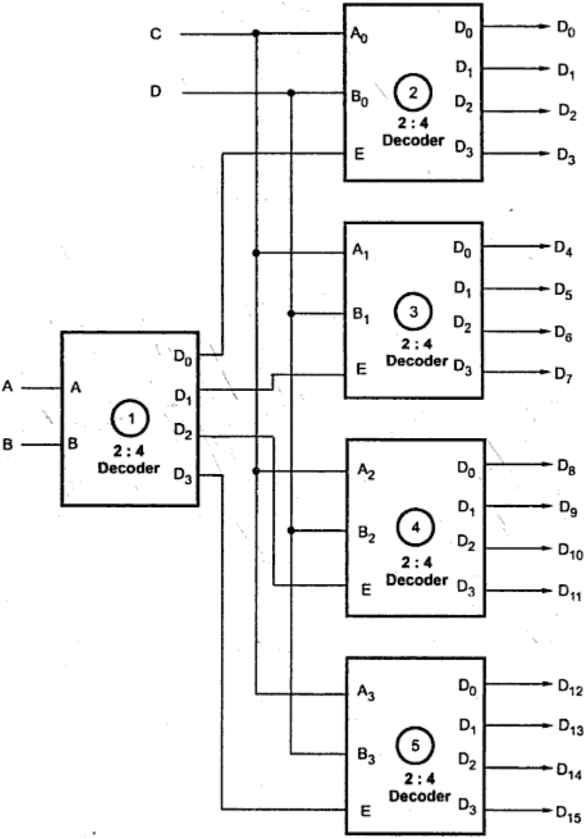

C
D
A
B
A
B
①
2 : 4
Decoder
D₀
D_0
D_1
D_2
D_3
A_0
B_0
E
②
2 : 4
Decoder
A_1
B_1
③
A_2
B_2
④
A_3
B_3
⑤
D_4
D_5
D_6
D_7
D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}

Fig. 5.46

When A and B are 0 0, decoder 2 is enabled, for AB = 0 1 decoder 3 is enabled, for AB = 10 decoder 4 is enabled and for A = B = 1, decoder 5 is enables.

5.5.6 Realization of Multiple Output Function using Binary Decoder

The combination of decoder and external logic gates can be used to implement single or multiple output functions. We know that decoder can have one of the two output states; either active low or active high. Let us see the significance of these output states in the implementation of binary function.

For Active High Output

SOP Function Implementation

When decoder output is active high, it generates minterms (product terms) for input variables; i.e. it makes selected output logic 1. In such case to implement SOP function we have to take sum of selected product terms generated by decoder. This can be implemented by ORing the selected decoder outputs, as shown in the Fig. 5.47. The Fig. 5.47 shows the implementation of function $f = \sum M(1, 2, 3, 7)$ using 3 : 8 decoder with active high outputs.

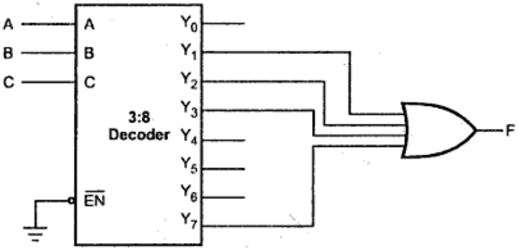


Fig. 5.47 Single output function implementation using decoder and gate

POS Function Implementation

When decoder output is active high, we can implement the POS function in similar manner as for SOP function except function output is complemented. This can be achieved by connecting NOR gate instead of OR gate. This is illustrated in Fig. 5.48. The Fig. 5.48 shows the implementation of function $f = \pi M(1, 3, 5, 7)$ using 3 : 8 decoder with active high outputs.

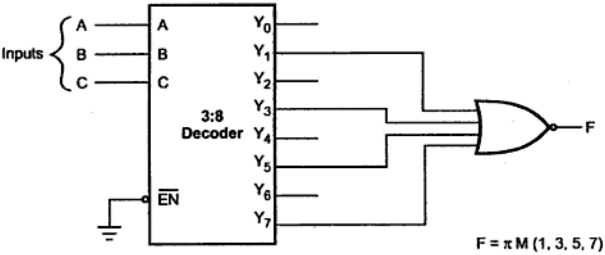


Fig. 5.48 Implementation of POS function using decoder (with active high outputs) and gate

For Active Low Output

POS Function Implementation

When decoder output is active low, the output is in complemented form, i.e., it generates maxterms (sum terms) for input variables. It makes selected output logic 0. In such case to implement POS function we have to take product of selected sum terms generated by decoder. This can be achieved by ANDing the selected decoder outputs, as shown in the Fig. 5.49 (a). The Fig. 5.49 (a) shows the implementation of function $f=\pi M(1,3,5,7)$ using 3 : 8 decoder with active low outputs.

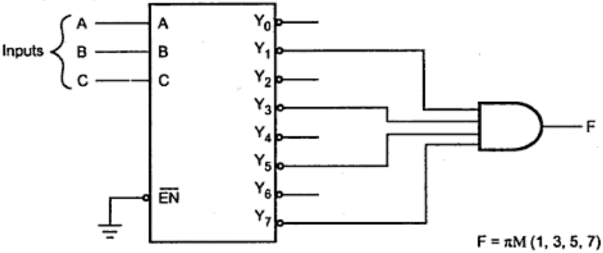


Fig. 5.49 (a) Implementation of POS function using decoder (with active low ouputs) and gate

SOP Function Implementation

When decoder output is active low, we can implement the SOP function in similar manner as for POS function except function output is complemented. This can be achieved by connecting NAND gate instead of AND gate. This is illustrated in Fig. 5.49 (b). The Fig. 5.92 (b) shows the implementation of function $f = \sum m(1,2,5,7)$ using 3 : 8 decoder with active low outputs.

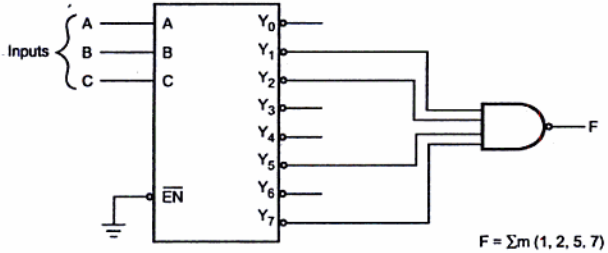

Inputs
A
B
C
A
B
C
$\overline{EN}$
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7
F
F = Σm (1, 2, 5, 7)

Fig. 5.49 (b) Implementation of SOP function using decoder (with active low outputs) and gate

Example 5.24 : *Implement following multiple output function using 74LS138 and external gates.* $F_1 (A, B, C) = \sum m(1, 4, 5, 7)$, $F_2 (A, B, C) = \pi M(2, 3, 6, 7)$.

Solution : In this example, we use IC 74LS138, 3 : 8 decoder to implement multiple output function. The outputs of 74LS138 are active low, therefore, SOP function (function F_1) can be implemented using NAND gate and POS function (function F_2) can be implemented using AND gate, as shown in Fig. 5.50.

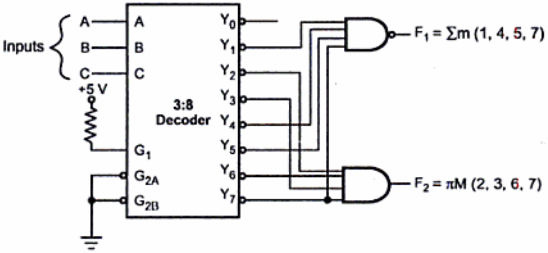

Inputs
A
B
C
+5 V
A
B
C
3:8
Decoder
G_1
G_{2A}
G_{2B}
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7
F_1 = Σm (1, 4, 5, 7)
F_2 = πM (2, 3, 6, 7)

Fig. 5.50

Example 5.25 : *Implement full subtractor using a decoder and write a truth table.*

Solution : The truth table for full subtractor is as shown in Table 5.14.

Inputs			Outputs	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1

0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 5.14 Truth table for full subtractor .

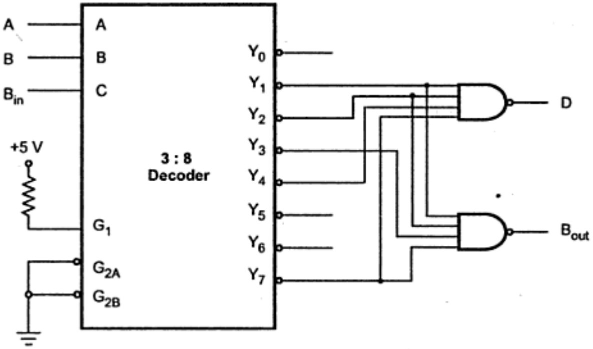

A
B
B_{in}
+5 V
A
B
C
3 : 8
Decoder
G_1
G_{2A}
G_{2B}
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7
D
B_{out}

Fig. 5.51 Implementation of full subtractor using 3 : 8 decoder

Example 5.26 : *Implement Gray to Binary code converter using suitable decoder.*

Solution : Table 5.15 shows the truth table for 3-bit binary to gray code converter.

A	B	C	G_2	G_1	G_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 5.15 Truth table for 3-bit binary to gray code converter

The Fig. 5.52 shows the implementation of 3-bit binary to gray code converter using 3:8 decoder. As outputs of 74138 are active low we have to use NAND gate instead of OR gate. The active low output from the decoder forces output(s) of connected NAND gate(s) to become HIGH, thus implementing the function.

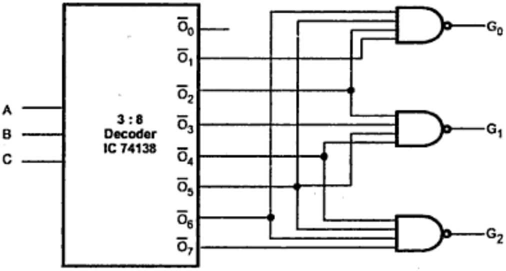

A
B
C
3 : 8
Decoder
IC 74138
$\overline{O}_0$
$\overline{O}_1$
$\overline{O}_2$
$\overline{O}_3$
$\overline{O}_4$
$\overline{O}_5$
$\overline{O}_6$
$\overline{O}_7$
G_0
G_1
G_2

Fig. 5.52

Example 5.27 : *Design 2-bit comparator using decoder.*

Solution :

Inputs				Outputs		
A_1	A_0	B_1	B_0	A > B	A = B	A< B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table 5.16

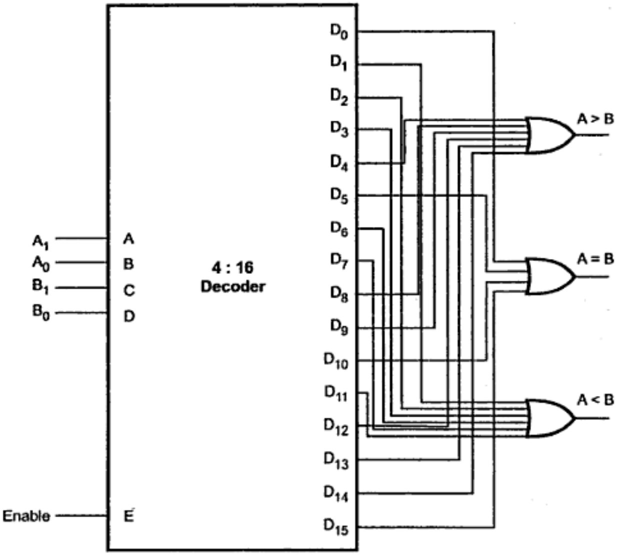

D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}
A > B
A = B
A < B
A_1
A_0
B_1
B_0
A
B
C
D
4 : 16
Decoder
Enable
E

Fig. 5.53

Example 5.28 : *Design and implement a full adder circuit using a 3 : 8 decoder.*

Solution : Truth table for full adder is as shown in the Table 5.17.

Inputs			Outputs	
A	B	C_{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 5.17 Truth table for full-adder

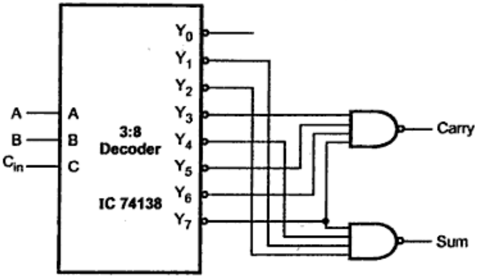
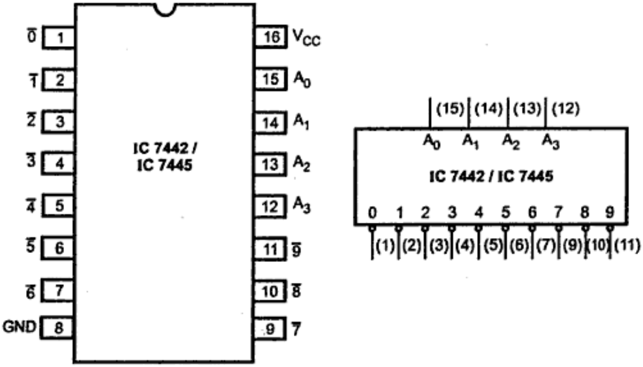

A
B
C_{in}
A
B
C
3:8
Decoder
IC 74138
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7
Carry
Sum

Fig. 5.54

Note : IC 74138 has active low outputs.

5.5.7 BCD to Decimal Decoder

BCD decoders have four inputs and 10 outputs. The four-bit BCD input is decoded to activate one of the ten outputs. The 74XX42 is a BCD to decimal decoder. It accepts four active high BCD inputs and provides 10 independent active low outputs. Fig. 5.55 (a) shows pin diagram and logic symbol for IC 7442. The active low outputs of IC 7442 facilitates addressing other MSI units with active low input enables.


$\overline{0}$ 1
$\overline{1}$ 2
$\overline{2}$ 3
$\overline{3}$ 4
$\overline{4}$ 5
$\overline{5}$ 6
$\overline{6}$ 7
GND 8
16 V_{CC}
15 A_0
14 A_1
13 A_2
12 A_3
11 $\overline{9}$
10 $\overline{8}$
9 $\overline{7}$
IC 7442 /
IC 7445
(15) (14) (13) (12)
A_0 A_1 A_2 A_3
IC 7442 / IC 7445
0 1 2 3 4 5 6 7 8 9
(1) (2) (3) (4) (5) (6) (7) (9) (10) (11)

(a) Pin diagram (b) Logic symbol

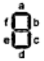
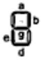
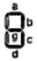
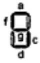
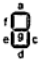
Fig. 5.55

The logic design of 7442 ensures that all outputs are high when binary codes greater than nine are applied to the inputs. The most significant input, A_3 produces a useful inhibit function when the 7442 is used as a 3 to 8 decoder.

The IC 7445 is also a BCD to decimal decoder with identical pin description as that of IC 7442. However, IC 7445 provides open collector outputs.

5.5.8 BCD to Seven Segment Decoder

In most practical applications, seven segment displays are used to give a visual indication of the output states of digital ICs such as decade counters, latches etc. These outputs are usually in four bit BCD (binary coded decimal) form, and are thus not suitable for directly driving seven segment displays. The special BCD to seven segment decoder/driver ICs are used to convert the BCD signal into a form suitable for driving these displays. In this sections, we are going to study LED and LCD decoders/drivers for seven segment displays. Let us tabulate the segments activated during each digit display.

Digit	Segments Activated	Display
0	a, b, c, d, e, f	
1	b, c	
2	a, b, d, e, g	
3	a, b, c, d, g	
4	b, c, f, g	
5	a, c, d, f, g	
6	a, c, d, e, f, g	

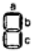
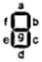
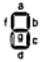
7	a, b, c	
8	a, b, c, d, e, f, g	
9	a, b, c, d, f, g	

Table 5.18

From the Table 5.18 we can determine the truth table for BCD-to-7 segment decoder/driver. This truth table also depends on the construction of 7-segment display. If 7-segment display is common anode, the segment driver output must be active low to glow the segment. In case of common cathode type 7-segment display, the segment driver output must be active high to glow the segment. Table 5.19 and 5.20 show the truth tables for both BCD to 7 segment decoder/driver with common cathode display and with common anode display respectively.

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 5.19 Truth table for BCD-to-common cathode 7-segment decoder/driver

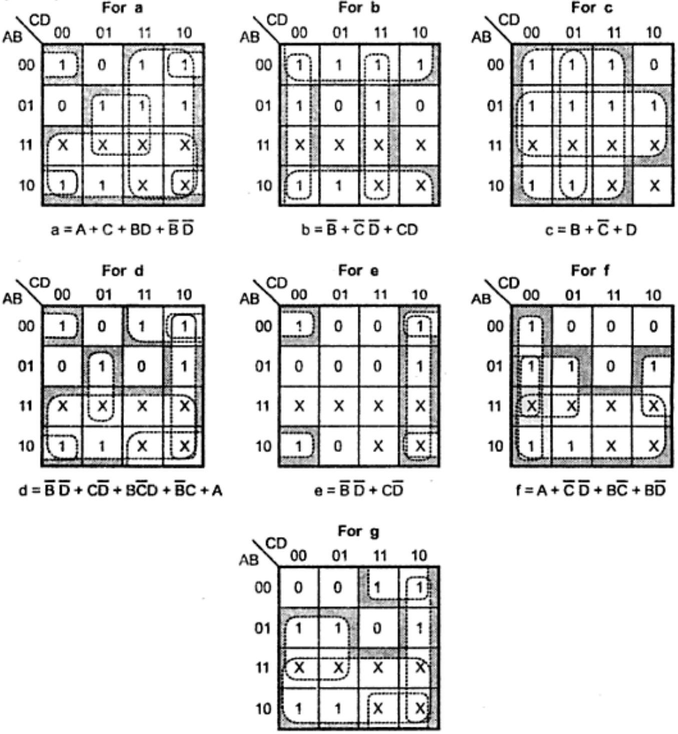
Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0

4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

Table 5.20 Truth table for BCD-to-common anode 7-segment decoder/driver

Let us design the combinational circuit for common cathode 7-segment display/driver.

K-map simplification



For a

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$a = A + C + BD + \overline{B}\,\overline{D}$

For b

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	X	X	X	X
10	1	1	X	X

$b = \overline{B} + \overline{C}\,\overline{D} + CD$

For c

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$c = B + \overline{C} + D$

For d

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

$d = \overline{B}\,\overline{D} + C\overline{D} + B\overline{C}D + \overline{B}C + A$

For e

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	1	0	X	X

$e = \overline{B}\,\overline{D} + C\overline{D}$

For f

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$f = A + \overline{C}\,\overline{D} + B\overline{C} + B\overline{D}$

For g

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$g = A + B\overline{C} + \overline{B}C + C\overline{D}$

Fig. 5.56

Logic diagram

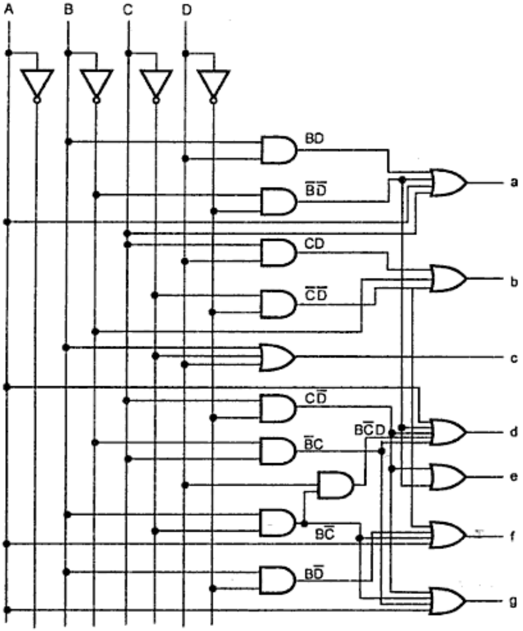


Fig. 5.57

➡ **Example 5.29 :** *Implement BCD-to-7 segment decoder for common anode using 4 : 16 decoder.*

Solution : Referring the truth table from Table 5.25 we can implement BCD-to-7 segment decoder for common anode as shown in the Fig. 5.58. (See Fig. 5.58 show on next page).

5.5.8.1 Basic Connection for Driving 7-Segment Displays

Fig. 5.59 and 5.60 show the basic connections of BCD to seven segment decoder/driver for common-anode and common-cathode displays, respectively. In both the circuits, current limiting resistors are placed in series with each display segment. Looking at the figures, we can observe that common anode decoder/driver sinks current whereas common-cathode decoder/driver source the current to each display segment.

Now we will see the practical decoder/driver ICs, their pin connections, functional description and features.

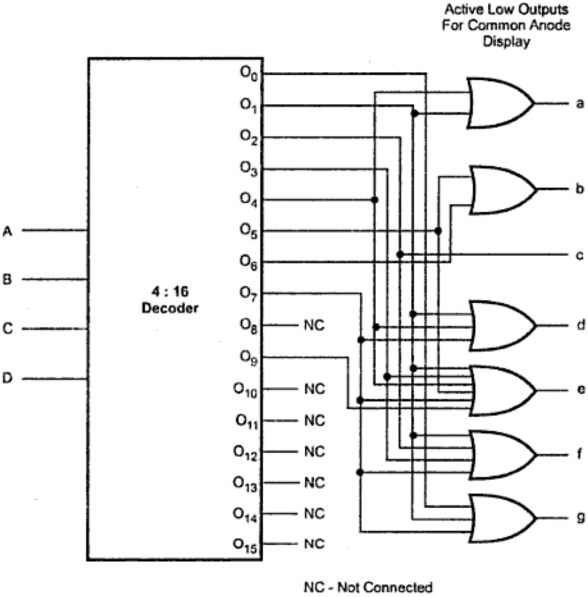

Active Low Outputs
For Common Anode
Display
A
B
C
D
4 : 16
Decoder
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
O_8
O_9
O_{10}
O_{11}
O_{12}
O_{13}
O_{14}
O_{15}
NC
a
b
c
d
e
f
g
NC - Not Connected

Fig. 5.58 BCD-to-7 segment decoder using 4 : 16 decoder

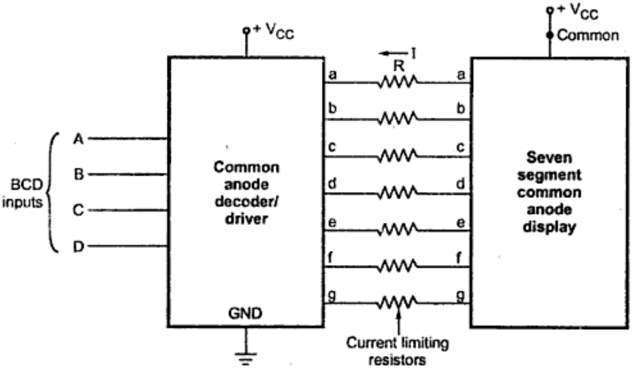

+ V_{CC}
+ V_{CC}
Common
I
R
BCD inputs
A
B
C
D
Common anode decoder/ driver
GND
a
b
c
d
e
f
g
Seven segment common anode display
Current limiting resistors

Fig. 5.59 Basic connections for driving common anode display

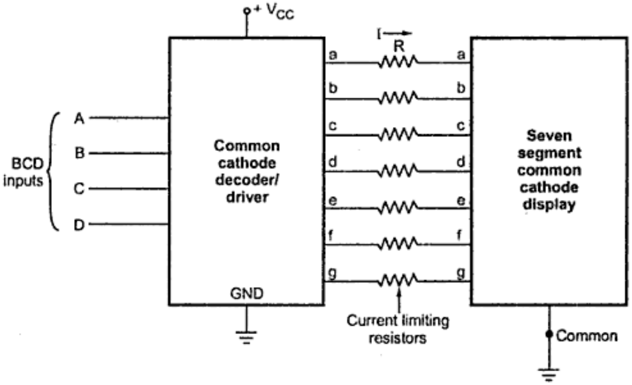

+ VCC
I
R
a
b
c
d
e
f
g
A
B
C
D
BCD inputs
Common cathode decoder/ driver
GND
Current limiting resistors
Seven segment common cathode display
Common

Fig. 5.60 Basic connections for driving common cathode display

5.5.8.2 IC 7446A, 7447A and 74LS47

The 7446A, 7447A and 74LS47 ICs accept four lines of BCD input data and gives open collector outputs to drive the individual segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for 74LS47) in the ON (LOW) state. As the outputs of these ICs sink the current, it is suitable to drive common anode seven segment displays.

Fig. 5.61 shows the pin diagram for 7446A, 7447A and 74LS47.

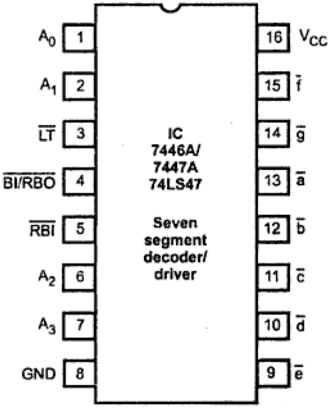

A0 1
A1 2
LT 3
BI/RBO 4
RBI 5
A2 6
A3 7
GND 8
16 VCC
15 f
14 g
13 a
12 b
11 c
10 d
9 e
IC 7446A/ 7447A 74LS47
Seven segment decoder/ driver

Fig. 5.61 Pin diagram for 7446A, 7447A and 74LS47

Pins A_0, A_1, A_2 and A_3 represent BCD inputs with A_0 as a least significant bit (LSB) and A_3 as a most significant bit (MSB). Pins $\bar{a}$ through $\bar{g}$ are the seven segment outputs. These are active low outputs, i.e. when segment output goes low (active state), segment is made 'ON'. The test lamp pin ($\overline{LT}$) is provided to test whether all segments are working properly or not. When $\overline{LT}$ pin is held low with $\overline{RBI}$ pin open or at logic high, IC drives all display terminals ON (active low). When the $\overline{BI/RBO}$ pin is pulled low, all outputs are blanked ; this pin also functions as a ripple-blanking output terminal. $\overline{BI/RBO}$ along with $\overline{RBI}$ can be used to provide ripple blanking feature discussed later.

Circuit to Drive Single Seven Segment LED Display

Fig. 5.62 shows a circuit to drive a single, seven segment, common anode LED display. For common anode, when anode is connected to positive supply, a low voltage is applied to a cathode to turn it on. Here, BCD to seven segment decoder, IC 7447 is used to apply low voltages at cathodes according to BCD input applied to 7447. To limit the current through LED segments, resistors are connected in series with the segments. This circuit connection is referred to as a static or non-multiplex display because current is being passed through the display at all times.

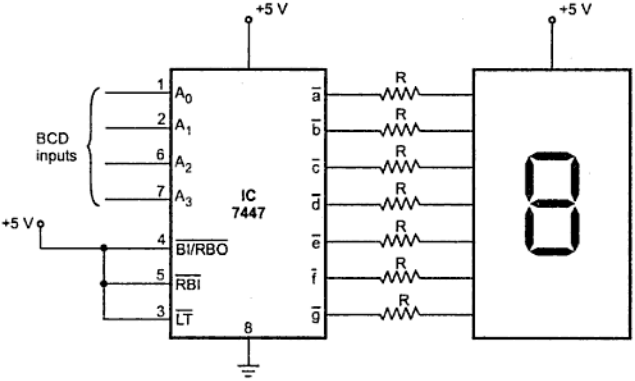


Fig. 5.62 Circuit for driving single seven segment display using 7446/7447

The value of the resistor in series with the segment can be calculated as follows :

We know, V_{CC} – drop across LED segment – IR = 0

Drop across LED segment is nearly 1.5 V.

$$
\begin{aligned}
IR &= V_{CC} - 1.5\text{ V} \\
&= 5 - 1.5\text{ V} \\
&= 3.5\text{ V}
\end{aligned}
$$

Each LED segment requires a current of between 5 and 30 mA to light. Let us assume that current through LED segment is 15 mA

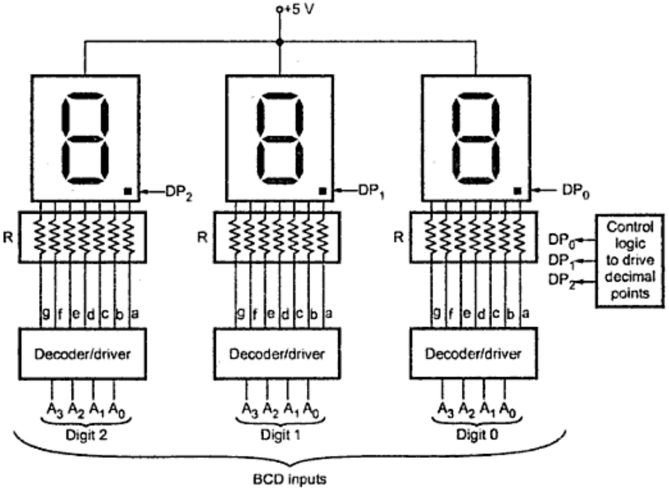
$$R = \frac{3.5\text{ V}}{15\text{ mA}}$$

$$= 233\ \Omega$$

In practice, the voltage drop across the LED and the output of 7447 are not exactly predictable and the exact current through the LED is not critical as long as we do not exceed its maximum current rating. Therefore, a standard value 220 Ω can be used.

Cascaded Non Multiplexed Displays

Several sets of seven segment displays and associated decoder/drivers ICs can be cascaded to make multi-digit display system. Fig. 5.63 shows the connection for cascaded multi-digit display system.



+5 V
DP₂
DP₁
DP₀
R
R
R
DP₀
DP₁
DP₂
Control logic to drive decimal points
g f e d c b a
g f e d c b a
g f e d c b a
Decoder/driver
Decoder/driver
Decoder/driver
A₃ A₂ A₁ A₀
A₃ A₂ A₁ A₀
A₃ A₂ A₁ A₀
Digit 2
Digit 1
Digit 0
BCD inputs

Fig. 5.63 Cascaded multi-digit non multiplexed display system

Ripple Blanking in Multi-digit Displays

If the display system shown in Fig. 5.63 is used to display count of 8, then it actually gives the reading 008. Similarly, if it is used to display 0.2, it actually gives reading 0.20. These leading and trailing zeroes can be automatically blanking using $\overline{\text{RBI}}$ and $\overline{\text{RBO}}$ signals of the IC 7447 decoder/driver. The technique of blanking leading and trailing zeroes is called **ripple blanking**.

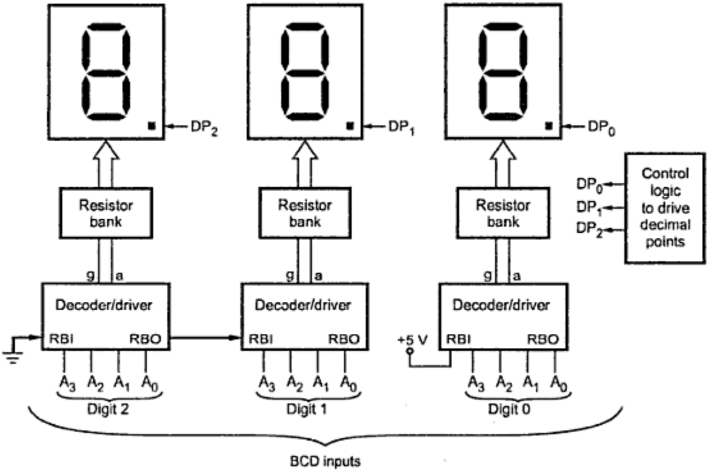

DP$_2$
DP$_1$
DP$_0$
Control logic to drive decimal points
DP$_0$
DP$_1$
DP$_2$
Resistor bank
g
a
Decoder/driver
RBI
RBO
+5 V
A$_3$ A$_2$ A$_1$ A$_0$
Digit 2
Digit 1
Digit 0
BCD inputs

Fig. 5.64 Circuit for blanking leading zeroes

Fig. 5.64 and 5.65 show circuits to provide ripple blanking for leading zeroes and trailing zeroes.

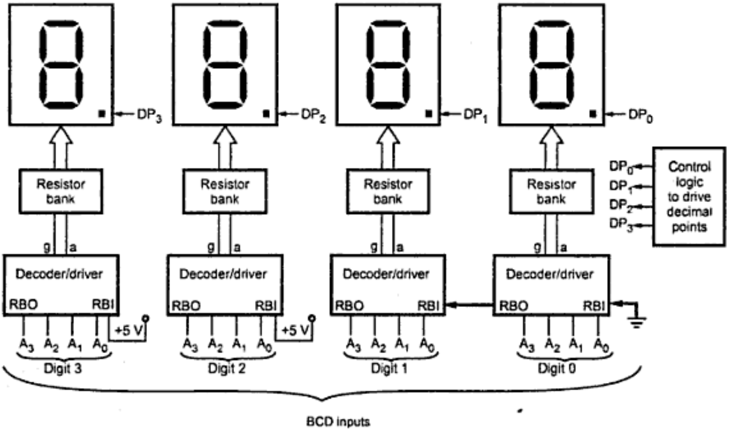

DP$_3$
DP$_2$
DP$_1$
DP$_0$
Control logic to drive decimal points
DP$_0$
DP$_1$
DP$_2$
DP$_3$
Resistor bank
g
a
Decoder/driver
RBO
RBI
+5 V
A$_3$ A$_2$ A$_1$ A$_0$
Digit 3
Digit 2
Digit 1
Digit 0
BCD inputs

Fig. 5.65 Circuit for blanking trailing zeroes

To understand the working of signals RBI and RBO we will see the internal circuit for these two signals, as shown in Fig. 5.66.

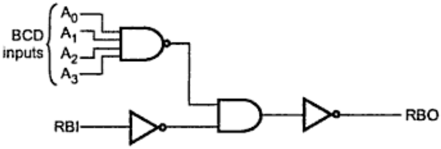


Fig. 5.66 Internal circuit for RBI and RBO signals

When RBI is low (activated) and all the BCD inputs are zero, then RBO goes low. Looking at Fig. 5.64 we can observe that when there is leading zero, digit 2 is blanked and it sets RBI zero for adjacent digit (digit 1), so that if BCD inputs for adjacent digit (digit 1) are zero, the digit is blanked.

In case of trailing zero the process of blanking starts from the right most digit. Here, digit 0 is blanked if all BCD inputs to the digit 0 are zero. If so, RBO for digit 0 goes low and therefore RBI input for digit 1 is low. Now if all BCD inputs of the digit 1 are zero then digit 1 is blanked.

Multiplexed Common Anode Displays

Untill now we have seen static or non-multiplexed display circuits. These circuits work well for driving up to four LED digits. However, these circuits are not suitable for driving more LED digits, say 8 digits. When there are more number of digits, the first problem is a power consumption. For worst-case calculations, assume that all eight digits with all segments are lit. Therefore, worst case current required is

$$I = 8 \text{ (digits)} \times 7 \text{ (segments)} \times 15 \text{ mA (current per segment)}$$
$$= 840 \text{ mA}$$

A second problem of the static approach is that each display digit requires a separate BCD to 7 segment decoder. To solve the problems of the static non-multiplexed display approach multiplexed display method is used. Fig. 5.67 shows the 4 seven segment displays connected using multiplexed method. Here, common anode seven segment LEDs are used.

Anodes are connected to + 5 V through transistors. Cathodes of all seven segments are connected in parallel and then to the output of 7447 IC through resistors. Looking at the Fig. 5.66, the question may occur in our mind that, "Aren't all of the digits going to display the same number ?" The answer is that they would show the same number only if all the digits are turned-on at the same time. However, in multiplexed display the segment information is sent for all digits on the common lines (output lines of 7447), but only one display digit is turned on at a time. The PNP transistors connected in series with the common anode of each digit acts as an ON and OFF switch for that digit. Here is how the multiplexing process works.

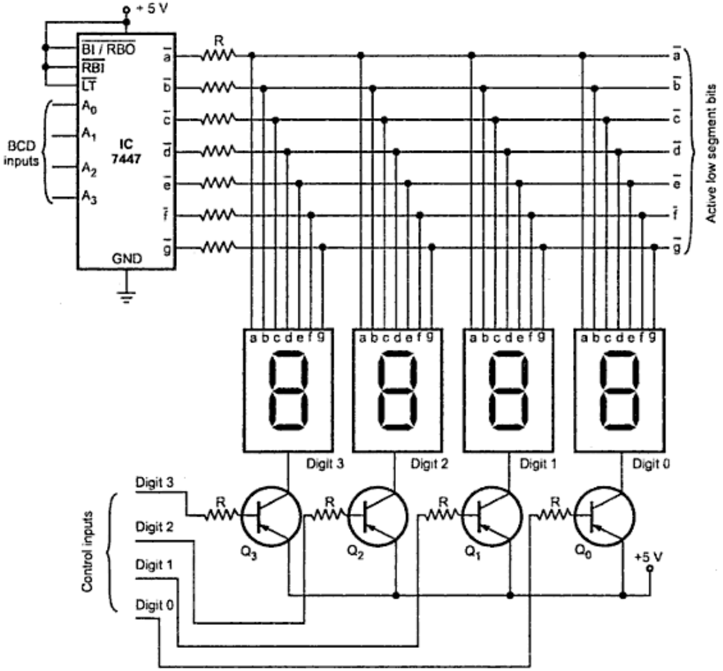

+5 V
$\overline{BI}$ / $\overline{RBO}$
$\overline{RBI}$
$\overline{LT}$
A_0
A_1
A_2
A_3
IC 7447
GND
BCD inputs
$\bar{a}$
$\bar{b}$
$\bar{c}$
$\bar{d}$
$\bar{e}$
$\bar{f}$
$\bar{g}$
R
Active low segment bits
a b c d e f g
Digit 3
Digit 2
Digit 1
Digit 0
Control inputs
Q_3
Q_2
Q_1
Q_0
+5 V

Fig. 5.67 Common anode seven segment display in multiplexed connection

The BCD code for digit 0 is first applied to the 7447. The 7447, BCD to seven segment decoder outputs the corresponding seven segment code on the segment bus lines. The transistor Q_0 connected to digit 0 is then turned on by corresponding control signals. All of the rest of the control lines are made high to ensure no other digits are turned on. After 2 ms, digit 0 is turned-off by making all control inputs high. The BCD code for digit 1 is then applied and the control input for digit 1 is made low to turn it ON. After next 2 ms, digit 1 is turned-off and the process is repeated for digit 2 and digit 4. After completion of turn for each digit, all the digits are lit again in turn.

With 4 digits and 2 ms per digit we get back to digit 1 every 8 ms or about 125 times a second. This refresh rate is fast enough that, to our eye and due to persistence of all digits will appear to be lit all the time.

In multiplexed display, the segment current is kept in between 40 mA to 60 mA so that they will appear as bright as they would, if not multiplexed. Even with this increased segment current, multiplexing gives a large saving in power and hardware components.

Multiplexed Common Cathode Displays

The Fig. 5.68 shows the circuit diagram for multiplexed common cathode seven segment display. The principle of operation of this multiplexed display is same as that of multiplexed common anode display. Here, IC 7448 is used as a BCD to seven segment decoder instead of 7447. IC 7448 has active high open collector outputs. Thus in the circuit diagram all anodes are tied to V_{CC} through full-up resistors. Other connections of IC 7448 are exactly same as that of 7447. The NPN transistors connected in series with common cathode of each digit act as a ON and OFF switch for that digit.

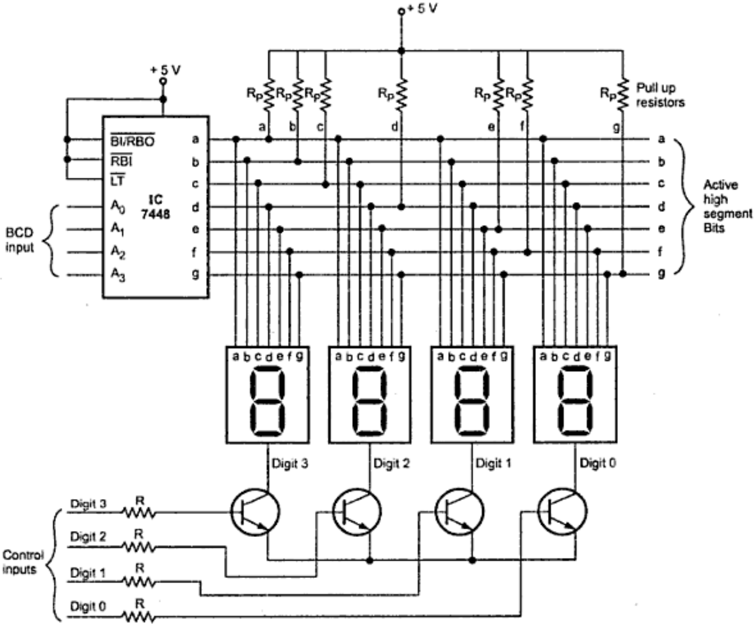

+5 V
+5 V
Rp
Pull up resistors
BI/RBO
RBI
LT
A0
A1
A2
A3
IC 7448
a b c d e f g
BCD input
Active high segment Bits
a b c d e f g
Digit 3
Digit 2
Digit 1
Digit 0
Control inputs
R

Fig. 5.68 Common cathode seven segment display in multiplexed connection

5.6 Encoders

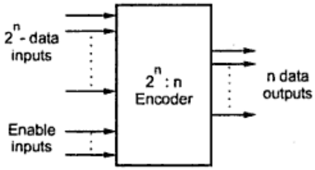

2^n - data inputs
Enable inputs
$2^n : n$ Encoder
n data outputs

Fig. 5.69 General structure of encoder

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value. The Fig. 5.69 shows the general structure of the encoder circuit. As shown in the Fig. 5.69, the decoded information is presented as 2^n inputs producing n possible outputs.

5.6.1 Decimal to BCD Encoder

The decimal to BCD encoder, usually has ten input lines and four output lines. The decoded decimal data acts as an input for encoder and encoded BCD output is available on the four output lines.

The Fig. 5.70 shows the logic symbol for decimal to BCD encoder IC, IC 74XX147. It has nine input lines and four output lines. Both input and output lines are asserted active low. It is important to note that there is no input line for decimal zero. When this condition occurs, all output lines are 1. The function table for the 74XX147 is shown in Table 5.21.

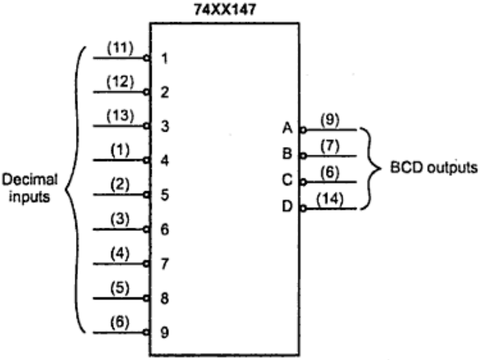

74XX147
Decimal inputs
(11) 1
(12) 2
(13) 3
(1) 4
(2) 5
(3) 6
(4) 7
(5) 8
(6) 9
A (9)
B (7)
C (6)
D (14)
BCD outputs

Fig. 5.70 Logic symbol for 74XX147 (Decimal to BCD encoder)

Decimal Value	Inputs									Outputs			
	1	2	3	4	5	6	7	8	9	D	C	B	A
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	x	0	1	1	1	1	1	1	1	1	1	0	1
3	x	x	0	1	1	1	1	1	1	1	1	0	0
4	x	x	x	0	1	1	1	1	1	1	0	1	1
5	x	x	x	x	0	1	1	1	1	1	0	1	0
6	x	x	x	x	x	0	1	1	1	1	0	0	1
7	x	x	x	x	x	x	0	1	1	1	0	0	0
8	x	x	x	x	x	x	x	0	1	0	1	1	1
9	x	x	x	x	x	x	x	x	0	0	1	1	0

x indicates don't care condition

Table 5.21 Truth table for decimal to BCD encoder

➠ **Example 5.30 :** *Draw the interfacing diagram of ten key keypad interface to a digital system using decimal to BCD encoder.*

Solution :

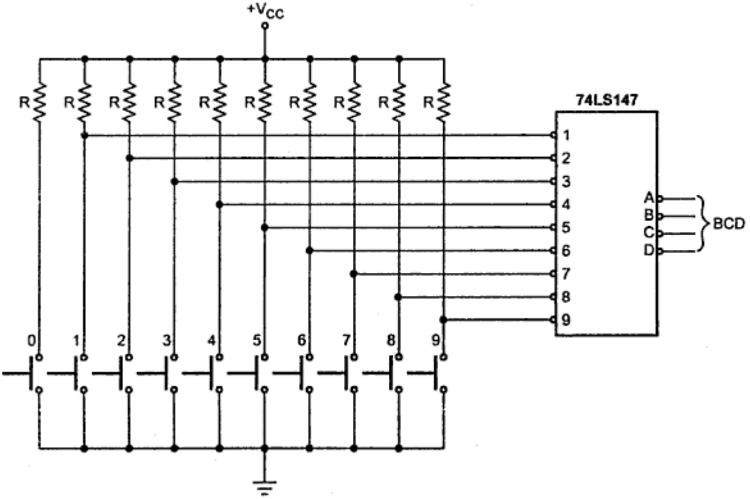


Fig. 5.71 Ten key keypad interface using decimal to BCD encoder

5.6.2 Octal to Binary Encoder

Fig. 5.72 shows octal to binary encoder. It has eight inputs, one for each octal digit, and three outputs that generate the corresponding binary code. In encoders it is assumed that only one input has a value of 1 at any given time; otherwise the circuit is meaningless.

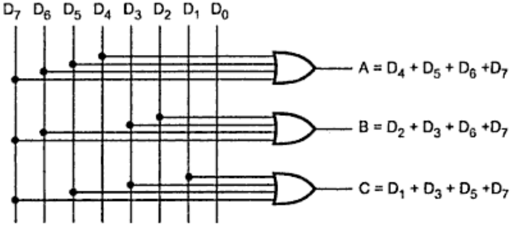

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
$A = D_4 + D_5 + D_6 + D_7$
$B = D_2 + D_3 + D_6 + D_7$
$C = D_1 + D_3 + D_5 + D_7$

Fig. 5.72 Octal to binary encoder

Table 5.22 shows the truth table of octal to binary converter.

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Table 5.22 Truth table of octal to binary encoder

The above circuit has one more ambiguity that when all inputs are 0s the outputs are 0s. The zero output can also be generated when $D_0 = 1$. This ambiguity can be resolved by providing an additional output that specifies the valid condition.

5.6.3 Priority Encoder

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

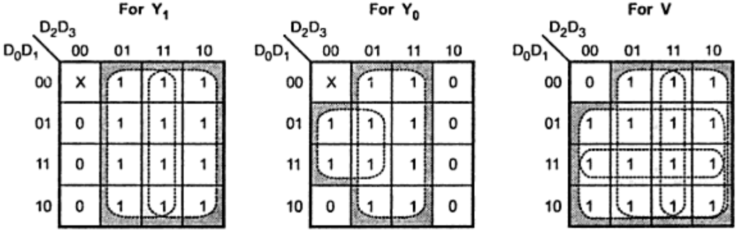
Table 5.23 shows truth table of 4-bit priority encoder.

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_0	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Table 5.23 Truth table of 4-bit priority encoder

Table 5.23 shows D_3 input with highest priority and D_0 input with lowest priority. When D_3 input is high, regardless of other inputs output is 11. The D_2 has the next priority. Thus, when $D_3 = 0$ and $D_2 = 1$, regardless of other two lower priority input, output is 10. The output for D_1 is generated only if higher priority inputs are 0, and so on. The output V (a valid output indicator) indicates, one or more of the inputs are equal to 1. If all inputs are 0, V is equal to 0, and the other two outputs (Y_1 and Y_0) of the circuit are not used.

K-map simplification



For Y_1

D_0D_1 \ D_2D_3	00	01	11	10
00	X	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

$Y_1 = D_2 + D_3$

For Y_0

D_0D_1 \ D_2D_3	00	01	11	10
00	X	1	1	0
01	1	1	1	0
11	1	1	1	0
10	0	1	1	0

$Y_0 = D_3 + D_1\overline{D}_2$

For V

D_0D_1 \ D_2D_3	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$V = D_0 + D_1 + D_2 + D_3$

Fig. 5.73(a)

Logic diagram

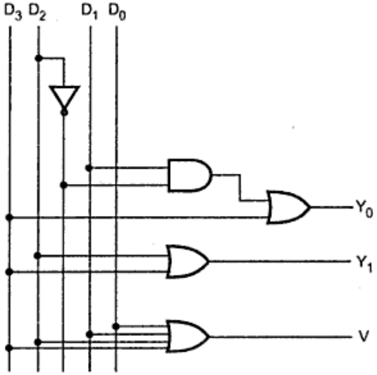
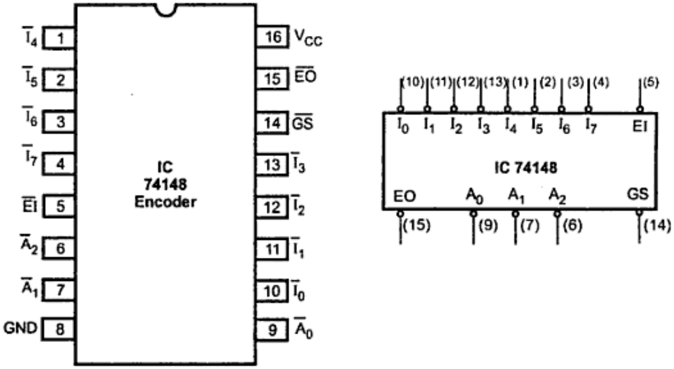

D3
D2
D1
D0
Y0
Y1
V

Fig. 5.73 (b)

5.6.4 Priority Encoder IC (74XX148)

The IC 74XX148 is an 8-input priority encoder. It accepts data from eight active low inputs and provides a binary representation on the three active-low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output. Input I_0 has least priority and input I_7 has highest priority.

Fig. 5.74 shows pin diagram and logic symbol for IC 74XX148.


$\overline{I}_4$ 1
$\overline{I}_5$ 2
$\overline{I}_6$ 3
$\overline{I}_7$ 4
$\overline{EI}$ 5
$\overline{A}_2$ 6
$\overline{A}_1$ 7
GND 8
16 V_{CC}
15 $\overline{EO}$
14 $\overline{GS}$
13 $\overline{I}_3$
12 $\overline{I}_2$
11 $\overline{I}_1$
10 $\overline{I}_0$
9 $\overline{A}_0$
IC 74148 Encoder
(10) (11) (12) (13) (1) (2) (3) (4) (5)
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 EI
IC 74148
EO A_0 A_1 A_2 GS
(15) (9) (7) (6) (14)

(a) Pin diagram

(b) Logic symbol

Fig. 5.74

$\overline{EI}$ is the active low Enable Input. A high on the $\overline{EI}$ will force all outputs to the inactive (high) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal ($\overline{GS}$) is asserted when the device is enabled and one or more of the inputs to the encoder are active. Enable Output ($\overline{EO}$) is an active low signal that can be used to cascade several priority encoder devices to form a larger priority encoding system. When all inputs are high, i.e., none of the input is active, the $\overline{EO}$ goes low indicating that no priority event connected to the IC is present. In cascaded priority encoders, $\overline{EO}$ is connected to the $\overline{EI}$ input of the next lower priority encoder. The Table 5.24 shows the truth table for 74XX148 priority encoder.

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A_2	A_1	A_0	GS	EO
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1

Table 5.24 Truth table for the 74XX148 priority encoder

➠ **Example 5.31 :** *Implement the 32 input to 5 output priority encoder using four 74LS148 and gates.*

Solution : Fig. 5.75 shows how four 74LS148 can be connected to accept 32 inputs and produce a 5-bit encoded output, A_0 - A_4. $\overline{EO}$ signal is connected to the $\overline{EI}$ input of the next lower priority encoder and $\overline{EI}$ input of the highest priority encoder is grounded. Therefore, at any time only one encoder is enabled. Since, the A_2 - A_0 outputs of at the most one 74LS148 will be enabled at a time, the outputs of the individual 74LS148s can be ORed to produce A_2 - A_0. Likewise, the individual $\overline{GS}$ outputs can be combined in a 4 to 2 encoder to produce A_4 and A_3. The GS output for 32-bit encoder is produced by ORing $\overline{GS}$ outputs of all encoders. (See Fig. 5.75 on next page.)

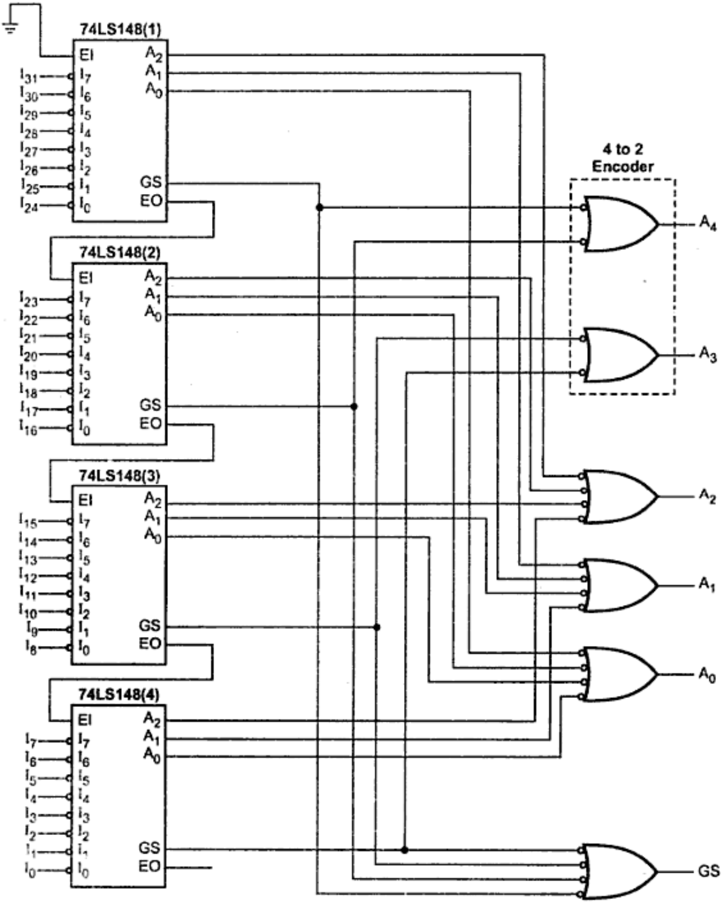

74LS148(1)
EI
I_{31} I_7
I_{30} I_6
I_{29} I_5
I_{28} I_4
I_{27} I_3
I_{26} I_2
I_{25} I_1
I_{24} I_0
A_2
A_1
A_0
GS
EO
74LS148(2)
EI
I_{23} I_7
I_{22} I_6
I_{21} I_5
I_{20} I_4
I_{19} I_3
I_{18} I_2
I_{17} I_1
I_{16} I_0
A_2
A_1
A_0
GS
EO
74LS148(3)
EI
I_{15} I_7
I_{14} I_6
I_{13} I_5
I_{12} I_4
I_{11} I_3
I_{10} I_2
I_9 I_1
I_8 I_0
A_2
A_1
A_0
GS
EO
74LS148(4)
EI
I_7 I_7
I_6 I_6
I_5 I_5
I_4 I_4
I_3 I_3
I_2 I_2
I_1 I_1
I_0 I_0
A_2
A_1
A_0
GS
EO
4 to 2
Encoder
A_4
A_3
A_2
A_1
A_0
GS

Fig. 5.75 32-input to 5 output priority encoder using four 74LS148s and gates

Review Questions

1. *Explain the design procedure for combinational circuits.*
2. *What is multiplexer ? Draw the logic diagram of 8 to 1 line multiplexer.*
3. *Design even parity generator circuit for 4-bit input using multiplexer.*
4. *Implement* $f(A, B, C, D) = \sum m(0, 3, 5, 6, 10, 12)$ *using 8:1 multiplexer.*
5. *Implement the following function using 8 : 1 MUX :*
   $f(A, B, C, D) = \pi M(0, 3, 5, 7, 12, 15) + d\ (2, 9)$
6. *Implement the following function using 4 : 1 multiplexers with active low strobe input :*
   $f(A, B, C, D) = \sum m\,(2, 3, 5, 7, 8, 9, 12, 13, 14, 15)$.
7. *Implement the following function using 4 : 1 multiplexers.*
   $f(A, B, C, D) = \sum m\ (1, 3, 6, 8, 10, 11, 15)$.
8. *What is the difference between decoder and demultiplexer ?*
9. *Design the full-adder circuit using decoder and demultiplexer.*
10. *What is decoder ?*
11. *Describe the pins required for a typical 3 to 8 decoder. Indicate the connection to be made with a neat diagram to implement.*
    $Y = \overline{C}\,\overline{B}\,\overline{A} + \overline{C}\,B\,\overline{A} + \overline{C}\,B\,A + C\,\overline{B}\,A + C\,B\,A$
12. *Implement the following functions using 3:8 decoder.*
    $F_1\ (A, B, C) = \sum m\ (0, 1, 4, 5, 7)$
    $F_2\ (A, B, C) = \sum m\ (2, 4, 6, 7)$
13. *What do you mean by encoder ?*
14. *Write a short note on priority encoder.*

□□□

6

Sequential Logic Circuits

6.1 Introduction

So far we have studied the analysis and design of combinational digital circuits. It constitutes only a part of digital systems. The other major aspect of digital system is analysis and design of sequential circuits.

There are many applications in which digital outputs are required to be generated in accordance with the sequence in which the input signals are received. This requirement cannot be satisfied using a combinational logic system. These applications require outputs to be generated that are not only dependent on the present input conditions but they also depend upon the past history of these inputs. The past history is provided by feedback from the output back to the input.

Fig. 6.1 shows the block diagram of sequential circuit/finite state machine (FSM). As shown in the Fig. 6.1, memory elements are connected to the combinational circuit as a feedback path.

The information stored in the memory elements at any given time defines the present state of the sequential circuit. The present state and the external inputs determine the outputs and the next state of the sequential circuit. Thus we can specify the sequential circuit by a time sequence of external inputs, internal states (present states and next states), and outputs.

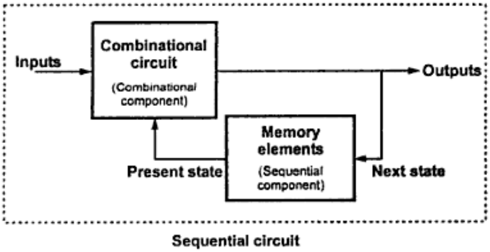

Inputs
Combinational circuit
(Combinational component)
Outputs
Memory elements
(Sequential component)
Present state
Next state
Sequential circuit

Fig. 6.1 Block diagram of sequential circuit / FSM

Sr. No.	Combinational circuits	Sequential circuits
1.	In combinational circuits, the output variables are at all times dependent on the combination of input variables.	In sequential circuits, the output variables depend not only on the present input variables but they also depend upon the past history of these input variables.
2.	Memory unit is not required in combinational circuits.	Memory unit is required to store the past history of input variables in the sequential circuit.
3.	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits.
4.	Combinational circuits are easy to design.	Sequential circuits are comparatively harder to design.
5.	Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

Table 6.1 (a) Comparison between combinational and sequential circuits

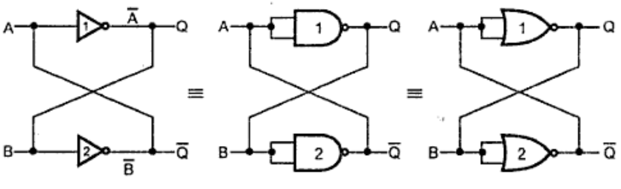
The sequential circuits can be classified depending on the timing of their signals : **Synchronous sequential circuits** and **Asynchronous sequential circuits.** In synchronous sequential circuits, signals can affect the memory elements only at discrete instants of time. In asynchronous sequential circuits change in input signals can affect memory element at any instant of time. The memory elements used in both circuits are flip-flops which are capable of storing 1-bit binary information.

Sr. No.	Synchronous sequential circuits	Asynchronous sequential circuits
1.	In synchronous circuits, memory elements are clocked flip-flops.	In asynchronous circuits, memory elements are either unclocked flip-flops or time delay elements.
2.	In synchronous circuits, the change in input signals can affect memory element upon activation of clock signal.	In asynchronous circuits change in input signals can affect memory element at any instant of time.
3.	The maximum operating speed of clock depends on time delays involved.	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits.
4.	Easier to design.	More difficult to design.

Table 6.1 (b) Comparison between synchronous and asynchronous sequential circuits

6.2 One-bit Memory Cell

The Fig. 6.2 shows the basic bistable element used in latches and flip-flops. The basic bistable element has two outputs Q and $\overline{Q}$. It has two cross-coupled inverters, i.e., the output of the first inverter is connected as an input to the second inverter and the output of second inverter is connected as an input to the first inverter.



(a) Using basic inverter (b) Using NAND gates (c) Using NOR gates

Fig. 6.2 Basic bistable element (1-bit memory cell)

The basic bistable element circuit has two stable states logic 0 and logic 1, hence the name 'bistable'. To illustrate this, assume A = 0. When A = 0, the output of inverter 1 is 1 ($\overline{A}$), i.e., Q = 1. Since the output of inverter 1 is the input to the inverter 2, $\overline{A}$ = B = 1. Consequently, the output of inverter 2, i.e., $\overline{B}$ is 0. Since the output of the inverter 2 is connected to the input of the inverter 1, $\overline{Q} = \overline{B}$ = A = 0. We have assumed same value for A. Thus, the circuit is stable with $\overline{Q} = A = \overline{B} = 0$ and $Q = \overline{A} = B = 1$. Using similar explanation it is easy to show that if it is assumed that A = 1, the basic bistable element is stable with $\overline{Q} = A = \overline{B} = 1$ and $Q = \overline{A} = B = 0$. This is a second stable condition of the basic bistable element.

The two stable states of basic bistable elements are used to store two binary elements, 0 and 1. In positive logic system, state Q = 1 is used to store logic 1, and state Q = 0 is used to store logic 0. It is important to note that the two outputs are complementary. That is when Q = 0, $\overline{Q}$ = 1; and when Q = 1, $\overline{Q}$ = 0.

From the above discussion we can note following things about the basic bistable element.

1. The outputs Q and $\overline{Q}$ are always complementary.
2. The circuit has two stable states. The state corresponds to Q = 1 is referred to as **1 state** or **set state** and state corresponds to Q = 0 is referred to as **0 state or Reset state.**
3. If the circuit is in the set (1) state, it will remain in the set state and if the circuit is in the reset (0) state, it will remain in the reset state. This property of the circuit shows that it can store 1-bit of digital information. Therefore, the circuit is called a **1-bit memory cell.**
4. The 1-bit information stored in the circuit is locked or latched in the circuit. Therefore, this circuit is also referred to as a **latch.**

Modified Circuit for 1-bit Memory Cell

In the above Fig. 6.2, when the power is switched on, the circuit switches to one of the stable states, i.e. Q = 1 or Q = 0 and it is not possible to predict the state. Thus we cannot store/enter the desired digital information in it. By replacing inverters 1 and 2 with 2-input NAND gates, we can use other input terminal of the NAND gates to enter the desired digital information. The Fig. 6.3 shows the modified circuit for 1-bit memory cell. As shown in the Fig. 6.3, two inverters 3 and 4 are connected to enter the digital information. Input for gate 3 is S and input for gate 4 is R. Hence this latch is also called **SR latch.**

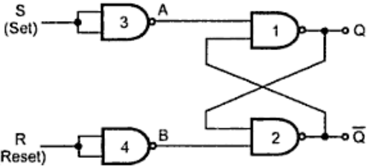


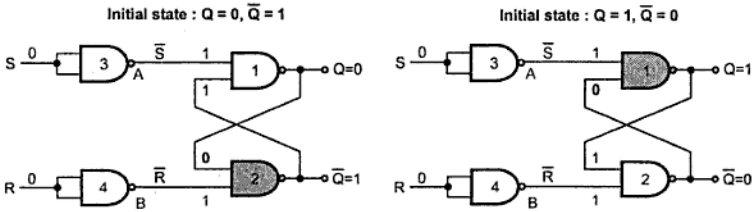
Fig. 6.3 Modified circuit for 1-bit memory cell (SR latch)

For understanding the circuit operation, we must first determine the output of NAND gate whose one of the input is logic 0 and accordingly we have to determine the output of other NAND gate in the cross coupled inverter. Because the output of NAND gate is 1 if any one input is 0. The circuit operation is as follows. In Fig. 6.4, the output of shaded NAND gate is determined first, and the 0 input that decides the output of shaded NAND as 1 is shown in bold.

Case 1 : S = R = 0

In this case, $\bar{S} = \bar{R} = 1$. If Q is 1, Q and B inputs for NAND gate 2 are both 1 and hence output $\overline{Q} = 0$. Since $\overline{Q} = 0$ and $\bar{S} = 1$, the output of NAND gate 1 is 1, i.e. Q = 1.

If Q is 0, Q and $\bar{R}$ inputs for NAND gate 2 are 0 and 1, and hence output $\overline{Q} = 1$. Since $\overline{Q} = 1$ and $\bar{S} = 1$, the output of NAND gate 1 is 0, i.e., Q = 0.


Initial state : Q = 0, $\overline{Q}$ = 1

Initial state : Q = 1, $\overline{Q}$ = 0

Fig. 6.4

This shows that when S = R = 0, the outputs do not change.

Case 2 : **S = 1 and R = 0**

In this case, $\overline{S} = 0$ and $\overline{R} = 1$. Since $\overline{S} = 0$, the output of NAND gate 1, Q = 1 (Recall that, for NAND any one or more input is 0, the output is 1). For NAND gate 2, both inputs Q and $\overline{R}$ are 1, thus output $\overline{Q} = 0$.

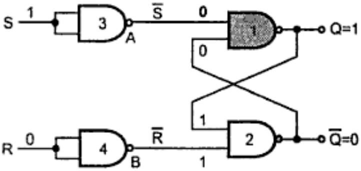


Fig. 6.5

The inputs S = 1 and R = 0, makes Q = 1, i.e., set state.

Case 3 : **S = 0 and R = 1**

In this case, $\overline{S} = 1$ and $\overline{R} = 0$. Since $\overline{R} = 0$, the output of NAND gate 2, $\overline{Q} = 1$. For NAND gate 1, both inputs $\overline{Q}$ and $\overline{S}$ are 1, thus output Q = 0.

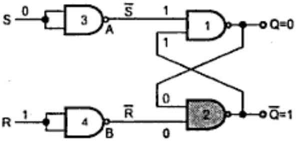


Fig. 6.6

The inputs S = 0 and R = 1, makes Q = 0, i.e., **reset** state.

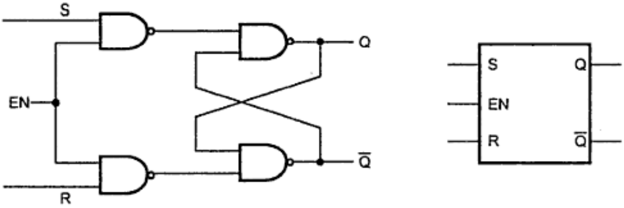
Case 4 : **S = 1 and R = 1**

When S = R = 1, both the outputs Q and $\overline{Q}$ try to become 1 which is not allowed and therefore, this input condition is prohibited.

6.3 Gated Latches

6.3.1 Gated SR Latch

In the SR latch we have seen that output changes occur immediately after the input changes occur i.e. the latch is sensitive to its S and R inputs at all times. However, it can easily be modified to create a latch that is sensitive to these inputs only when an enable input is active. Such a latch with enable input is known as **gated SR latch.** It is as shown in the Fig. 6.7. The Table 6.2 shows the truth table for gated latch. As shown by truth table, the circuit behaves like a SR latch when EN = 1, and retains its previous state when EN = 0.



(a) SR latch with enable input using NAND gates

(b) Logic symbol

Fig. 6.7

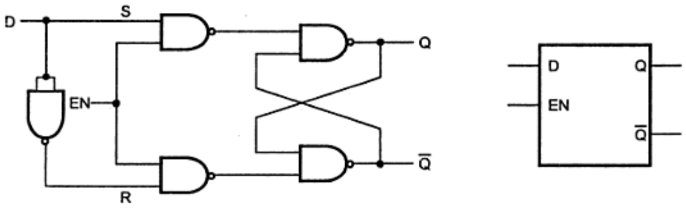
EN	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate
1	1	1	1	X	
0	X	X	0	0	No change (NC)
0	X	X	1	1	

Table 6.2 Truth table for SR latch with enable input

6.3.2 Gated D Latch

Looking at the truth table of the SR latch we can realize that when both inputs are same the output either does not change or it is invalid (Inputs → 00, no change and inputs → 11, invalid). In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other. This modified SR latch is known as D latch.

Fig. 6.8 shows the D latch. The NAND gates 1, 2, 3 and 4 form the basic SR latch with enable input. The fifth NAND gate is used to provide the complemented inputs.



(a) D latch

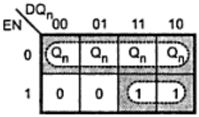
(b) Logic symbol

Fig. 6.8

As shown in the Fig. 6.8, D input goes directly to the S input, and its complement is applied to the R input, through gate 5. Therefore, only two input conditions exists, either $S = 0$ and $R = 1$ or $S = 1$ and $R = 0$. The truth table for D latch is as shown in the Table 6.3.

EN	D	Q_n	Q_{n+1}	State
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Q_n	No change (NC)

Table 6.3 Truth table for D latch



$$Q_{n+1} = EN \cdot D + \overline{EN} \cdot Q_n$$

Fig. 6.9 Characteristic equation

As shown in the truth table, the Q output follows the D input. For this reason D latch is sometimes called **transparent latch.**

Looking at the truth table for D latch with enable input and simplifying Q_{n+1} function by k-map we get the characteristic equation for D latch with enable input as $Q_{n+1} = EN \cdot D + \overline{EN} \cdot Q_n$. This is illustrated in Fig. 6.9.

6.4 Flip-Flops

6.4.1 Latches Vs Flip-Flops

Latches and flip-flops are the basic building blocks of the most sequential circuits. The main difference between latches and flip-flops is in the method used for changing their state.

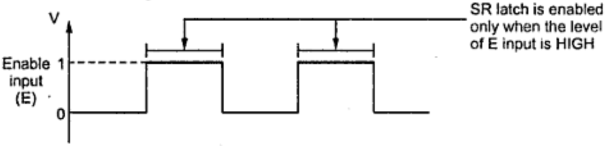
A simple latch forms the basis for the flip-flop. We have seen SR and D latches with Enable input. Latches are controlled by enable signal, and they are level triggered, either positive level triggered or negative level triggered. The output state is free to change according to the S and R input values, when active level is maintained at the enable input. Flip-flops are different from latches. Flip-flops are pulse or clock edge triggered instead of level triggered.

6.4.2 Level and Edge Triggering

Level Triggering

In the level triggering, the output state is allowed to change according to input(s) when active level (either positive or negative) is maintained at the enable input. There are two types of level triggered latches :

- **Positive level triggered :** The output of latch responds to the input changes only when its enable input is 1 (HIGH).

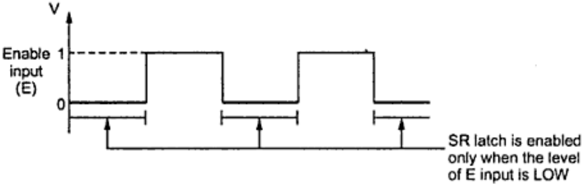


SR latch is enabled only when the level of E input is HIGH

Fig. 6.10 Positive level triggering

The SR latch shown in the Fig. 6.7 is a positive level triggered SR latch.

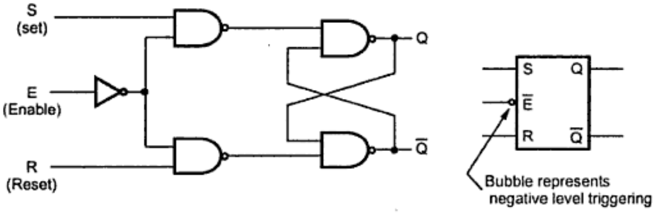
- **Negative level triggered :** The output of latch responds to the input changes only when its enable input is 0 (Low).



SR latch is enabled only when the level of E input is LOW

Fig. 6.11 Negative level triggering

The Fig. 6.12 shows the circuit and symbol for negative level triggered SR latch.



Bubble represents negative level triggering

(a) Negative level triggered SR latch **(b) Logic symbol**

Fig. 6.12

Edge triggering

In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock pulse at the clock input. There are two types of edge triggering.

- **Positive edge triggering :** Here, the output responds to the changes in the input only at the positive edge of the clock pulse at the clock input.

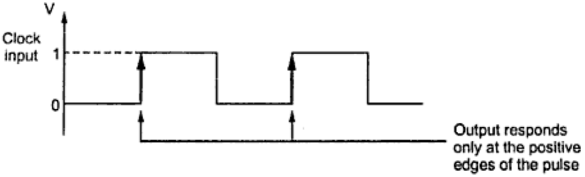

V
Clock input
1
0
Output responds only at the positive edges of the pulse

Fig. 6.13 Positive edge triggering

- **Negative edge triggering :** Here, the output responds to the changes in the input only at the negative edge of the clock pulse at the clock input.

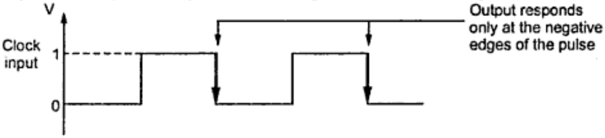

V
Output responds only at the negative edges of the pulse
Clock input
1
0

Fig. 6.14 Negative edge triggering

6.4.3 Clocked SR Flip-Flop

Positive edge triggered SR flip-flop

The Fig. 6.15 shows the positive edge triggered clocked SR flip-flop. The circuit is similar to SR latch except enable signal is replaced by the clock pulse (CP) followed by the positive edge detector circuit. The edge detector circuit is a differentiator. The Fig. 6.17 shows input and output waveforms for positive edge triggered clocked SR flip-flop. As shown in Fig. 6.17 the circuit output responds to the S and R inputs only at the positive edges of the clock pulse. At any other instants of time, the SR flip-flop will not respond to the changes in input.

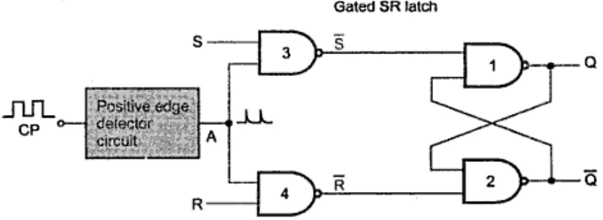
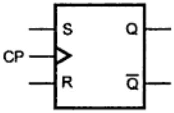

Gated SR latch
S
3
$\bar{S}$
1
Q
CP
Positive edge detector circuit
A
4
$\bar{R}$
2
$\bar{Q}$
R

Fig. 6.15 Clocked SR flip-flop

The Fig. 6.16 shows the logic symbol and truth table of clocked SR flip-flop, and Fig. 6.17 shows input and output waveforms.



CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	No change(NC)
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	X	Indeterminate
↑	1	1	1	X	
0	X	X	0	0	No change(NC)
0	X	X	1	1	

(a) Logic symbol (b) Truth table for positive edge clocked SR flip-flop

Fig. 6.16

Negative edge triggered SR flip-flop

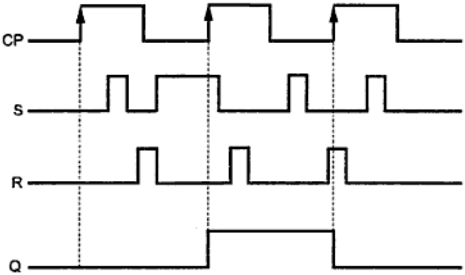
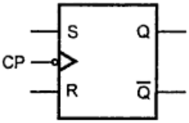


Fig. 6.17 Input and output waveforms for positive edge triggered clocked SR flip-flop

In the negative edge triggered SR flip-flop, the negative edge detector circuit is used and the circuit output responds at the negative edges of the clock pulse. The Fig. 6.18 and 6.19 shows the logic symbol, truth table, and input and output waveforms for negative edge triggered SR flip-flop. The bubble at the clock input indicates that the flip-flop is negative edge triggered.



(a) Logic symbol

CP	S	R	Q_n	Q_{n+1}	State
↓	0	0	0	0	No change(NC)
↓	0	0	1	1	
↓	0	1	0	0	Reset
↓	0	1	1	0	
↓	1	0	0	1	Set
↓	1	0	1	1	
↓	1	1	0	X	Indeterminate
↓	1	1	1	X	
0	X	X	0	0	No change(NC)
0	X	X	1	1	

(b) Truth Table for negative edge clocked SR flip-flop

Fig. 6.18

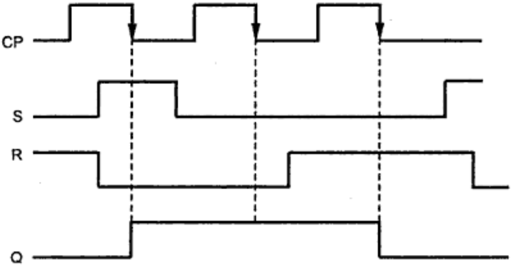


Fig. 6.19 Input and output waveforms for negative edge triggered clocked SR flip-flop

6.4.4 Clocked D Flip-Flop

Like in D latch, in D flip-flop the basic SR flip-flop is used with complemented inputs. The D flip-flop is similar to D-latch except clock pulse followed by edge detector is used instead of enable input. Such an edge triggered D flip-flop can be of two types :

- Positive edge triggered D flip-flop
- Negative edge triggered D flip-flop.

Positive edge triggered D flip-flop

The Fig. 6.20 shows the positive edge triggered D flip-flop. It consists of a gated D-latch and a positive edge detector circuit.

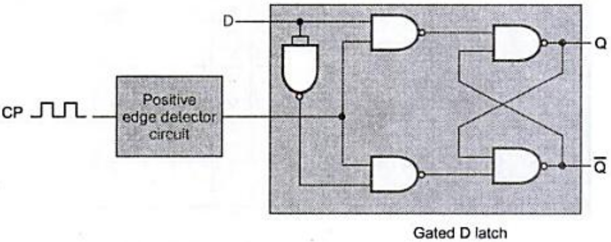


Fig. 6.20 Positive edge triggered D flip-flop

The Fig. 6.21 shows the logic symbol, truth table and the input and the output waveforms for positive edge triggered D flip-flop. As shown in the Fig. 6.21 (c), the circuit output responds to the D input only at the positive edges of the clock pulse. At any other instants of time the D flip-flop will not respond to the changes in input.

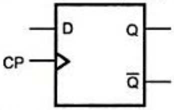


Fig. 6.21 (a) Logic symbol

CP	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n

Fig. 6.21 (b) Truth table of D flip-flop

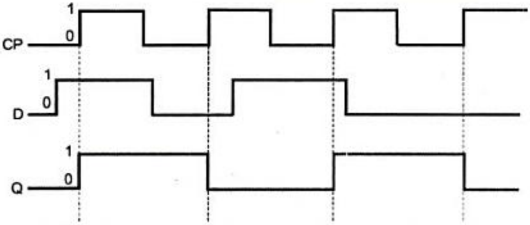


Fig. 6.21 (c) Input and output waveforms of clocked D flip-flop

Looking at the truth table for D flip-flop we can realise that Q_{n+1} function follows D input at the positive going edges of the clock pulses. Hence the characteristic equation for D flip-flop is $Q_{n+1} = D$. However, the output Q_{n+1} is delayed by one clock period. Thus, D flip-flop is also known as **delay flip-flop.**

If we connect the $\overline{Q}$ output of D flip-flop to its D input as shown in the Fig. 6.22, the output of D flip-flop will change either from 0 to 1 or form 1 to 0 at every positive edge of the D flip-flop.

Such change in the output is known as **toggling** of the flip-flop output.

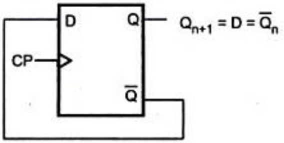
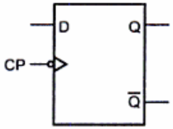


Fig. 6.22

Negative edge triggered D flip-flop



(a) Logic symbol

CP	D	Q_{n+1}
↓	0	0
↓	1	1
0	X	Q_n

(b) Truth table of D flip-flop

Fig. 6.23

In the previous explanation we have seen the output of D flip-flop is sensitive at the positive edge of the clock input. In case of negative edge triggering, the output is sensitive at the negative edge of the clock input. The Fig. 6.23 shows the logic symbol and truth table for negative edge triggered D flip-flop and Fig. 6.24 shows input and output waveforms for negative edge triggered D flip-flop. The bubble at the clock input indicates that the flip-flop is negative edge triggered.

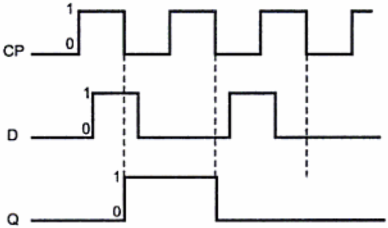


Fig. 6.24 Input output waveforms of negative edge triggered D flip-flop

6.5 Clocked JK Flip-Flop

The uncertainty in the state of an SR flip-flop when S = R = 1 can be eliminated by converting it into a JK flip-flop. The data inputs are J and K which are ANDed with $\overline{Q}$ and Q, respectively, to obtain S and R inputs, as shown in the Fig. 6.25. Thus, $S = J \cdot \overline{Q}$ and $R = K \cdot Q$.

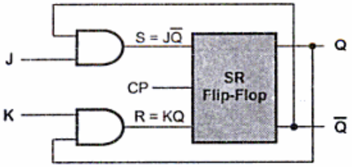


Fig. 6.25 JK flip-flop using SR flip-flop

Let us see the operation of JK flip-flop.

Case 1 : J = K = 0

When J = K = 0, S = R = 0 and according to truth table of SR flip-flop there is no change in the output.

When inputs J = K = 0, output does not change.

Case 2 : J = 1 and K = 0

Q = 0, $\overline{Q}$ = 1 : When J = 1, K = 0 and Q = 0, S = 1 and R = 0. According to truth table of SR flip-flop it is **set** state and the output Q will be 1.

Q = 1, $\overline{Q}$ = 0 : When J = 1, K = 0 and Q = 1, S = 0 and R = 0. Since SR = 00, there is no change in the output and therefore, Q = 1 and $\overline{Q}$ = 0.

The inputs J = 1 and K = 0, makes Q = 1, i.e. set state.

Case 3 : J = 0 and K = 1

Q = 0, $\overline{Q}$ = 1 : When J = 0, K = 1 and Q = 0, S = 0 and R = 0. Since SR = 00, there is no change in the output and therefore, Q = 0 and $\overline{Q}$ = 1.

Q = 1, $\overline{Q}$ = 0 : When J = 0, K = 1 and Q = 1, S = 0 and R = 1. According to truth table of SR flip-flop it is a **reset** state and the output Q will be 0.

The inputs J = 0 and K = 1, makes Q = 0, i.e., reset state.

Case 4 : J = K = 1

Q = 0, $\overline{Q}$ = 1 : When J = K = 1 and Q = 0, S = 1 and R = 0. According to truth table of SR flip-flop it is a set state and the output Q will be 1.

Q = 1, $\overline{Q}$ = 0 : When J = K = 1 and Q = 1, S = 0 and R = 1. According to truth table of SR flip-flop it is a reset state and the output Q will be 0.

The input J = K = 1, toggles the flip-flop output.

The Fig. 6.26 shows the logic symbol, truth table and timing diagram of positive edge triggered JK flip-flop.

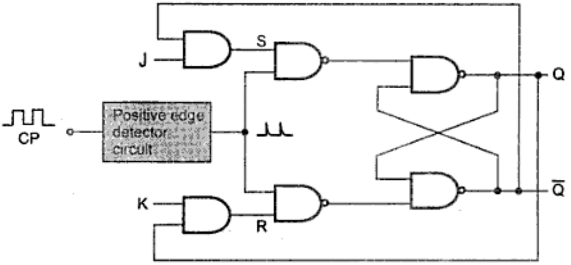


Fig. 6.26 (a) Clocked JK flip-flop

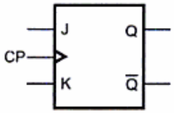


Fig. 6.26 (b) Logic symbol

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

≡

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Fig 6.26 (c) Truth table

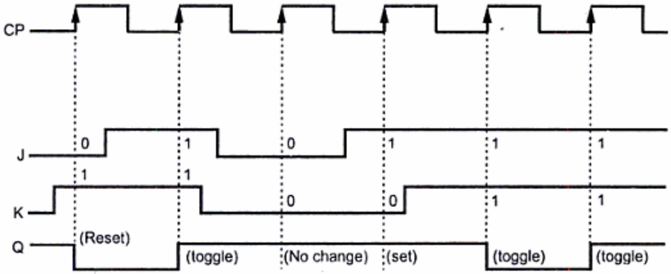


Fig. 6.26 (d) Input and output waveforms for positive edge triggered JK flip-flop

6.5.1 JK Flip-Flop using NAND Gates

In the previous section we have seen the operation of JK flip-flop using SR flip-flop and AND gates. It is not necessary to use the AND gates of Fig. 6.26 (a), since the same function can be performed by adding an extra input terminal to NAND gates 3 and 4 of Fig. 6.27. The Fig. 6.27 shows the modified circuit of JK flip-flop which has only NAND gates.

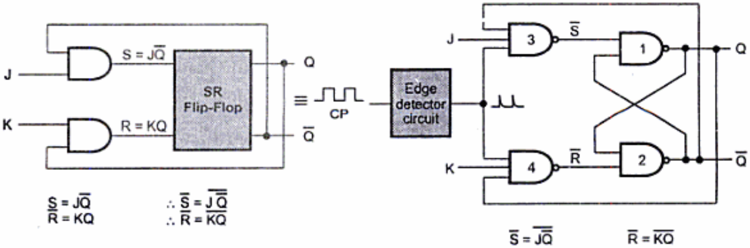

J
K
S = JQ̄
R = KQ
SR Flip-Flop
Q
Q̄
≡
CP
Edge detector circuit
J
K
3
4
1
2
S̄
R̄
Q
Q̄
S = JQ̄
R = KQ
∴ S̄ = $\overline{J\bar{Q}}$
∴ R̄ = $\overline{KQ}$
S̄ = $\overline{J\bar{Q}}$
R̄ = $\overline{KQ}$

Fig. 6.27 JK flip-flop using NAND gates

6.5.2 Race-Around Condition

In JK flip-flop, when J = K = 1, the output toggles (output changes either from 0 to 1 or from 1 to 0). Consider that initially Q = 0 and J = K = 1. After a time interval Δt equal to the propagation delay through two NAND gates in series, the output will change to Q = 1 and after another time interval of Δt the output will change back to Q = 0. This toggling will continue until the flip-flop is enabled and J = K = 1. At the end of clock pulse the flip-flop is disabled and the value of Q is uncertain. This situation is referred to as the **race-around condition.** This is illustrated in Fig. 6.28. This condition exists when $t_p \geq \Delta t$. Thus by keeping $t_p < \Delta t$ we can avoid race around condition.

We can keep $t_p < \Delta t$ by keeping the duration of edge less than Δt. A more practical method for overcoming this difficulty is the use of the master-slave (MS) configuration.

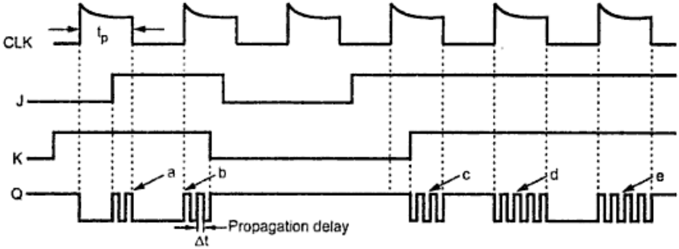


Fig. 6.28 Input and output waveforms for clocked JK flip-flop

6.6 Master-Slave Flip-Flops

6.6.1 Master-Slave SR Flip-Flop

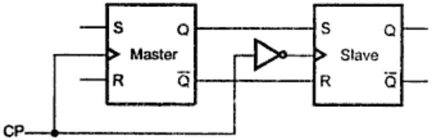


Fig. 6.29 Master-slave SR flip-flop

A master-slave flip-flop is constructed from two flip-flops. One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a master-slave flip-flop. Fig. 6.29 shows SR master-slave flip-flop. It consists of a master flip-flop, a slave flip-flop, and an inverter. Both the flip-flops are positive level triggered, but inverter connected at the clock input of the slave flip-flop forces it to trigger at the negative level.

The output state of the master flip-flop is determined by the S and R inputs at the positive clock pulse. The output state of the master is then transferred as an input to the slave flip-flop. The slave flip-flop uses this input at the negative clock pulse to determine its output state. The Fig. 6.30 illustrates the operation of the master-slave flip-flop.

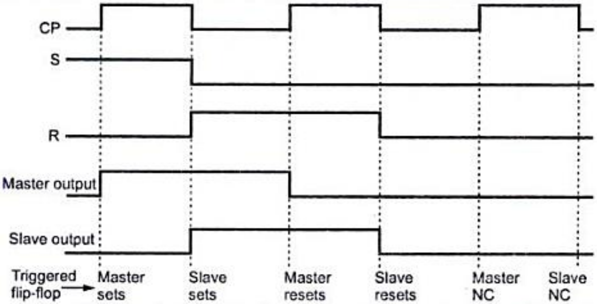


Fig. 6.30 Input and output waveforms for master-slave flip-flop

6.6.2 Master-Slave JK Flip-Flop

The master-slave combination can be constructed for any type of flip-flop. Fig. 6.30 shows one way to build a JK master-slave flip-flop. It consists of clocked JK flip-flop as a master and clocked SR flip-flop as a slave. Like SR master-slave, the output of the master flip-flop is fed as an input to the slave flip-flop. As shown in the Fig. 6.31, clock signal is connected directly to the master flip-flop, but it is connected through inverter to the slave flip-flop. Therefore, the information present at the J and K inputs is transmitted to the output of master flip-flop on the positive clock pulse and it is held there until the negative clock pulse occurs, after which it is allowed to pass through to the output of slave flip-flop. The output of the slave flip-flop is connected as a third input of the master JK flip-flop.

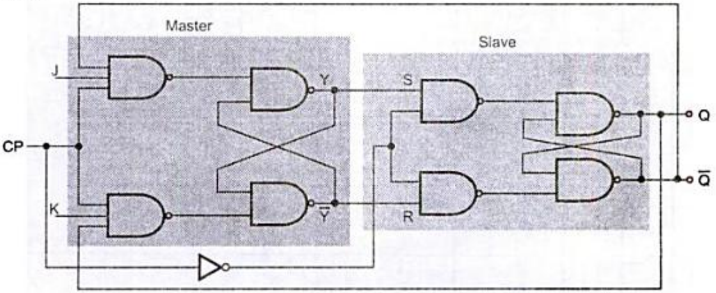


Fig. 6.31 Master-slave JK flip-flop

When J = 1 and K = 0, the master sets on the positive clock. The high Y output of the master drives the S input of the slave, so at negative clock, slave sets, copying the action of the master.

When J = 0 and K = 1, the master resets on the positive clock. The high $\overline{Y}$ output of the master goes to the R input of the slave. Therefore, at the negative clock slave resets, again copying the action of the master.

When J = 1 and K = 1, master toggles on the positive clock and slave then copies the output of master on the negative clock. At this instant, feedback inputs to the master flip-flop are complemented but as it is negative half of the clock pulse master flip-flop is inactive. This prevents race around condition. Fig. 6.32 shows input and output waveforms of master-slave JK flip-flop.

CP	Q_n	J	K	Y	Q_{n+1}
↑	0	0	0	0	NC
↓	0	0	0	NC	0
↑	0	0	1	0	NC
↓	0	0	1	NC	0
↑	0	1	0	1	NC
↓	0	1	0	NC	1
↑	0	1	1	1	NC
↓	0	1	1	NC	1
↑	1	0	0	1	NC
↓	1	0	0	NC	1
↑	1	0	1	0	NC
↓	1	0	1	NC	0
↑	1	1	0	1	NC
↓	1	1	0	NC	1
↑	1	1	1	0	NC
↓	1	1	1	NC	0

Table 6.4 Truth table for master-slave JK flip-flop

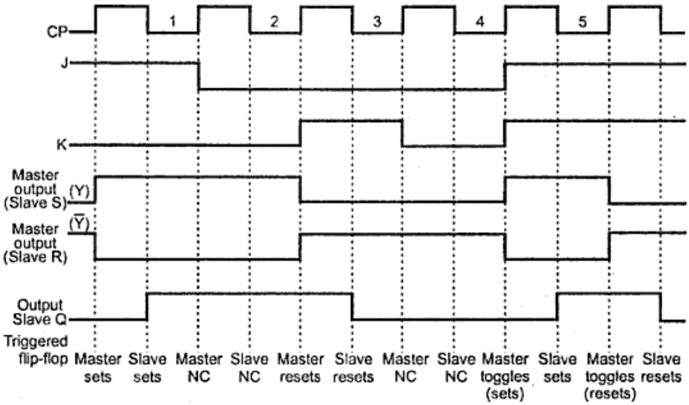

CP
1
2
3
4
5
J
K
Master output (Y) (Slave S)
Master output (Ȳ) (Slave R)
Output Slave Q
Triggered flip-flop
Master sets
Slave sets
Master NC
Slave NC
Master resets
Slave resets
Master NC
Slave NC
Master toggles (sets)
Slave sets
Master toggles (resets)
Slave resets

Fig. 6.32 Input and output waveforms of master-slave JK flip-flop

➡ **Example 6.1 :** *The D input and a single clock pulse are shown in Fig. 6.33. Compare the resulting Q outputs for : Positive edge triggered flip-flop, negative edge triggered flip-flop and pulse triggered master-slave flip-flops. The flip-flops are initially RESET.*

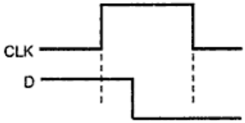


Fig. 6.33

Solution :

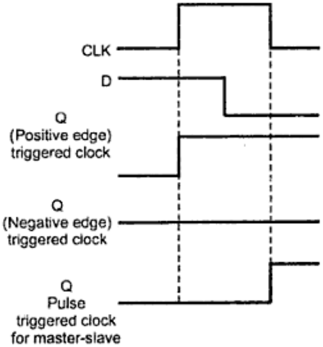

CLK
D
Q (Positive edge) triggered clock
Q (Negative edge) triggered clock
Q Pulse triggered clock for master-slave

Fig. 6.33 (a)

6.7 Clocked T Flip-Flop

T flip-flop is also known as **'Toggle flip-flop'**. The T flip-flop is a modification of the JK flip-flop. As shown in the Fig. 6.34, the T flip-flop is obtained from a JK flip-flop by connecting both inputs, J and K together.

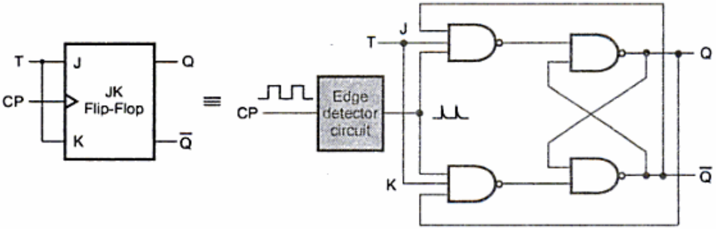
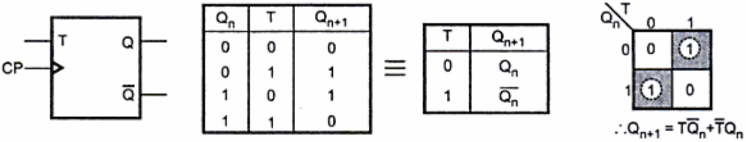

T
CP
J
JK Flip-Flop
K
Q
$\overline{Q}$
≡
CP
Edge detector circuit
T
J
K
Q
$\overline{Q}$

Fig. 6.34 T flip-flop using NAND gates

When T = 0, J = K = 0 and hence there is no change in the output. When T = 1, J = K = 1 and hence output toggles.

The Fig. 6.35 shows logic symbol, truth table and the characteristic equation for T flip-flop.


T
Q
CP
$\overline{Q}$
T
Q_n
0
1
0
0
1
1
1
0

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

≡

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

$\therefore Q_{n+1} = T\overline{Q_n} + \overline{T}Q_n$

(a) Logic symbol **b) Truth table** **(c) Characteristic equation**

Fig. 6.35

➡ **Example 6.2 :** *Refer Fig. 6.36 and determine the Q output waveform if the flip-flop starts out RESET.*

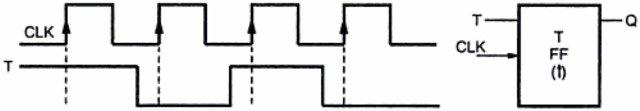

CLK
T
T
CLK
Q
T
FF
(↑)

Fig. 6.36

Solution :

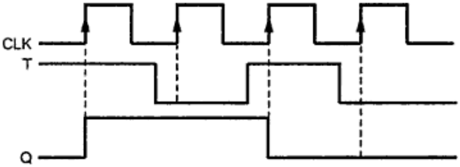
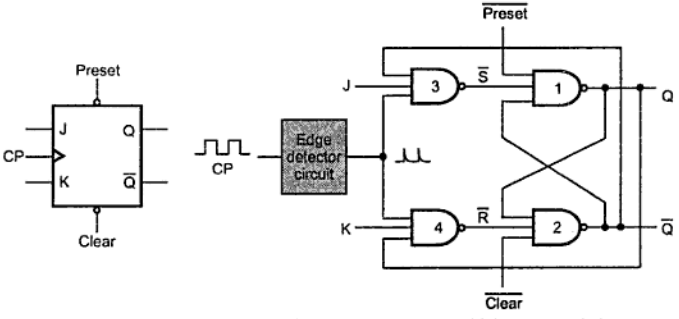


Fig. 6.37

6.8 Asynchronous or Direct Inputs

For the flip-flops discussed so far, the SR, D, JK, and T, the inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.

Flip-flops available in IC packages sometimes provide special inputs for setting (preset) or clearing (clear) the flip-flop, asynchronously. These inputs are called **asynchronous** or **direct** inputs. These inputs are connected directly into the latch portion of the flip-flop so that they override the effect of the synchronous inputs J, K and the clock.



(a) Logic symbol (b) JK flip-flop with active high preset and clear

Fig. 6.38

The JK flip-flop with preset and clear is shown in Fig. 6.38. If preset and clear inputs are 1, the circuit operates in accordance with the truth table of JK flip-flop given in the Fig. 6.26 (c). If preset = 0 and clear = 1, the output of NAND gate 1 will certainly be 1. Consequently, all the three inputs to NAND gate 2 will be 1 which will make $\overline{Q} = 0$. Hence making preset = 0 sets the flip-flop. Here, preset signal is active when it is low, hence it is active low signal. Similarly, low (0) on the clear input resets the flip-flop making $\overline{Q} = 1$.

state to the next state. For each transition, the required input condition is derived from the information available in the truth table. Let us see the process by examining each case.

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	*

Table 6.5 (a) RS Truth table

Q_n	Q_{n+1}	R	S
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

Table 6.5 (b) RS Excitation table

Note : The symbol "X" in the table represents a don't care condition, i.e., it indicates that to get required output it does not matter whether the input is either 1 or 0.

0 → 0 Transition : The present state of the flip-flop is 0 and is to remain 0 when a clock pulse is applied. Looking at truth table of RS flip-flop we can understand that, this can happen either when R = S = 0 (no-change condition) or when R = 1 and S = 0. Thus, S has to be at 0, but R can be at either level. The table indicates this with a "0" under S and an "X" (don't care) under R.

0 → 1 Transition : The present state is 0 and is to change to 1. This can happen only when S = 1 and R = 0 (set condition). Therefore, S has to be 1 and R has to be 0 for this transition to occur.

1→ 0 Transition : The present state is 1 and is to change to a 0. This can happen only when S = 0 and R = 1 (Reset condition). Therefore, S has to be 0 and R has to be 1 for this transition to occur.

1 → 1 Transition : The present state is 1 and is to remain 1. This can happen either when S = 1 and R = 0 (set condition) or when S = 0 and R = 0 (no change condition). Thus R has to be 0, but S can be at either level. The table indicates this with a "X" under S and "0" under R.

6.9.2 JK Flip-Flop

The truth table and excitation table for JK flip-flop are shown in Table 6.6 (a) and (b) respectively. Let us examine each case.

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Table 6.6 (a) JK truth table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 6.6 (b) JK excitation table

0 → 0 Transition : When both present state and next state are 0, the J input must remain at 0 and the K input can be either 0 and 1.

6.10 Conversion of Flip-Flops

It is possible to convert one flip-flop into another flip-flop with some additional gates or simply doing some extra connection. Let us see few conversions among flip-flops.

6.10.1 SR Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in Table 6.9.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Table 6.9

K-map simplification

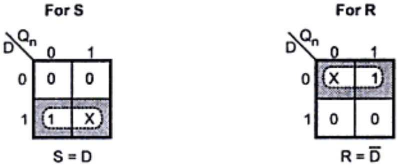

For S
D
Q_n
0
1
0
1
0
0
1
X
S = D
For R
D
Q_n
0
1
0
1
X
1
0
0
R = $\overline{D}$

Fig. 6.40

Logic diagram

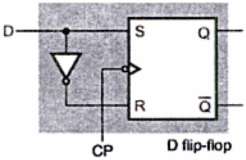

D
S
Q
R
$\overline{Q}$
CP
D flip-flop

Fig. 6.41 SR to D flip-flop conversion

6.10.3 SR Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in the Table 6.11.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Table 6.11

K-map simplification

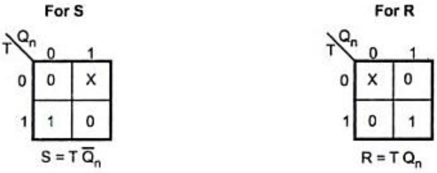

For S
T
Qn
0
1
0
1
0
X
1
0
S = T Q̄n
For R
T
Qn
0
1
0
1
X
0
0
1
R = T Qn

Fig. 6.44

Logic diagram

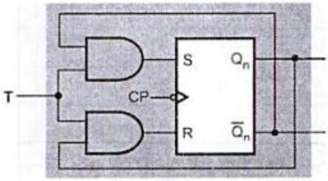


Fig. 6.45 SR to T flip-flop conversion

If we apply clock pulses to the circuit, the circuit output will toggle from 0 to 1 and 1 to 0. Thus, we can build 1-bit counter using SR Flip-flop by converting it to T flip-flop.

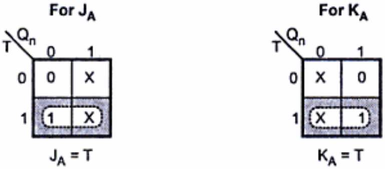
6.10.4 JK Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in Table 6.13.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	J_A	K_A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Table 6.13

K-map simplification


For J_A
T
Q_n
0
1
0
1
0
X
1
X
For K_A
T
Q_n
0
1
0
1
X
0
X
1

$J_A = T$ $K_A = T$

Fig. 6.47

Logic diagram

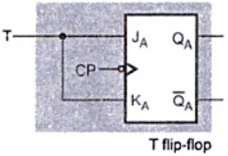

T
J_A
Q_A
CP
K_A
$\overline{Q}_A$
T flip-flop

Fig. 6.48 JK to T flip-flop conversion

6.10.5 JK Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 6.14.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Table 6.14

K-map simplification

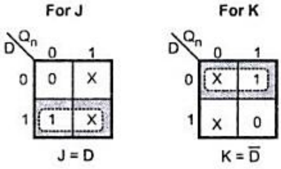

For J
D
Q_n
0
1
0
0
X
1
1
X
J = D
For K
D
Q_n
0
1
0
X
1
1
X
0
K = $\overline{D}$

Fig. 6.49

Logic diagram

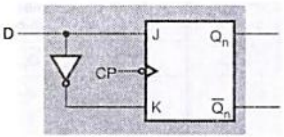

D
J
Q_n
CP
K
$\overline{Q}_n$

Fig. 6.50 JK to D flip-flop conversion

6.10.6 D Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in the Table 6.15.

Input	Present state	Next state	Flip-flop input
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Table 6.15

K-map simplification

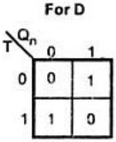

For D
T
Q_n
0
1
0
0
1
1
1
0

Fig. 6.51

Logic diagram

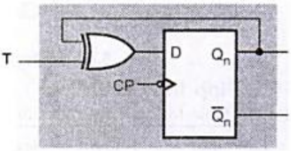

T
D
Q_n
CP
$\overline{Q}_n$

Fig. 6.52 D to T flip-flop conversion

$$D = \overline{T}Q_n + T\overline{Q}_n$$

$$= T \oplus Q_n$$

Example 6.4 : *Analyze the circuit and prove that it is equivalent to T flip-flop.*

Solution : To analyze the circuit means to derive the truth table for it.

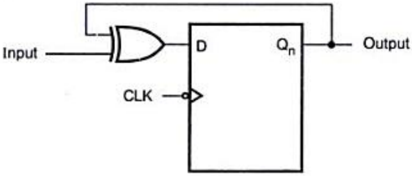


Fig. 6.53

We have, $D = \text{Input} \oplus Q_n$

CLK	Input	Q_n	$D = \text{input} \oplus Q_n$	Q_{n+1}	
↓	0	0	0	0	When input is 0 output does not change
↓	0	1	1	1	
↓	1	0	1	1	When input is 1 output toggles
↓	1	1	0	0	

Table 6.16 Truth table for given circuit

In the above circuit, output does not change when input is 0 and it toggles when input is 1. This is the characteristics of T flip-flop. Hence, the given circuit is T flip-flop constructed using D flip-flop.

6.10.7 T Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 6.17.

Input	Present state	Next state	Flip-flop input
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 6.17

K-map simplification

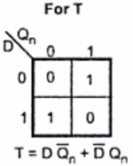
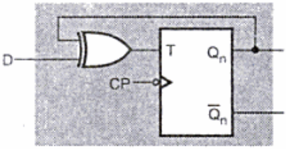

For T
D
Q_n
0
1
0
0
1
1
1
0
$T = D\overline{Q}_n + \overline{D}Q_n$

Fig. 6.54

Logic diagram


D
T
Q_n
CP
$\overline{Q}_n$

Flip-flop conversion

Fig. 6.55 T to D flip-flop conersion

$$T = D\overline{Q}_n + \overline{D}Q_n$$

6.10.8 JK Flip-Flop to SR Flip-Flop

The excitation table for above conversion is as shown in Table 6.18.

Inputs		Present state Q_n	Next state Q_{n+1}	Flip-flop inputs	
S	R			J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

Table 6.18 Excitation table for JK to SR conversion

K-map simplification

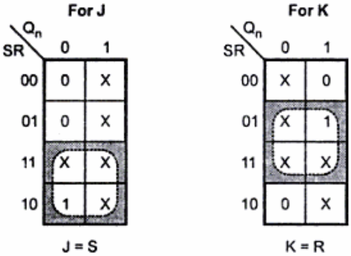

For J
SR
Q_n
0
1
00
0
X
01
0
X
11
X
X
10
1
X
J = S
For K
SR
Q_n
0
1
00
X
0
01
X
1
11
X
X
10
0
X
K = R

Fig. 6.56

Logic diagram

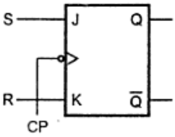

S
J
Q
R
K
$\overline{Q}$
CP

Fig. 6.57 JK to SR

6.10.9 D Flip-Flop to SR Flip-Flop

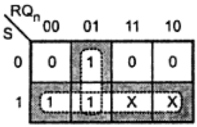
The excitation table for above conversion is as shown in the table 6.19.

Inputs		Present state	Next state	Flip-flop input
S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X

Table 6.19 Excitation table for D to SR conversion

K-map simplification

For D


RQ_n
S
00
01
11
10
0
0
1
0
0
1
1
1
X
X

$D = \overline{R}\,Q_n + S$

Fig. 6.58

Logic diagram

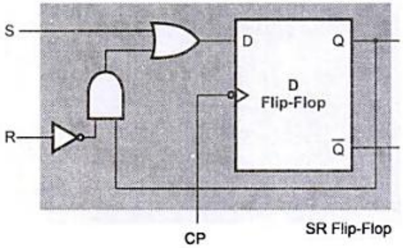


Fig. 6.59 D to SR flip-flop conversion

6.11 Applications of Flip-Flops

Some of the important applications of flip-flops are :

- It can be used as a memory element.
- It can be used to eliminate key debounce.
- It is used as a basic building block in sequential circuits such as counters and registers.
- It can be used as a delay element.

Let us discuss the application of flip-flop as a key debounce eliminator.

For interfacing keys to the digital systems, usually push button keys are used. These push button keys when pressed bounces a few times, closing and opening the contacts before providing a steady reading, as shown in the Fig. 6.60. Reading taken during bouncing period may be faulty. This problem is known as **key debounce**. The problem o key debounce is undesirable and it must be avoided.

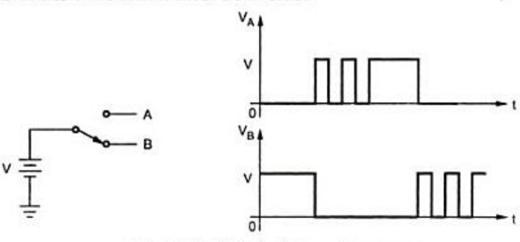


Fig. 6.60 Effect of key debounce

One way to avoid key debounce problem is to use SR latch. The circuit used to avoi keybounce with SR latch is called a **switch or contact debouncer**. The Fig. 6.61 shows th switch debouncer circuit and its waveforms. When key is at position A, the output of S latch is logic 1, and when key is at position B, the output of SR latch is logic 0. It is important to note that, when key is in between A and B, SR inputs are 00 and hence output does not change, preventing debouncing of key output. In other words, we can say that the output does not change during transition period, eliminating key debounce.

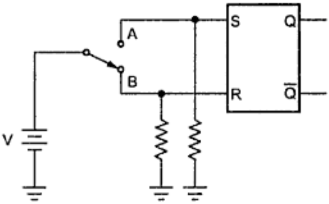


Fig. 6.61 (a) Switch debouncer

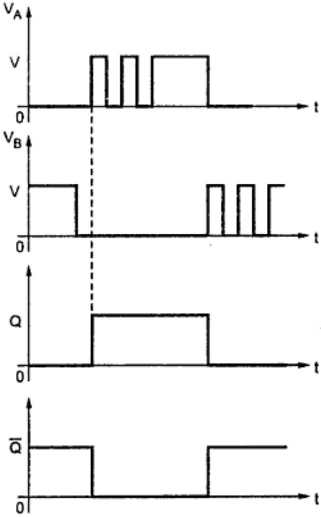


Fig. 6.61 (b) Waveforms of switch debouncer

Review Questions

1. *Draw and explain the working of following flip-flops*

   a) RS b) Clocked RS c) D d) JK e) Clocked JK

2. *Write short notes on*

   a) Edge triggered flip-flop b) Master slave flip-flop

3. *What is race around condition ? How it is avoided ?*
4. *List the functions of asynchronous inputs.*
5. *Construct the truth table for circuit shown in Fig. 6.62.*

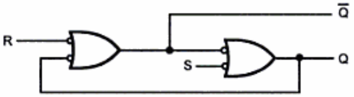


Fig. 6.62

Ans. :

R	S	Q	$\overline{Q}$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	No change	

Table 6.24

6. *Convert SR flip-flop into JK flip-flop.*
7. *Convert JK flip-flop into T flip-flop.*

□□□

7

Shift Registers

7.1 Introduction

In chapter 6 we have seen that a flip-flop is nothing but a binary cell capable of storing one bit information, and can be connected together to perform counting operations. Such a group of flip-flops is called **counter**. We have also seen that group of flip-flops can be used to store a word, which is called **register**.

A flip-flop can store 1-bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

Buffer register

Fig. 7.1 shows the simplest register constructed with four D flip-flops. This register is also called **buffer register**. Each D flip-flop is triggered with a common negative edge clock pulse. The input bits set up the flip-flops for loading. Therefore, when the first negative clock edge arrives, the stored binary information becomes,

$$Q_AQ_BQ_CQ_D = ABCD$$

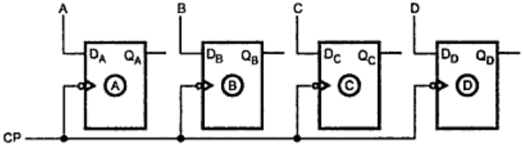


Fig. 7.1 Buffer register

In this register, four D flip-flops are used. So it can store 4-bit binary information. Thus the number of flip-flop stages in a register determines its total storage capacity.

Controlled buffer register

We can control input and output of the register by connecting tri-state devices at the input and output sides of register as shown in Fig. 7.2. So this register is called **'controlled buffer register'**.

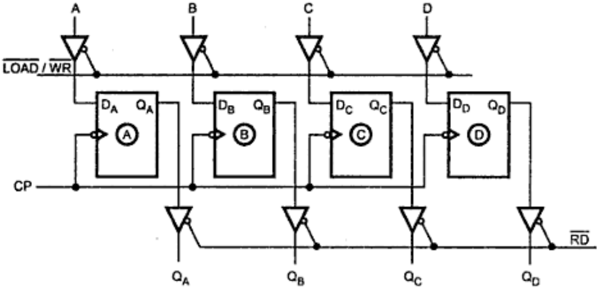


Fig. 7.2 Controlled buffer register

Here, tri-state switches are used to control the operation. When you want to store data in the register, you have to make $\overline{\text{LOAD}}$ or $\overline{\text{WR}}$ signal low to activate the tri-state buffers. When you want the data at the output, you have to make $\overline{\text{RD}}$ signal low to activate the buffers. Controlled buffer registers are commonly used for temporary storage of data within a digital system.

As seen above the 4-bit register can store 4-bit binary information. In general, n-bit register can store n-bit binary information.

➠ **Example 7.1 :** *Determine the number of flip-flops needed to construct a register capable of storing,*

i) A 6-bit binary number *ii) Decimal numbers upto 32*

iii) Hexadecimal numbers upto F *iv) Octal numbers upto 10.*

Solution :

i) A 6-bit binary number requires register with 6 flip-flops.

ii) $(32)_{10}$ = $(100000)_2$. The number of bits required to represent 32 in binary are six, therefore, 6 flip-flops are needed to construct a register capable of storing 32 decimal.

iii) $(F)_{16}$ = $(1111)_2$. The number of bits required to represent $(F)_{16}$ in binary are four, therefore four flip-flops are needed to construct a register capable of storing $(F)_{16}$.

iv) $(10)_8$ = $(1000)_2$. The number of bits required to represent $(10)_8$ in binary are four, therefore, four flip-flops are needed to construct a register capable of storing $(10)_8$.

We will illustrate the entry of the four bit binary number 1111 into the register, beginning with the left-most bit.

Initially, register is cleared. So

$$Q_AQ_BQ_CQ_D = 0\ 0\ 0\ 0$$

a) When data 1 1 1 1 is applied serially, i.e. left-most 1 is applied as D_{in},

$D_{in} = 1,\ Q_AQ_BQ_CQ_D = 0\ 0\ 0\ 0$

The arrival of the first falling clock edge sets the right-most flip-flop, and the stored word becomes,

$$Q_AQ_BQ_CQ_D = 0\ 0\ 0\ 1$$

b) When the next negative clock edge hits, the Q_C flip-flop sets and the register contents become,

$$Q_AQ_BQ_CQ_D = 0\ 0\ 1\ 1$$

c) The third negative clock edge results in,

$$Q_AQ_BQ_CQ_D = 0\ 1\ 1\ 1$$

d) The fourth falling clock edge gives,

$$Q_AQ_BQ_CQ_D = 1\ 1\ 1\ 1$$

Fig. 7.5 illustrates the input and output condition for each flip-flop stage upon application of each clock pulse. (See Fig. 7.5 on next page.)

Fig. 7.6 shows serial-in serial-out shift-right register.

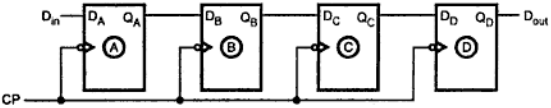


Fig. 7.6 Shift-right register

We will illustrate the entry of the four bit binary number 1111 into the register, beginning with the left-most bit.

Initially, register is cleared. So $Q_AQ_BQ_CQ_D = 0\ 0\ 0\ 0$

a) When data 1 1 1 1 is applied serially, i.e. left-most 1 is applied as D_{in},

$$D_{in} = 1,\ Q_AQ_BQ_CQ_D = 0\ 0\ 0\ 0$$

The arrival of the first falling clock edge sets the left-most flip-flop, and the stored word becomes,

$$Q_AQ_BQ_CQ_D = 1\ 0\ 0\ 0$$

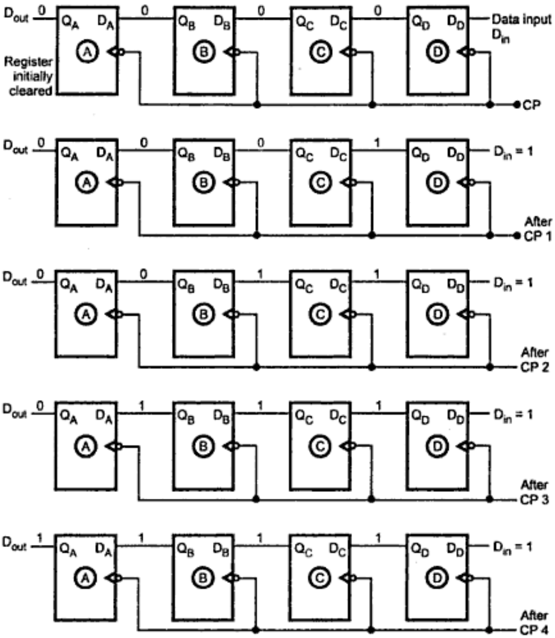

D_out
Q_A D_A
Q_B D_B
Q_C D_C
Q_D D_D
A
B
C
D
Register initially cleared
Data input D_in
CP
D_in = 1
After CP 1
After CP 2
After CP 3
After CP 4
0
1

Fig. 7.5 Four bits 1111 being serially entered into shift-left register

b) When the next falling clock edge hits, the Q_B flip-flop sets and the register contents become,

$$Q_AQ_BQ_CQ_D = 1100$$

c) The third falling clock edge results in,

$$Q_AQ_BQ_CQ_D = 1110$$

d) The fourth falling clock edge gives,

$$Q_AQ_BQ_CQ_D = 1111$$

Fig. 7.7 illustrates the input and output condition of each flip-flop stage upon application of each clock pulse.

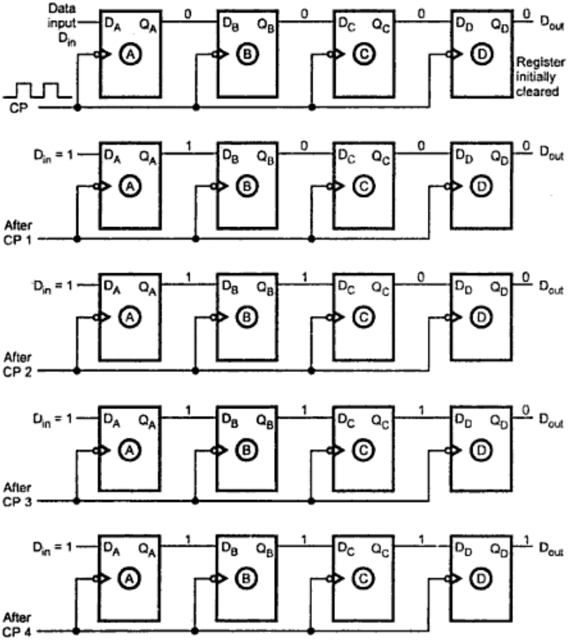

Data input D_{in}
CP
D_A Q_A A
D_B Q_B B
D_C Q_C C
D_D Q_D D
0 0 0 0 D_{out}
Register initially cleared
D_{in} = 1
1 0 0 0 D_{out}
After CP 1
D_{in} = 1
1 1 0 0 D_{out}
After CP 2
D_{in} = 1
1 1 1 0 D_{out}
After CP 3
D_{in} = 1
1 1 1 1 D_{out}
After CP 4

Fig. 7.7 Four bits 1111 being serially entered into shift-right register

7.3.2 Serial In Parallel Out Shift Register

In this case, the data bits are entered into the register in the same manner as discussed in the last section, i.e. serially. But the output is taken in parallel. Once the data are stored, each bit appears on its respective output line and all bits are available simultaneously, instead of on a bit-by-bit basis as with the serial output as shown in Fig. 7.8.

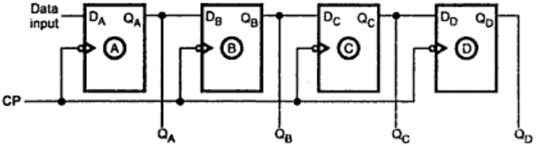

Data input
CP
D_A Q_A A
D_B Q_B B
D_C Q_C C
D_D Q_D D
Q_A
Q_B
Q_C
Q_D

Fig. 7.8 A serial in parallel out shift register

7.3.3 Parallel In Serial Out Shift Register

In this type, the bits are entered in parallel i.e simultaneously into their respective stages on parallel lines.

Fig. 7.9 illustrates a four-bit parallel in serial out register. There are four input lines X_A, X_B, X_C, X_D for entering data in parallel into the register. SHIFT/$\overline{\text{LOAD}}$ is the control input which allows shift or loading data operation of the register. When SHIFT/$\overline{\text{LOAD}}$ is low, gates G_1, G_2, G_3 are enabled, allowing each input data bit to be applied to D input of its respective flip-flop. When a clock pulse is applied, the flip-flops with D = 1 will SET and those with D = 0 will RESET. Thus all four bits are stored simultaneously.

When SHIFT/$\overline{\text{LOAD}}$ is high, gates G_1, G_2, G_3 are disabled and gates G_4, G_5, G_6 are enabled. This allows the data bits to shift left from one stage to the next. The OR gates at the D-inputs of the flip-flops allow either the parallel data entry operation or shift operation, depending on which AND gates are enabled by the level on the SHIFT/$\overline{\text{LOAD}}$ input.

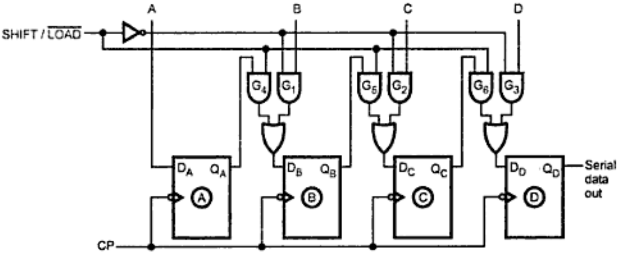


Fig. 7.9 Parallel in serial out shift register

7.3.4 Parallel In Parallel Out Shift Register

From the third and second types of registers, it is cleared that how to enter the data in parallel i.e. all bits simultaneously into the register and how to take data out in parallel from the register. In 'parallel in parallel out register', there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously. Fig. 7.10 shows this type of register.

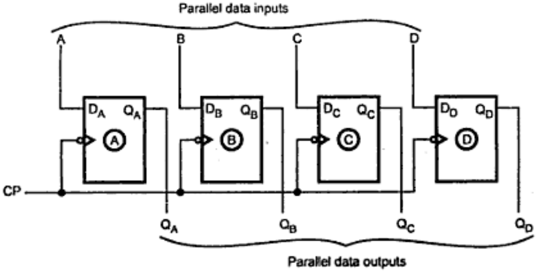


Fig. 7.10 Parallel in parallel out shift register

7.3.5 Bidirectional Shift Register

This type of register allows shifting of data either to the left or to the right side. It can be implemented by using logic gate circuitry that enables the transfer of data from one stage to the next stage to the right or to the left, depending on the level of a control line. Fig. 7.11 illustrates a four-bit bidirectional register. The RIGHT/$\overline{\text{LEFT}}$ is the control input signal which allows data shifting either towards right or towards left. A high on this line enables the shifting of data towards right and a low enables it towards left. When RIGHT/$\overline{\text{LEFT}}$ signal is high, gates G_1, G_2, G_3, G_4 are enabled. The state of the Q output of

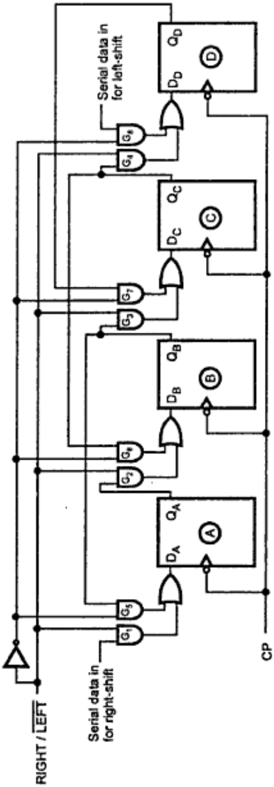

Serial data in for left-shift
Q_D
D_D
D
G_8
G_4
Q_C
D_C
C
G_7
G_3
Q_B
D_B
B
G_6
G_2
Q_A
D_A
A
G_5
G_1
Serial data in for right-shift
RIGHT / $\overline{\text{LEFT}}$
CP

Fig. 7.11 4-bit bidirectional shift register each flip-flop is passed through the D input of the following flip-flop. When a clock pulse arrives, the data are shifted one place to the right. When the RIGHT/$\overline{\text{LEFT}}$ signal is low, gates G_5, G_6, G_7, G_8 are enabled. The Q output of each flip-flop is passed through the D input of the preceding flip-flop. When clock pulse arrives, the data are shifted one place to the left.

Bidirectional Shift Register With Parallel Load

We have seen that shift register can be used for converting serial data into parallel data, and vice-versa. When parallel load capability is added to the shift register, the data entered in parallel can be taken out in serial fashion by shifting the data stored in the register. Such a register is called bidirectional shift register with parallel load. Fig. 7.12 shows bidirectional shift register with parallel load.

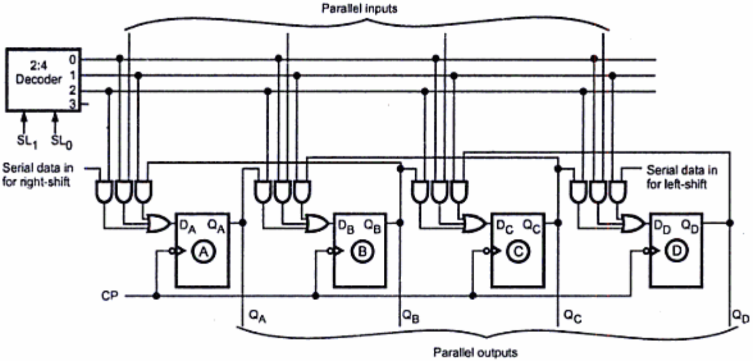


Fig. 7.12 4-bit bidirectional shift register with parallel load

As shown in the Fig. 7.12, the D input of each flip-flop has three sources : Output of left adjacent flip-flop, output of right adjacent flip-flop and parallel input. Out of these three sources one source is selected at a time and it is done with the help of decoder. The decoder select lines (SL_1 and SL_0) select the one source out of three as shown in the Table 7.1.

SL_1	SL_0	Selected source
0	0	Parallel input
0	1	Output of right adjacent FF
1	0	Output of left adjacent FF
1	1	–

Table 7.1

The Fig. 7.14 shows the 4-bit universal shift register. It has all the capabilities listed above. It consists of four flip-flops and four multiplexers. The four multiplexers have two common selection inputs S_1 and S_0, and they select appropriate input for D flip-flop. The Table 7.2 shows the register operation depending on the selection inputs of multiplexers. When $S_1S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in the register value. When $S_1S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift register. When $S_1S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left-shift register. Finally, when $S_1S_0 = 11$, the binary information on the parallel input lines is transferred into the register simultaneously and it is a parallel load operation.

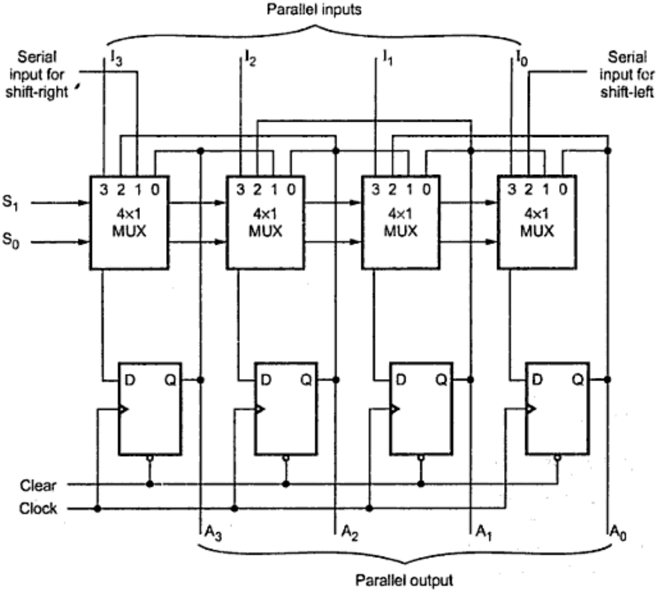

Parallel inputs
Serial input for shift-right
I3
I2
I1
I0
Serial input for shift-left
3 2 1 0
4×1 MUX
S1
S0
D
Q
Clear
Clock
A3
A2
A1
A0
Parallel output

Fig. 7.14 4-bit universal shift register

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	Shift-right

1	0	Shift-left
1	1	Parallel load

Table 7.2 Mode control and register operation

7.4 Applications of Shift Registers

We have seen that primary use of shift register is temporary data storage and bit manipulations. Some of the common applications of shift registers are as discussed below.

7.4.1 Delay Line

A serial-in-serial-out (SISO) shift register can be used to introduce time delay Δt in digital signals. The time delay can be given as,

$$\Delta t = N \times \frac{1}{f_c}$$

where N is the number of stages (i.e. flip-flops) and f_c is the clock frequency.

Thus, an input pulse train appears at the output delayed by Δt. The amount of delay can be controlled by the clock frequency or by the number of flip-flops in the shift register.

7.4.2 Serial-to-Parallel Converter

A serial-in-parallel-out (SIPO) shift register can be used to convert data in the serial form to the parallel form.

7.4.3 Parallel-to-Serial Converter

A parallel-in-serial-out (PISO) shift register can be used to convert data in the parallel form to the serial form.

7.4.4 Shift Register Counters

A shift register can also be used as a counter. A shift register with the serial output connected back to the serial input is called **shift register counter**. Because of such a connection, special specified sequences are produced as the output. The most common shift register counters are the ring counter and the Johnson counter.

7.4.5 Pseudo-Random Binary Sequence (PRBS) Generator

Another important application of shift register is a pseudo-random binary sequence generator. Here, suitable feedback is used to generate pseudo-random sequence. The term random here means that the outputs do not cycle through a normal binary count sequence. The term pseudo here refers to the fact that the sequence is not truly random because it does cycle through all possible combinations once every $2^n - 1$ clock cycles, where n represents the number of shift register stages (number of flip-flops).

7.4.6 Sequence Generator

The shift register can be used to generate a particular bit pattern repetitively. The Fig. 7.15 shows the basic block diagram of a sequence generator. Here, left most flip-flop input accept the serial input and the right most flip-flop gives serial data output. It is important to note that the serial data output signal is connected as a serial data in. On every clock pulse the data shift operation takes place. We get the loaded bit pattern at the serial output in a sequence. Same bit pattern is again loaded in the register since serial output is connected serial in of the register. Thus, the circuit generates a particular bit pattern repetitively.

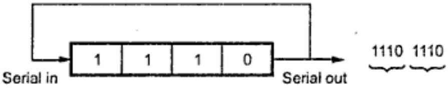
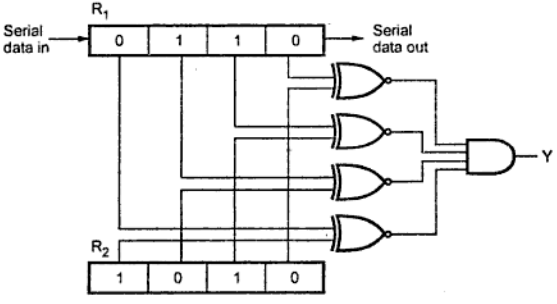


Fig. 7.15 4-bit sequence generator

7.4.7 Sequence Detector

The shift register can be used to detect the desired sequence. The detection process requires two resistors : one register stores the bit pattern to be detected i.e. R_1 and other register accepts the input data stream i.e. R_2. Input data stream enters a shift register as serial data in and leaves as serial out. In every clock cycle, bit-wise comparisons of these two registers are done using EX-NOR gates as shown in the Fig. 7.16. We know that, the two-input EX-NOR gate gives logic high output when both inputs are either low or high, i.e. when both are equal. When outputs of all the EX-NORs gates are logic high we can say that all bits are matched and hence the desired bit pattern is detected. The final output which indicates that the pattern is detected is taken from four-input AND gate.

The 4-bit sequence detector shown in Fig. 7.16 can be made programmable by loading the desired 4-bit data in the register R_2.



Bit-pattern to be detected

Fig. 7.16 4-bit sequence detector

7.4.8 Serial Adder/Subtractor

The Fig. 7.17 shows the logic diagram of serial adder. Using the logic diagram shown in Fig. 7.17 we can add numbers stored in the right shift registers A and B, serially. The full-adder is used to perform bit by bit addition and D-flip-flop is used to store the carry output generated after addition. This carry is used as carry input for the next addition. Initially, the D-flip-flop is cleared and addition starts with the least significant bits of both register. After each clock pulse data within the right shift registers are shifted right 1-bit and we get bits from next digit and carry of previous addition as new inputs for the full-adder. The result SUM is stored bit by bit in the register A.

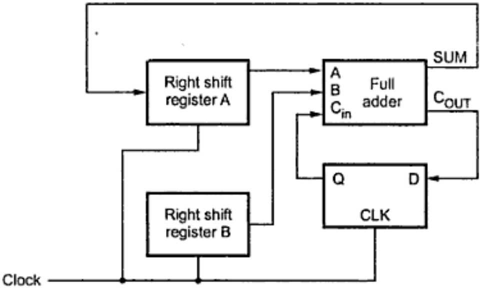


Fig. 7.17 Serial adder

We can implement serial subtractor by replacing full-subtractor instead of full-adder in the Fig. 7.17. Here, we will get difference and borrow instead of sum and carry.

7.5 MSI Shift Registers

7.5.1 4-bit Parallel Access Shift Registers (7495)

IC 7495 is 4-bit shift register with parallel and serial inputs, parallel output mode control and two clock inputs. The Fig. 7.18 (a) shows pin diagram and logic diagram of 7495. It can be operated in three modes :

- Parallel load
- Shift-right (the direction Q_A towards Q_D)
- Shift-left (the direction Q_D towards Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. When the mode control input is held high, the AND gate on the right input to each NOR gate is enabled while the left AND gate is disabled. The data is loaded into associated flip-flops and appears at the output after the negative transition of clock 2 input. During paralled loading, the entry of serial data is inhibited.

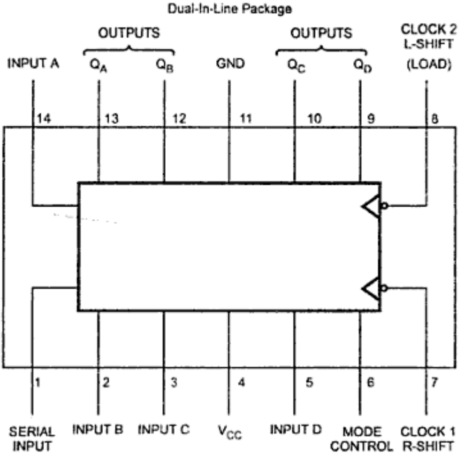

Dual-In-Line Package
OUTPUTS
OUTPUTS
CLOCK 2
L-SHIFT
(LOAD)
INPUT A
Q_A
Q_B
GND
Q_C
Q_D
14
13
12
11
10
9
8
1
2
3
4
5
6
7
SERIAL INPUT
INPUT B
INPUT C
V_CC
INPUT D
MODE CONTROL
CLOCK 1
R-SHIFT

Fig. 7.18 (a) Pin diagram

When the mode control input is low, the AND gate on the right input to each NOR gate is disabled while the left AND gate is enabled. The data input to flip-flop Q_A is now at serial input; the data input to Q_B is Q_A and so on down the line. On each negative clock1 transition, a data bit is entered serially into the register at the first flip-flop Q_A, and each stored data bit is shifted one flip-flop to the right (towards the last flip-flop Q_D). This is the serial input of data, and also the right-shift operation.

For left-shift operation, serial data input must be connected to the data input pin D, as shown in Fig. 7.18 (b). (See Fig. 7.18 (b) on next page.) It is also necessary to connect Q_D to C, Q_C to B, and Q_B to A. Now when the mode control input is held high, a data bit will be entered into flip-flop Q_D and each stored data bit will be shifted one flip-flop to the left on each negative clock 2 transition.

There are two separated clocks for left-shift and right-shift operation, When separate clocks are not required, the clock input may be applied simultaneously to clock 1 and clock 2.

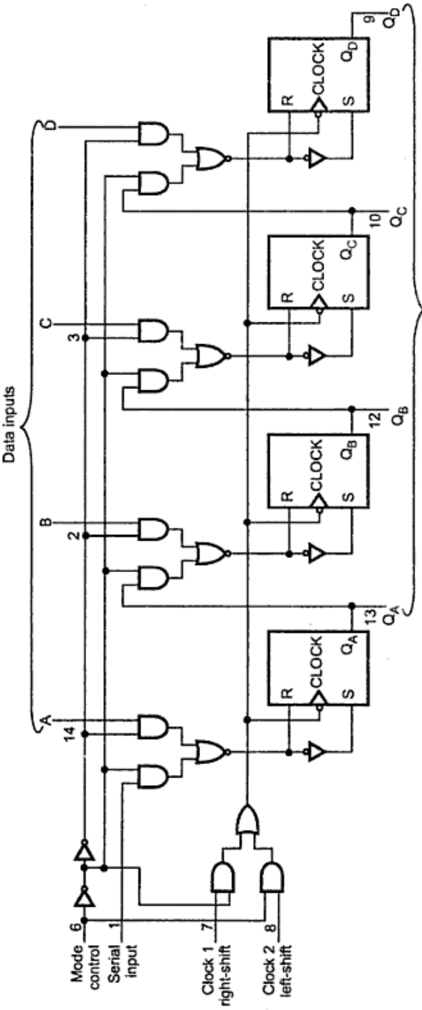

Data inputs
A
14
B
2
C
3
D
R
CLOCK
S
Q_A
13
Q_B
12
Q_C
10
Q_D
9
Outputs
Mode control
6
Serial input
1
Clock 1 right-shift
7
Clock 2 left-shift
8

Fig. 7.18 (b) Logic diagram

The Table 7.3 shows the funciton table for 7495.

Inputs								Outputs				Function
Mode control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D	
	2 (L)	1(R)		A	B	C	D					
H	↓	X	X	a	b	c	d	a	b	c	d	Parallel load
H	↓	X	X	$Q_B^{\bullet}$	$Q_C^{\bullet}$	$Q_D^{\bullet}$	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d	Shift-left
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Shift-right
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Shift-right

• Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

↓ = Transition from high to low level. ↑ = Transition from low to high level.

a,b,c,d = The level of steady state input at inputs A,B,C or D respectively.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C or Q_D respectively, before the most recent ↓ transition of the clock.

Table 7.3 Function table

7.5.2 Parallel Access Shift Register (74195)

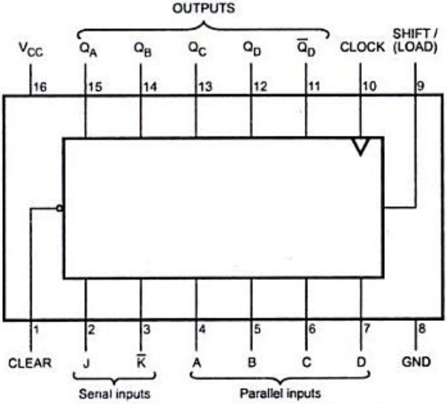


Fig. 7.19 (a) Pin diagram of 74195

The 74195 is 4-bit register with parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. It can be used for parallel in-parallel out operation. Since it also has a serial input; it can be used for serial in-serial out and serial in-parallel out operation. It can also be used for parallel in-serial output operation by using Q_D as the output. This register basically has two modes of operation.

- Parallel load
- Shift (in the direction Q_A toward Q_D)

The Fig. 7.19 (a) shows the pin diagram and Fig 7.19 (b) shows the logic diagram for 74195.

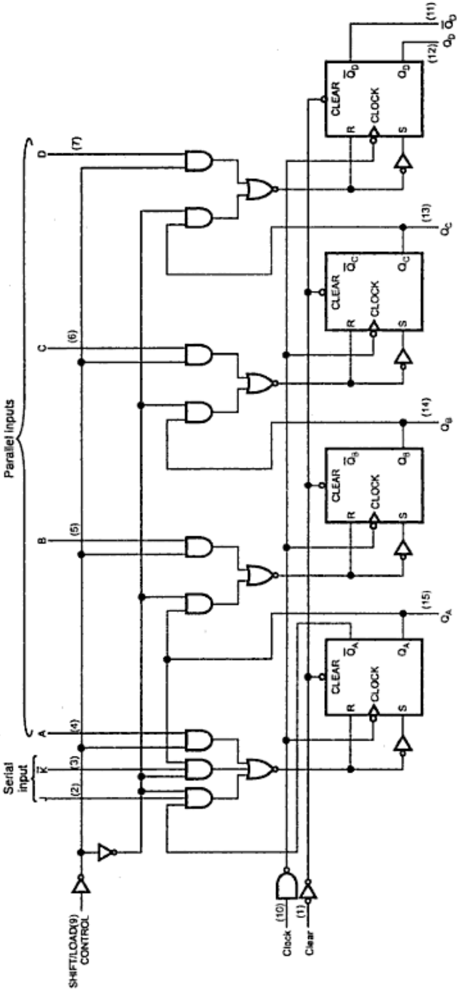

Parallel inputs
A (4)
B (5)
C (6)
D (7)
Serial input
J (2)
K̄ (3)
SHIFT/LOAD(9) CONTROL
Clock (10)
Clear (1)
CLEAR
CLOCK
R
S
Q_A
Q̄_A
Q_B
Q̄_B
Q_C
Q̄_C
Q_D
Q̄_D
(15) Q_A
(14) Q_B
(13) Q_C
(12) Q_D
(11) Q̄_D

Fig. 7.19 (b) Logic diagram of 74195

7.5.3 Universal Shift Register (IC 74194)

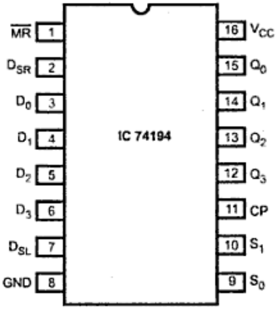

$\overline{MR}$ 1
D_{SR} 2
D_0 3
D_1 4
D_2 5
D_3 6
D_{SL} 7
GND 8
IC 74194
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 CP
10 S_1
9 S_0

Fig. 7.21 Pin configuration

We know that a register may operate in any of the modes, like, SISO, SIPO, PISO, PIPO or bidirectional. If a register can be operated in all the five possible ways, it is known as **Universal Shift Register.** The IC 74194 is a 4-bit universal shift register. Fig. 7.21 shows the pin configuration of IC 74194.

As shown in the Fig. 7.21, 74194 has 4 parallel data inputs (D_0-D_3), and S_0 and S_1 are the control inputs. When S_0 and S_1 are HIGH, data appearing on D_0-D_3 inputs is transferred to the Q_0-Q_3 outputs, respectively, following the next LOW to HIGH transition of the clock shift-right is accomplished by setting S_1S_0 = 01, and serial data is entered at the shift-right serial input, D_{SR}. Shift-left is accomplished by setting S_1S_0 = 10, and serial data is entered at the shift-left serial input, D_{SL}.

Fig. 7.22 shows the logic diagram and function table of IC 74194.

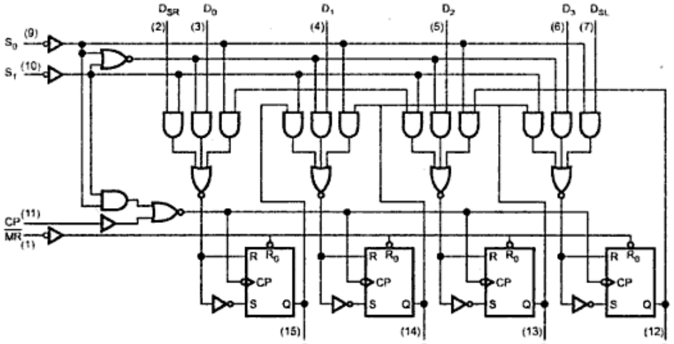
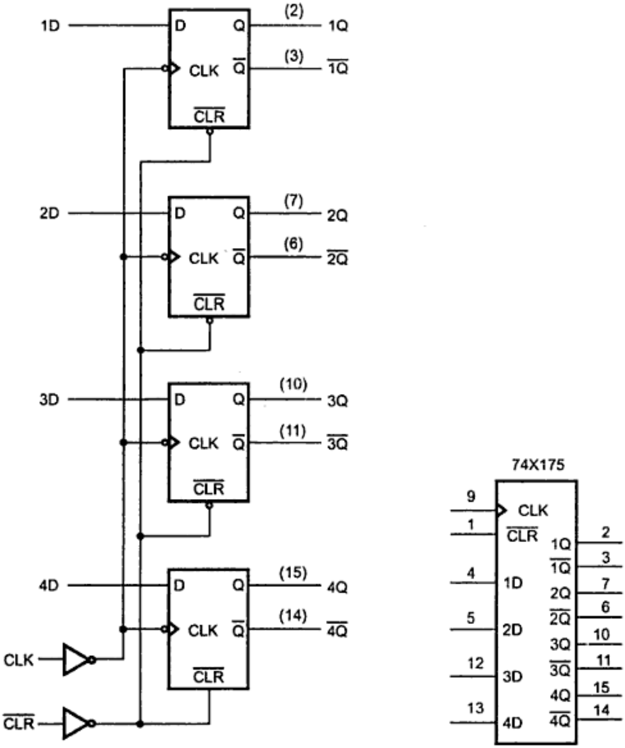

D_{SR}
(2)
D_0
(3)
D_1
(4)
D_2
(5)
D_3
(6)
D_{SL}
(7)
S_0 (9)
S_1 (10)
CP (11)
$\overline{MR}$ (1)
R R_0
CP
S
Q
(15)
Q_0
(14)
Q_1
(13)
Q_2
(12)
Q_3

Fig. 7.22 Logic diagram of 74194

7.6 MSI Registers

IC 74X175

The Fig. 7.24 shows the logic symbol and logic diagram for a commonly used MSI register, the 74X175. The 74X175 contains four negative edge-triggered D flip-flops with a common clock and asynchronous clear inputs. It provides both active-high and active-low outputs.


1D
2D
3D
4D
CLK
$\overline{CLR}$
D
Q
CLK
$\overline{Q}$
$\overline{CLR}$
(2)
1Q
(3)
$\overline{1Q}$
(7)
2Q
(6)
$\overline{2Q}$
(10)
3Q
(11)
$\overline{3Q}$
(15)
4Q
(14)
$\overline{4Q}$
74X175
9
1
4
5
12
13
2
3
7
6
10
11
15
14

(a) Logic diagram (b) Logic symbol

Fig. 7.24 IC 74X175

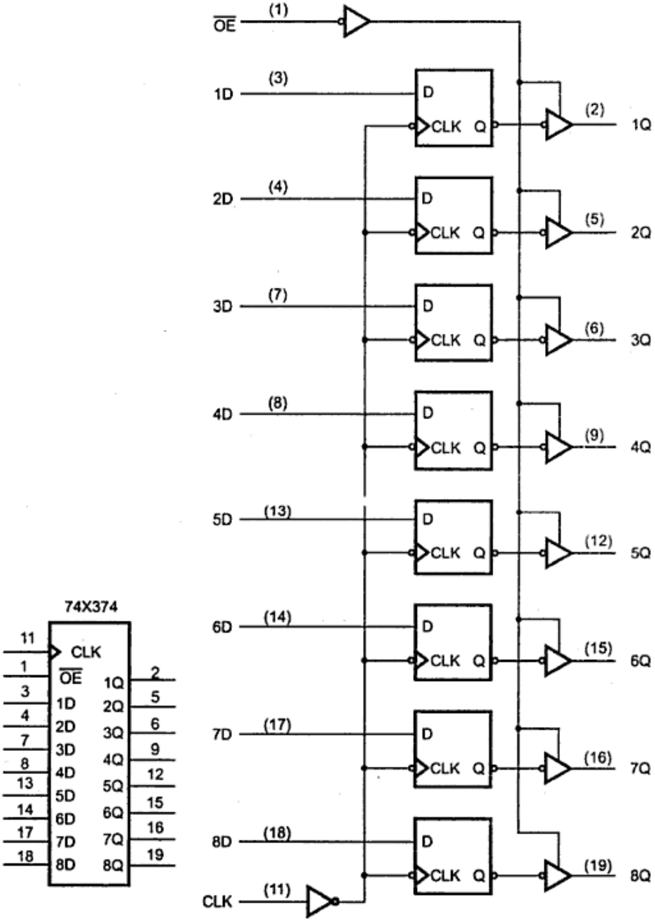

OE
(1)
1D
(3)
D
CLK
Q
(2)
1Q
2D
(4)
(5)
2Q
3D
(7)
(6)
3Q
4D
(8)
(9)
4Q
5D
(13)
(12)
5Q
6D
(14)
(15)
6Q
7D
(17)
(16)
7Q
8D
(18)
(19)
8Q
CLK
(11)
74X374
11
CLK
1
OE
3
1D
4
2D
7
3D
8
4D
13
5D
14
6D
17
7D
18
8D
1Q
2
2Q
5
3Q
6
4Q
9
5Q
12
6Q
15
7Q
16
8Q
19

Fig. 7.26 IC 74X134, 8-bit register

IC 74X273

The Fig. 7.28 shows logic symbol for IC 74X273. The IC 74X273 is a 8-bit register with a non tri-state outputs and no $\overline{\text{OE}}$ input; instead, it provides an asynchronous clear input $\overline{\text{CLR}}$.

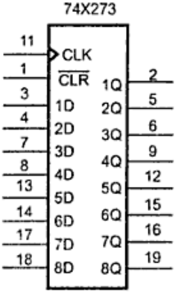
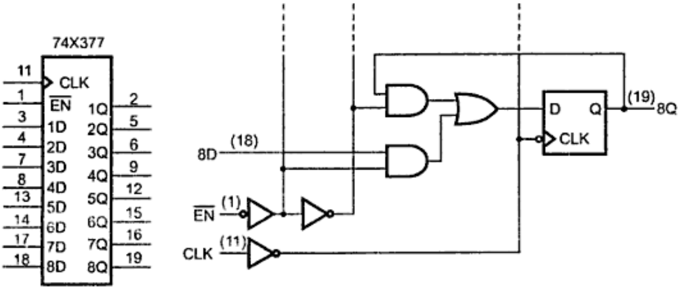

74X273
11
CLK
1
$\overline{\text{CLR}}$
3
1D
4
2D
7
3D
8
4D
13
5D
14
6D
17
7D
18
8D
1Q
2
2Q
5
3Q
6
4Q
9
5Q
12
6Q
15
7Q
16
8Q
19

Fig. 7.28 Logic symbol for the 74X273 8-bit register

IC 74X377

The Fig. 7.29 (a) shows the logic symbol for IC 74X377. It is an edge-triggered register like 74X374, but it does not have tri-state outputs. Instead, it provides active-low clock-enable input $\overline{\text{EN}}$. If $\overline{\text{EN}}$ is asserted (Low) at the rising edge of the clock, then the flip-flops are loaded from the data inputs; otherwise, they retain their present values. The Fig. 7.29 (b) shows the logic diagram for one flip-flop stage.


74X377
11
CLK
1
$\overline{\text{EN}}$
3
1D
4
2D
7
3D
8
4D
13
5D
14
6D
17
7D
18
8D
1Q
2
2Q
5
3Q
6
4Q
9
5Q
12
6Q
15
7Q
16
8Q
19
8D
(18)
$\overline{\text{EN}}$
(1)
CLK
(11)
D
Q
CLK
(19)
8Q

(a) Logic symbol

(b) Logical behaviour of one bit

Fig. 7.29 The 74X377 8-bit register with gated clock

Review Questions

1. *Draw and explain the operation of controlled buffer register.*
2. *List the basic types of shift registers interms of data movement.*
3. *Explain the operation of 4-bit serial-in-serial-out shift register with the help of neat diagram.*
4. *Draw and explain 4-bit serial-in-parallel-out shift register.*
5. *The binary number 10111011 is serially left-shifted into an eight-bit parallel out shift register that has an initial content of 10101010. a) What are the Q outputs after two clock pulses? b) After four clock pulses ? c) After eight clock pulses ?*

   (Ans : a) 10101010 b) 10101011 c) 10111011)
6. *An eight-bit bidirectional shift register contains 11011101. Zeros are applied to the shift-right and shift-left serial data inputs. The shift register is in the shift-right mode for three clock pulses, then in the shift-left mode for five clock pulses, then in the shift-right mode for one clock pulse. What is the final state of the register question ?* **(Ans. : 00110000)**
7. *Draw and explain the operation of parallel-in-parallel-out shift register.*
8. *Explain the operation of 4-bit bidirectional shift register with the help of neat diagram.*
9. *State various applications of shift register.*

❑❑❑

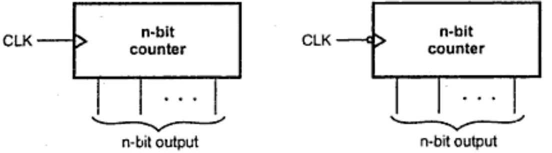
8

Counters

8.1 Introduction

A group of flip-flops connected together forms a **register.** A register is used solely for storing and shifting data which is in the form of 1s and/or 0s, entered from an external source. It has no specific sequence of states except in certain very specialized applications. A **counter** is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. On arrival of each clock pulse, the counter is incremented by one. In case of down counter, it is decremented by one.

The Fig. 8.1 shows the logic symbol of a binary counter. External clock is applied to the clock input of the counter. The counter can be positive edge triggered or negative edge triggered. The n-bit binary counter has n flip-flops and it has 2^n distinct states of outputs. For example, 2-bit counter has 2 flip-flops and it has $4(2^2)$ distinct states : 00, 01, 10 and 11. Similarly, the 3-bit binary counter has 3 flip-flops and it has $8\,(2^3)$ distinct states : 000, 001, 010, 011, 100, 101 110 and 111.



(a) Positive edge triggered n-bit counter

(b) Negative edge triggered n-bit counter

Fig. 8.1 Logic symbol of counter

The maximum count that the binary counter can count is 2^{n-1}. For example, in 2-bit binary counter, the maximum count is $2^2 - 1 = 3$ (11 in binary). After reaching the maximum count the counter resets to 0 on arrival of the next clock pulse and it starts counting again.

➡ **Example 8.1 :** *Assume that the 4-bit counter starts in the 0000 state. What will be the count after 12 input pulses ?*

Solution : After 12 pulses, the count will be $(1100)_2$, i.e. 12 in decimal.

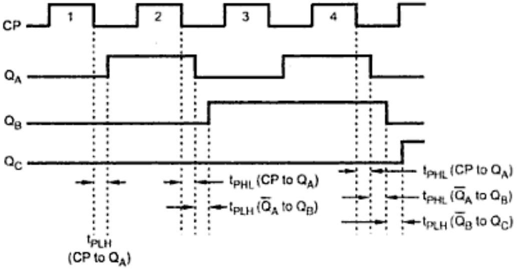


Fig. 8.4 Propagation delays in a ripple clocked binary counter

The timing diagram shows propagation delays. We can see that propagation delay of the first stage is added in the propagation delay of second stage to decide the transition time for third stage. This cumulative delay of an asynchronous counter is a major disadvantage in many applications because it limits the rate at which the counter can be clocked and creates decoding problems.

Example 8.4 : *Draw the logic diagram for 3-stage asynchronous counter with negative edge triggered flip-flops.*

Solution : When flip-flops are negatively edge triggered, the Q output of previous stage is connected to the clock input of the next stage. Fig. 8.5 shows 3-stage asynchronous counter with negative edge triggered flip-flops.

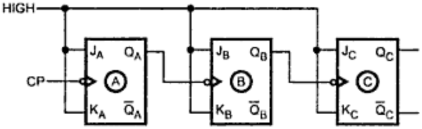


Fig. 8.5 Logic diagram of 3-stage negative edge triggered counter

Example 8.5 : *A counter has 14 stable states 0000 through 1101. If the input frequency is 50 kHz what will be its output frequency?*

Solution :

$$\frac{50\,\text{kHz}}{14} = 3.57\,\text{kHz}$$

Example 8.6 : *The t_{pd} for each flip-flop is 50 ns , determine the maximum operating frequency for MOD-32 ripple counter.*

Solution : We know that MOD-32 uses five flip-flops. With t_{pd} = 50 ns, the f_{max} for ripple counter can be given as,

$$f_{\max\,(\text{ripple})} = \frac{1}{5\times 50\,\text{ns}} = 4\text{ MHz}$$

8.2.1 Asynchronous/Ripple Down Counter

In the last section we have seen that the output of counter is incremented by one for each clock transition. Therefore, we call such counters as up **counters.** In this section we see the asynchronous/ripple down counter. The down counter will count downward from a maximum count to zero.

The Fig. 8.6 shows the 4-bit asynchronous down counter using JK flip-flops. Here, the clock signal is connected to the clock input of only first flip-flop. This connection is same as asynchronous/ripple up counter. However, the clock input of the remaining flip-flops is triggered by the $\overline{Q}_A$ output of the previous stage instead of Q_A output of the previous stage.

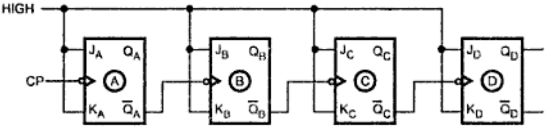
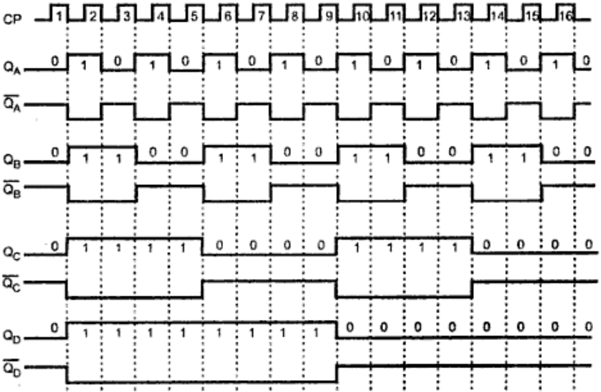

HIGH
CP
J_A Q_A
A
K_A Q̄_A
J_B Q_B
B
K_B Q̄_B
J_C Q_C
C
K_C Q̄_C
J_D Q_D
D
K_D Q̄_D

Fig. 8.6 4-bit asynchronous down counter

The Fig. 8.7 shows the timing diagram for 4-bit asynchronous down counter. It illustrates the changes in the state of the flip-flop outputs in response to the clock. Again the J and K inputs of JK flip-flops are tied to logic HIGH hence output will toggle for each negative edge of the clock input.


CP
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Q_A
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Q̄_A
Q_B
0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0
Q̄_B
Q_C
0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0
Q̄_C
Q_D
0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0
Q̄_D

Count																
	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000

Fig. 8.7 Timing diagram of 4-bit asynchronous down counter

Down counters are not as widely used as up counters. They are used in situations where it must be known when a desired number of input pulses has occurred. In these situations the down counter is preset to the desired number and then allowed to count down as the pulses are applied. When the counter reaches the zero state it is detected by a logic gate whose output then indicates that the preset number of pulses have occurred.

Example 8.7 : *For the ripple counter shown in Fig. 8.8, show the complete timing diagram for eight clock pulses, showing the clock, Q_0 and Q_1 waveforms.*

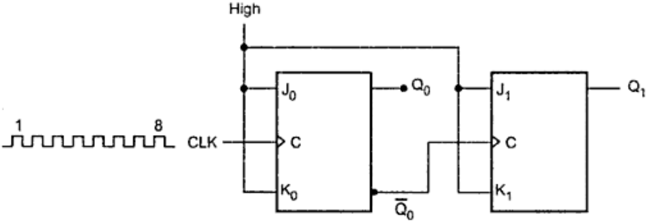


Fig. 8.8

Solution :

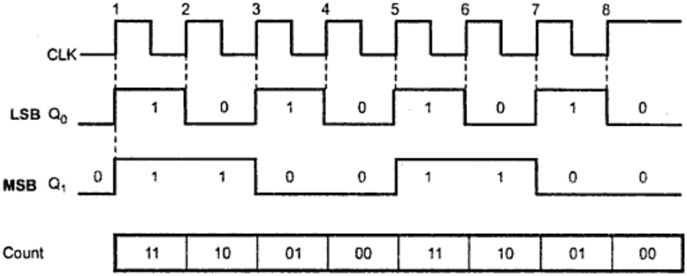


Fig. 8.9

8.2.2 Asynchronous Up/Down Counter

To form an asynchronous up/down counter one control input say M is necessary to control the operation of the up/down counter. When M = 0, the counter will count up and when M = 1, the counter will count down. To achieve this the M input should be used to control whether the normal flip-flop output (Q) or the inverted flip-flop output ($\overline{Q}$) is fed to drive the clock signal of the successive stage flip-flop, as shown in Fig. 8.10 (a). The truth table for such combinational circuit is shown in Fig. 8.10 (b).

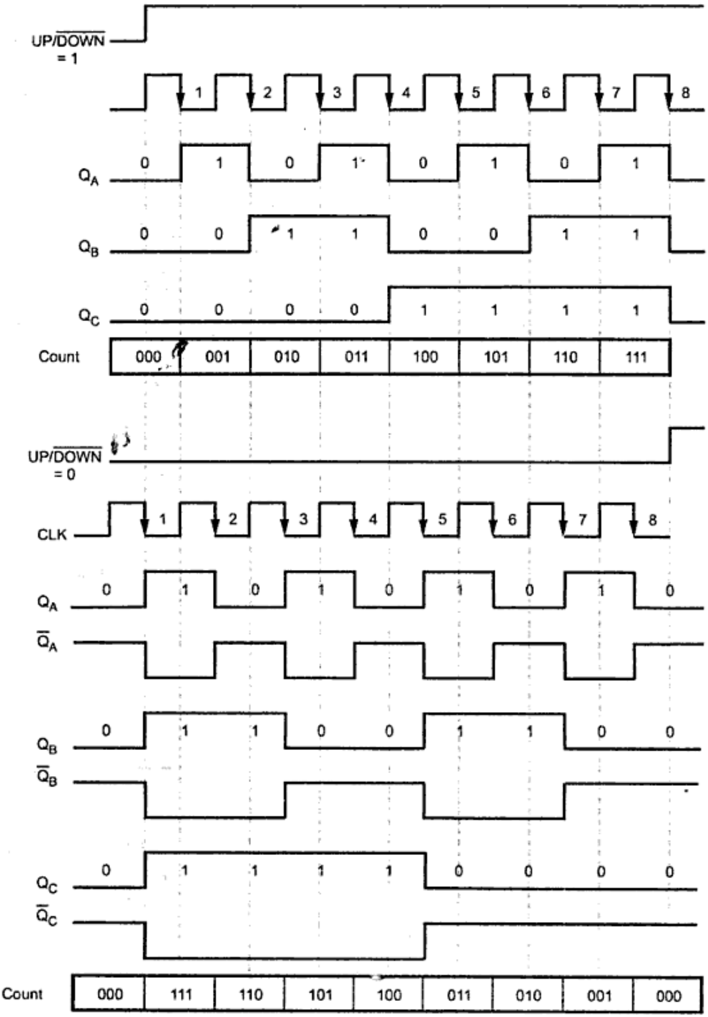

UP/$\overline{DOWN}$ = 1
1 2 3 4 5 6 7 8
Q_A 0 1 0 1 0 1 0 1
Q_B 0 0 1 1 0 0 1 1
Q_C 0 0 0 0 1 1 1 1
Count 000 001 010 011 100 101 110 111
UP/$\overline{DOWN}$ = 0
CLK 1 2 3 4 5 6 7 8
Q_A 0 1 0 1 0 1 0 1 0
$\overline{Q}_A$
Q_B 0 1 1 0 0 1 1 0 0
$\overline{Q}_B$
Q_C 0 1 1 1 1 0 0 0 0
$\overline{Q}_C$
Count 000 111 110 101 100 011 010 001 000

Fig. 8.13 Timing diagram for 3-bit UP/ $\overline{\text{DOWN}}$ ripple counter

Example 8.8 : *Design a 4-bit up/down ripple counter with a control for up/down counting.*

Solution : The 4-bit counter needs four flip-flops. The circuit for 4-bit up/down ripple counter is similar to 3-bit up/down ripple counter except that 4-bit counter has one more flip-flop and its clock driving circuiting.

The Fig. 8.14 shows the 4-bit up/down ripple counter.

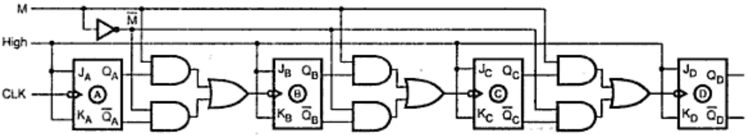

M
$\overline{M}$
High
CLK
J_A Q_A
A
K_A $\overline{Q}_A$
J_B Q_B
B
K_B $\overline{Q}_B$
J_C Q_C
C
K_C $\overline{Q}_C$
J_D Q_D
D
K_D $\overline{Q}_D$

Fig. 8.14 4-bit asynchronous up/down counter

8.2.3 IC 7492/93 (4-bit Ripple Counter)

The 7492 and 7493 are high speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-six (7492) or divide-by-eight (7493) section which are triggered by a HIGH to LOW transition on the clock inputs. Each section can be used separately or tied together to form divide-by-twelve or divide-by-sixteen counters.

The 7492 is 4-bit divide-by-twelve counter and 7493 is 4-bit binary counter. Each device consists of four master slave flip-flops which are internally connected to provide a divide-by-two section. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

Connection Diagram of 7492

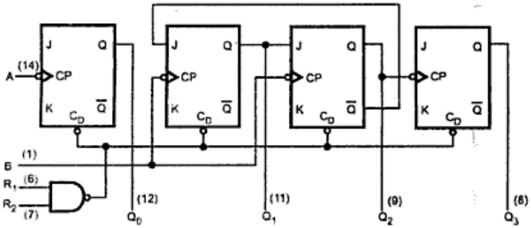
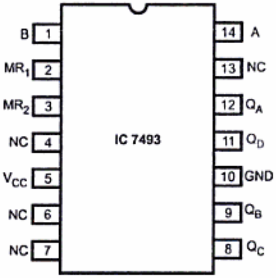

J
Q
CP
K
C_D
$\overline{Q}$
A
(14)
B
(1)
R_1
(6)
R_2
(7)
(12)
Q_0
(11)
Q_1
(9)
Q_2
(8)
Q_3

Fig. 8.15 (a)

Logic Diagram



NC : NO INTERNAL CONNECTION

NOTE :
The flat pack version has the
same pinouts (Connection diagram)
as the dual in-line package

Fig. 8.15 (d)

Modes of 7493

1. 4-Bit Ripple Counter :

The output Q_A must be externally connected to input B. The input count pulses are applied to the input A. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C and Q_D outputs as shown in the truth table.

2. 3-Bit Ripple Counter :

The input count pulses are applied to input A. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_B, Q_C and Q_D outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple through counter.

Table. 8.1 shows the truth tables for 7492 and 7493.

7492 and 7493

Reset Inputs		Outputs			
R_1	R_2	Q_A	Q_B	Q_C	Q_D
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

Table 8.1 (a)

MODE SELECTION

H : High Voltage Level
L : Low Voltage Level
X : Don't Care

Example 8.11 : *Design a divide-by-78 counter using 7493 and 7492 (as divide-by-6) counter ICs.*

Solution : Since 78 = 13 × 6, we have to use 7493 as mod-13 and 7492 as mod-6 counters. For the mod-13 counter Q_D, Q_C and Q_A outputs of 7493 are ANDed and used to clear the count when the count reaches 1101. For the mod-6 counter, clock is applied to B input of 7492.

The circuit diagram is as shown in the Fig. 8.19.

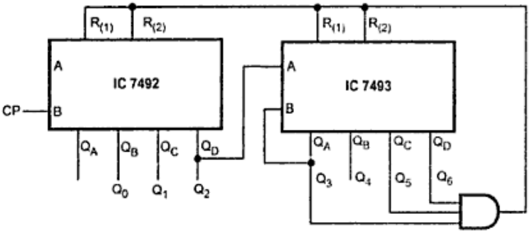

R(1)
R(2)
IC 7492
A
B
CP
QA
QB
QC
QD
Q0
Q1
Q2
R(1)
R(2)
IC 7493
A
B
QA
QB
QC
QD
Q3
Q4
Q5
Q6

Fig. 8.19 Divide-by-78 counter

Example 8.12 : *Design divide-by-6 counter using IC 7493.*

Solution : The Fig. 8.20 shows divide-by-6 (MOD 6) counter using 7493. As shown in the Fig. 8.20, the clock is applied to input B of IC 7493 and the output count sequence is taken from Q_D, Q_C and Q_B. As soon as count is 110, i.e. Q_D and Q_C = 1, the internal NAND gate output goes low and it resets the counter.

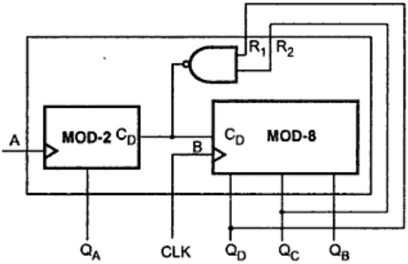

R1
R2
MOD-2
CD
A
B
CD
MOD-8
QA
CLK
QD
QC
QB

Fig. 8.20 Divide-by-6 counter using 7493

8.3 Decoding Gates

Decoding gates are used to indicate whether counter has reached to particular state. The outputs of the counter are connected to the AND gate as inputs and the output of the AND gate goes high for particular state. Let us see the Fig. 8.21 (a). Here, the output of decoding gate goes high when counter outputs are C = 1, B = 1 and A = 1. In Fig. 8.21 (b) the output of decoding gate goes high when counter outputs are C = 1, B = 0 and A = 0.

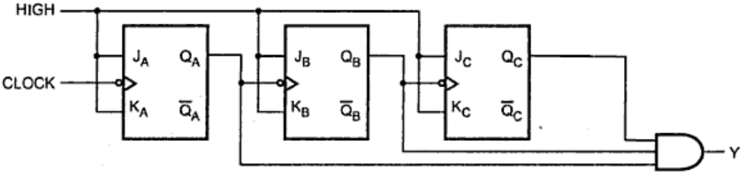

HIGH
CLOCK
J_A
Q_A
K_A
$\overline{Q}_A$
J_B
Q_B
K_B
$\overline{Q}_B$
J_C
Q_C
K_C
$\overline{Q}_C$
Y

Fig. 8.21 (a) Decoding gate to indicate state 7 (111)

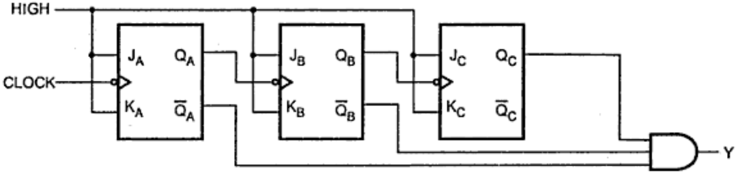

HIGH
CLOCK
J_A
Q_A
K_A
$\overline{Q}_A$
J_B
Q_B
K_B
$\overline{Q}_B$
J_C
Q_C
K_C
$\overline{Q}_C$
Y

Fig. 8.21 (b) Decoding gate to indicate state 4 (100)

Similarly, we can connect corresponding outputs to decoding gate inputs to indicate desired state. The Fig. 8.22 gives these connections for all possible state detection for 3-bit counter.

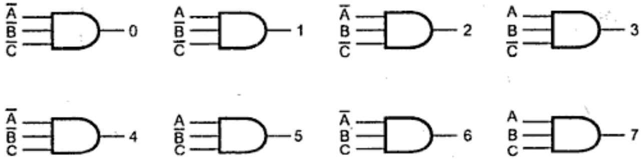

$\overline{A}$ $\overline{B}$ $\overline{C}$ 0
A $\overline{B}$ $\overline{C}$ 1
$\overline{A}$ B $\overline{C}$ 2
A B $\overline{C}$ 3
$\overline{A}$ $\overline{B}$ C 4
A $\overline{B}$ C 5
$\overline{A}$ B C 6
A B C 7

Fig. 8.22 Decoding gate connections

8.4 Problem Faced by Ripple Counters (Glitch Problem)

We know that, due to the propagation delay the output flip-flop is delayed by time t_p. This illustrated in the waveform shown in Fig. 8.23 shows the waveform of the circuit which decodes state 6. Here, the output of flip-flop A triggers the flip-flop B, hence the B waveform is delayed by one flip-flop delay time (t_p) from the negative transition of A. Similarly, the C waveform is delayed by t_p from each negative transition of B.

CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 8.2 State sequence for 3-bit binary counter

Looking at Fig. 8.26 (b), we can see that Q_A changes on each clock pulse as we progress from its original state to its final state and then back to its original state. To produce this operation, flip-flop A is held in the toggle mode by connecting J and K inputs to HIGH. Now let us see what flip-flop B does. Flip-flop B toggles, when Q_A is 1. When Q_A is a 0, flip-flop B is in the no-change mode and remains in its present state. Looking at the Table 8.2 we can notice that flip-flop C has to change its state only when Q_B and Q_A both are at logic 1. This condition is detected by AND gate and applied to the J and K inputs of flip-flop C. Whenever both Q_A and Q_B are HIGH, the output of the AND gate makes the J and K inputs of flip-flop C HIGH and flip-flop C toggles on the following clock pulse. At all other times, the J and K inputs of flip-flop C are held LOW by the AND gate output and flip-flop does not change state.

8.5.3 4-bit Synchronous Binary Up Counter

Fig. 8.27 (a) shows logic diagram and timing diagram for 4-bit synchronous binary counter. As counter is implemented with negative edge triggered flip-flops, the transitions occur at the negative edge of the clock pulse. In this circuit, first three flip-flops work same as 3-bit counter discussed previously.

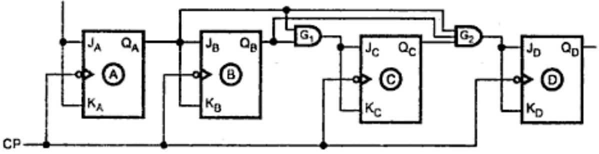


Fig. 8.27 (a)

For the fourth stage, flip-flop has to change the state when $Q_A = Q_B = Q_C = 1$. This condition is decoded by 3-input AND gate G_2. Therefore, when $Q_A = Q_B = Q_C = 1$, flip-flop D toggles and for all other times it is in no change condition.

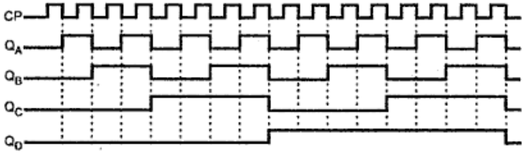


Fig. 8.27 (b) A four-bit synchronous binary counter and timing diagram

➡ **Example 8.13 :** *Determine f_{max} for the 4-bit synchronous counter if t_{pd} for each flip-flop is 50 ns and t_{pd} for each AND gate is 20 ns. Compare this with f_{max} for a MOD-16 ripple counter.*

Solution : For a synchronous counter the total delay that must be allowed between input clock pulses is equal to flip-flop t_{pd} + AND gate t_{pd}. Thus $T_{clock} \geq 50 + 20 = 70$ ns and so the counter has

$$f_{max} = \frac{1}{70\,\text{ns}} = 14.3\ \text{MHz}$$

We know that MOD-16 ripple counter used four flip-flops. With flip-flop $t_{pd} = 50$ ns, the f_{max} for ripple counter can be given as,

$$f_{max\,(ripple)} = \frac{1}{4 \times 50\,\text{ns}} = 5\ \text{MHz}$$

8.5.4 Synchronous Down and Up/Down Counters

We have seen that a ripple counter could be made to count down by using the inverted output of each flip-flop to drive the next flip-flops in the counter. A parallel/synchronous down counter can be constructed in a similar manner that is, by using the inverted FF outputs to drive the following JK inputs. For example, the parallel up counter of Fig. 8.27 (a) can be converted to a down counter by connecting the $\overline{Q}_A$, $\overline{Q}_B$, $\overline{Q}_C$ and $\overline{Q}_D$ outputs in place of Q_A, Q_B, Q_C and Q_D respectively. The counter will then proceed through the following sequence as input pulses are applied :

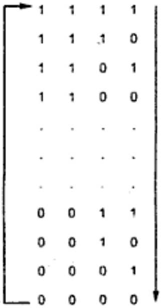


Fig. 8.28

To form a parallel up/down counter the control input (UP/$\overline{\text{DOWN}}$) is used to control whether the normal flip-flop outputs or the inverted flip-flop outputs are fed to the J and K inputs of the following flip-flops. The Fig. 8.28 shows 3-bit up/down counter that will count from 000 up to 111 when the up/$\overline{\text{Down}}$ control input is 1 and from 111 down to 000 when the Up/$\overline{\text{Down}}$ control input is 0.

A logic 1 on the Up/$\overline{\text{Down}}$ enables AND gates 1 and 2 and disables AND gates 3 and 4. This allows the Q_A and Q_B outputs through to the J and K inputs of the next flip-flops so that the counter will count up as pulses are applied. When Up/$\overline{\text{Down}}$ line is logic 0, AND gates 1 and 2 are disables and AND gates 3 and 4 are enabled. This allows the $\overline{Q}_A$ and $\overline{Q}_B$ outputs through to the J and K inputs of the next flip-flops so that the counter will count down as pulses are applied.

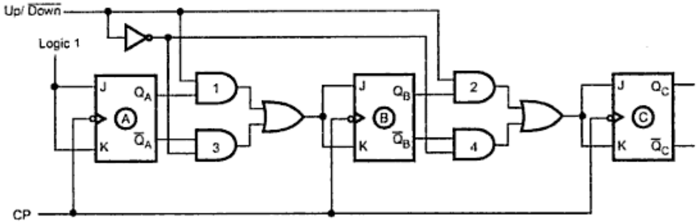


Fig. 8.29 3-bit synchronous/parallel up/down counter

8.5.5 Synchronous Vs Asynchronous Counters

The Table 8.3 shows the comparison between synchronous and asynchronous counters.

Sr. No.	Asynchronous Counters	Synchronous Counters
1.	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2.	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3.	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip-flops increases in the given design.

Table 8.3 Synchronous Vs asynchronous counters

Pin Description

1. **Data inputs :** D_0, D_1, D_2 and D_3 are the four data input lines with D_0 is LSB and D_3 is MSB. We can load data through these lines.
2. **$\overline{\text{PL}}$ (Parallel Load) :** On activation of this signal (active low) the data available on data inputs (D_0, D_1, D_2, D_3) is loaded into the counter and it is then available on output lines. The parallel load operation has higher priority than counting operation.
3. **Enable ($\overline{\text{G}}$) Input :** When this signal is low, counting is enabled and count is incremented or decremented according to status of Down/$\overline{\text{UP}}$ signal on each low to high transition of clock pulse applied to clock input. High on this input disables counting.
4. **Outputs :** Q_0, Q_1, Q_2 and Q_3 are the four output lines with Q_0 is LSB and Q_3 is MSB.
5. DOWN/$\overline{\text{UP}}$: This signal determines the direction of the counting . When this signal is high counter acts as a down counter; otherwise it acts as a up counter.
6. **CP (Clock) :** This is the clock input for the counter.
7. **Terminal Count :** As soon as the counter reaches its maximum (1111) or minimum (0000) count this signal goes high for one clock pulse.
8. **Ripple Clock ($\overline{\text{RC}}$) :** This is an active low output signal. It is used as the clock input for the next higher stage as shown in the Fig. 8.32.

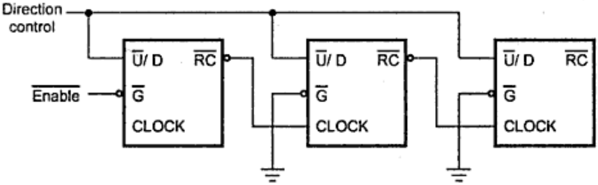
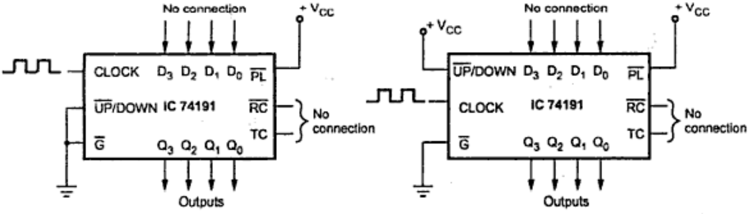

Direction control
$\overline{\text{Enable}}$
$\overline{\text{U}}$/ D
$\overline{\text{RC}}$
$\overline{\text{G}}$
CLOCK
$\overline{\text{U}}$/ D
$\overline{\text{RC}}$
$\overline{\text{G}}$
CLOCK
$\overline{\text{U}}$/ D
$\overline{\text{RC}}$
$\overline{\text{G}}$
CLOCK

Fig. 8.32 Ripple clock connections

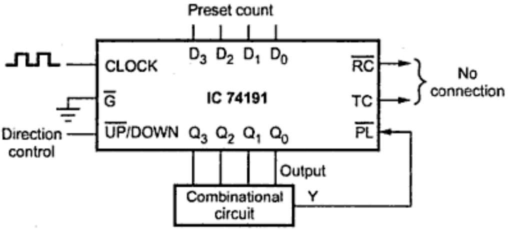
Connection Diagram for Different Operating Modes

The Fig. 8.33 shows the connection diagram of 74191 for various operating modes.

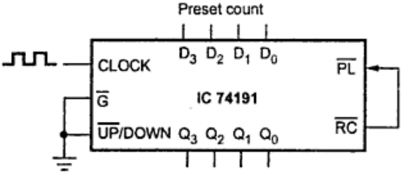

No connection
+ V_{CC}
CLOCK
D_3 D_2 D_1 D_0
$\overline{\text{PL}}$
$\overline{\text{UP}}$/DOWN
IC 74191
$\overline{\text{RC}}$
TC
No connection
$\overline{\text{G}}$
Q_3 Q_2 Q_1 Q_0
Outputs
+ V_{CC}
No connection
+ V_{CC}
$\overline{\text{UP}}$/DOWN
D_3 D_2 D_1 D_0
$\overline{\text{PL}}$
CLOCK
IC 74191
$\overline{\text{RC}}$
TC
No connection
$\overline{\text{G}}$
Q_3 Q_2 Q_1 Q_0
Outputs

(a) Connection for up counter

(b) Connection for down counter


Preset count
CLOCK
D3 D2 D1 D0
RC
No connection
G
IC 74191
TC
Direction control
UP/DOWN Q3 Q2 Q1 Q0
PL
Output
Combinational circuit
Y

(c) Presettable up/down counter


Preset count
CLOCK
D3 D2 D1 D0
PL
G
IC 74191
UP/DOWN Q3 Q2 Q1 Q0
RC

(d) Programmable frequency divider/mod counter

Fig. 8.33 Operating modes of IC 74191

TC and $\overline{RC}$ Function Table

The Table 8.5 shows TC and $\overline{RC}$ function table.

Inputs			Terminal Count State				Outputs	
$\overline{U}$/D	$\overline{G}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
1	1	X	1	1	1	1	0	1
0	1	X	1	1	1	1	1	1
0	0	⊔	1	1	1	1	⎺⎽	⊔
0	1	X	0	0	0	0	0	1
1	1	X	0	0	0	0	1	1
1	0	⊔	0	0	0	0	⎺⎽	⊔

Table 8.5 Function table for TC and $\overline{RC}$

Timing waveforms for 74191

Fig. 8.34 shows the timing waveforms for IC 74191.

Example 8.15 : *Design MOD-10 counter using IC 74191.*

Solution : Refer solution of example 8.14. Load 0110 instead of 0101 count.

Example 8.16 : *Design down counter, counting states from 1101 to 0011 using 4-bit synchronous counter IC 74LS191.*

Solution : The Fig. 8.36 shows the connections for 74LS191 to get desire operation. We can design the combinational circuit for such counter from the truth table shown in the Table 8.6.

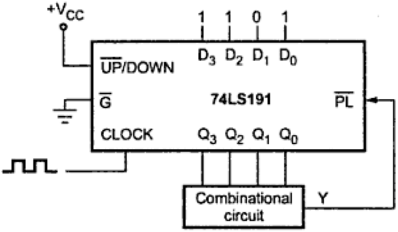

+V_CC
1 1 0 1
UP/DOWN
D_3 D_2 D_1 D_0
G
74LS191
PL
CLOCK
Q_3 Q_2 Q_1 Q_0
Combinational circuit
Y

Fig. 8.36

Q_3	Q_2	Q_1	Q_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Table 8.6

K-map simplification

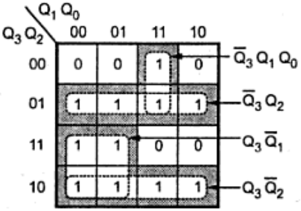

Q1 Q0
Q3 Q2
00
01
11
10
00
01
11
10
0
0
1
0
1
1
1
1
1
1
0
0
1
1
1
1
$\overline{Q}_3 Q_1 Q_0$
$\overline{Q}_3 Q_2$
$Q_3 \overline{Q}_1$
$Q_3 \overline{Q}_2$

Fig. 8.37

$$\therefore \qquad \overline{PL} = Y = \overline{Q}_3 Q_1 Q_0 + \overline{Q}_3 Q_2 + Q_3 \overline{Q}_1 + Q_3 \overline{Q}_2$$

Logic diagram for counter

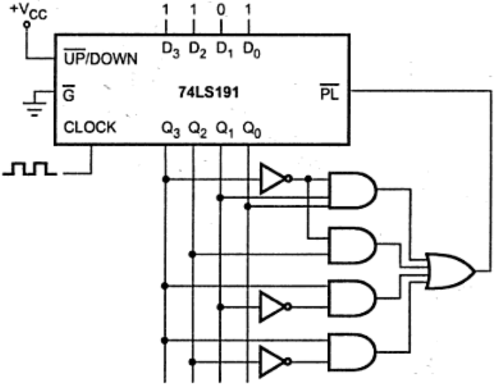

+VCC
1 1 0 1
UP/DOWN
D3 D2 D1 D0
G
74LS191
PL
CLOCK
Q3 Q2 Q1 Q0

Fig. 8.38

After switch ON, if the counter output is other than 1101 through 0011, the $\overline{PL}$ goes low and count 1101 is loaded in the counter. The counter is then decremented on the occurrence of clock pulses. When counter reaches 0010, the $\overline{PL}$ again goes low and count 1101 is loaded in the counter.

Example 8.17 : *How output frequency, f_{out} and clock frequency, f_{CLK} are related in case of binary counter, IC 74191 in up and down counting mode ? If f_{CLK} = 500 Hz and f_{out} = 50 Hz, design the programmable frequency divider using IC 74191 in up counting mode.*

Solution : The IC 74191 is a 4-bit binary counter, therefore $f_{out} = f_{CLK}/16$ in up and down counting mode. If f_{CLK} = 500 Hz and f_{out} = 50 Hz we need mod 10 (500/50) counter. The Fig. 8.39 shows the mod-10 counter using IC 74191.

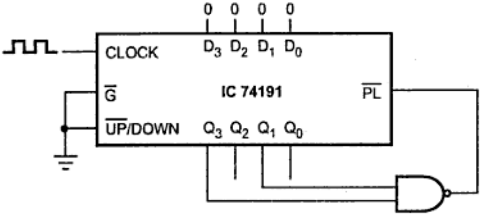

0 0 0 0
CLOCK
D3 D2 D1 D0
G
IC 74191
PL
UP/DOWN
Q3 Q2 Q1 Q0

Fig. 8.39

Example 8.18 : *Design a counter to count from 1110 to 0011 using 74191 IC.*

Solution : Refer similar example 8.16.

Example 8.19 : *Explain how IC 74191 can also be used as programmable frequency divider.*

Solution : IC 74191 is a 4-bit binary counter. Thus it divides the input frequency by 16. However, we can design MOD-N counter using IC 74191. For MOD-N counter the output frequency will be $f_{out} = \frac{f_{in}}{N}$. Thus by changing N we can change the output frequency. The Fig. 8.40 shows the programmable frequency divider using IC 74191.

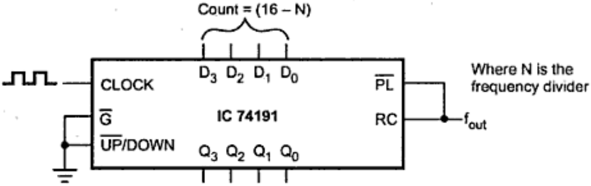

Count = (16 – N)
CLOCK
D3 D2 D1 D0
PL
Where N is the frequency divider
G
IC 74191
RC
fout
UP/DOWN
Q3 Q2 Q1 Q0

Fig. 8.40 Programmable frequency divider

Example 8.20 : *Design divide-by-2 for upcounting and divide-by-5 for down counting using frequency divider IC 74191.*

Solution : Divide-by for up counting

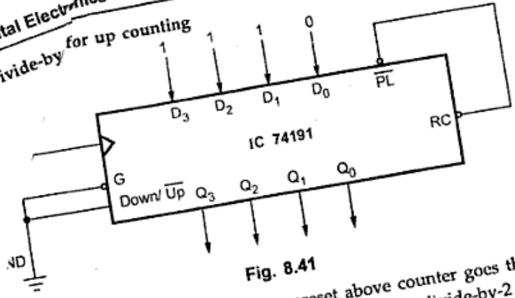

1
1
1
0
D3
D2
D1
D0
PL
RC
IC 74191
G
Down/ Up
Q3
Q2
Q1
Q0
ND

Fig. 8.41

-by-2 is a mod-2 counter. Since, after preset above counter goes through 2 states 1111, it is a mod-2 counter. Thus, above circuit is a divide-by-2 counter for up ode.

y-5 for down counting mode :

ary
ate
h
e
r

		Q1	Q0	Y
		0	0	0
		0	1	0
		1	0	0
	0	1	1	0
	1	0	0	0
	1	0	1	0
	1	1	0	0
	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Truth table

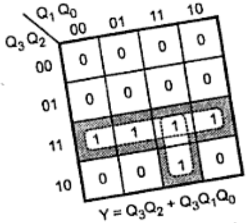

Q1 Q0
Q3 Q2
00
01
11
10
$Y = Q_3Q_2 + Q_3Q_1Q_0$

Fig. 8.42 K-map simplification

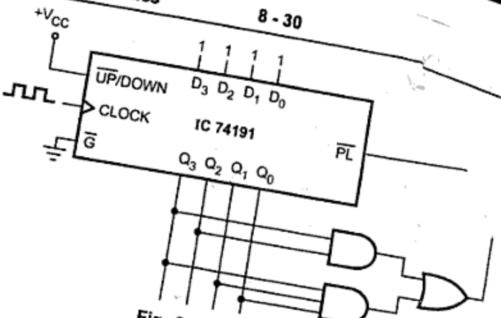


Fig. 8.43 Logic diagram

Example 8.21 : *Design mod 9 counter using IC 74191.*

Solution : Refer example 8.14.

8.6 Changing the Counter Modulus

Fig. 8.45 shows basic 3-bit ripple counter. In its basic form it is a MOD-8 bin counter which count in sequence from 000 to 111. However, the presence of NAND g will alter this sequence as follows :

1. The NAND gate output is connected to the asynchronous RESET inputs of ea flip-flop. As long as the NAND output is HIGH, it will have no effect on th counter. When it goes LOW, it will reset all the flip-flops so that counte immediately goes to the 000 state.
2. The inputs for the NAND gate are the outputs of the A and C flip-flops and so the NAND output will go LOW whenever $Q_A = Q_C = 1$. This condition will occur when the counter goes from the 100 state to the 101 state (input pulse 5 on waveforms). The LOW at the NAND output will immediately (generally within a few nanoseconds) reset the counter to the 000 state. Once the flip-flops have been reset, the NAND output goes back HIGH, since the $Q_A = Q_C = 1$ condition no longer exists.

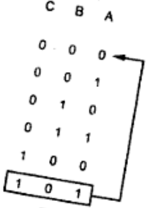
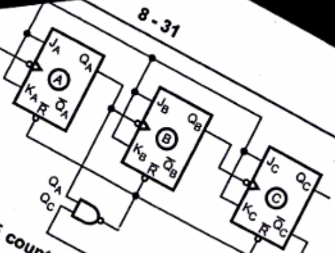
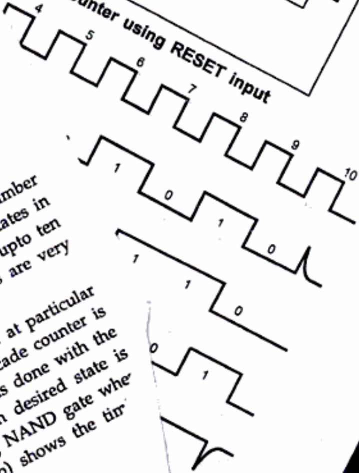


Fig. 8.44

3. The counting sequence is 000 through 101 therefore, though the counter does go to the 101 state, it remains there for only a few nanoseconds before it recycles to 000. Thus, we can essentially say that the counter counts from 000 to 100 and then recycles to 000. Due to this counter skips 101, 110, and 111 states and it goes through only five different states; thus it is a MOD-5 counter.


JA
QA
A
KA
R̄
Q̄A
JB
QB
B
KB
R̄
Q̄B
JC
QC
C
KC
R̄
Q̄C
QA
QC

8.45 MOD-5 counter using RESET input


4
5
6
7
8
9
10
1
0
1
0
1
1
0
0
1

ere n is the number
n number of states in
e is truncated upto ten
pe of counters are very

ng the counter at particular
se of BCD decade counter is
ng of counter is done with the
activated when desired state is
activated using NAND gate whe
(a). Fig. 8.47 (b) shows the tim

. The

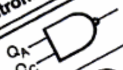
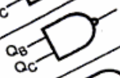
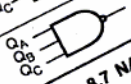
	MOD-5 Co
	MOD-6 Counter
	MOD-7 Counter

Table 8.7 NAND gate inputs for MOD-N counter

Example 8.22 : A *certain counter is being pulsed by a 256 kHz clc frequency from the last flip-flop is 2 kHz :*

i) *Determine the MOD number.*

ii) *Determine the counting range.*

Solution : Clock frequency = 256 kHz

Output frequency = 2 kHz

Mod number = $n = \frac{256}{2} = 128$

∴ Counter is Mod-128 counter

∴ Mod-128 counter can count the numbers from 0 t

8.7 Decade Counters

The binary counter has maximum number o of flip-flops in the counter. Counters can also their sequence that is less than 2^n. In decad states, 0000 (0 in decimal) through 1001 (useful in display applications in which BC

The truncation in the count sequen count instead of going through all of reset back to the 0000 state after the help of reset inputs of each flip- reached. In case of BCD decade 1010 state is reached. This is i diagram for circuit shown in F

Solution : Divide-by-2 for up counting

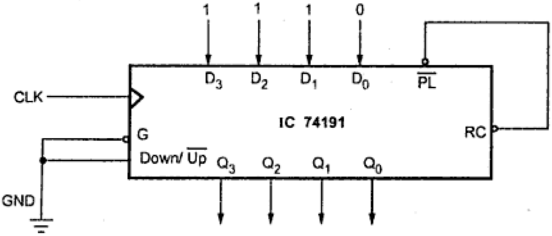

1
1
1
0
D_3
D_2
D_1
D_0
$\overline{PL}$
CLK
IC 74191
G
RC
Down/ $\overline{Up}$
Q_3
Q_2
Q_1
Q_0
GND

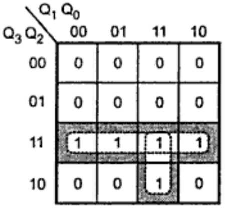
Fig. 8.41

Divide-by-2 is a mod-2 counter. Since, after preset above counter goes through 2 states 1110 and 1111, it is a mod-2 counter. Thus, above circuit is a divide-by-2 counter for up counting mode.

Divide-by-5 for down counting mode :

Q_3	Q_2	Q_1	Q_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Truth table


$Q_1 Q_0$
$Q_3 Q_2$
00
01
11
10
00
01
11
10
0
0
0
0
0
0
0
0
1
1
1
1
0
0
1
0

$Y = Q_3Q_2 + Q_3Q_1Q_0$

Fig. 8.42 K-map simplification

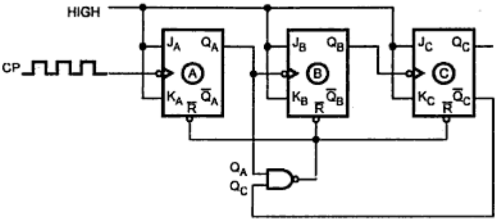

HIGH
CP
J_A
Q_A
K_A
Q̄_A
R̄
A
J_B
Q_B
K_B
Q̄_B
R̄
B
J_C
Q_C
K_C
Q̄_C
R̄
C
Q_A
Q_C

Fig. 8.45 MOD-5 counter using RESET input

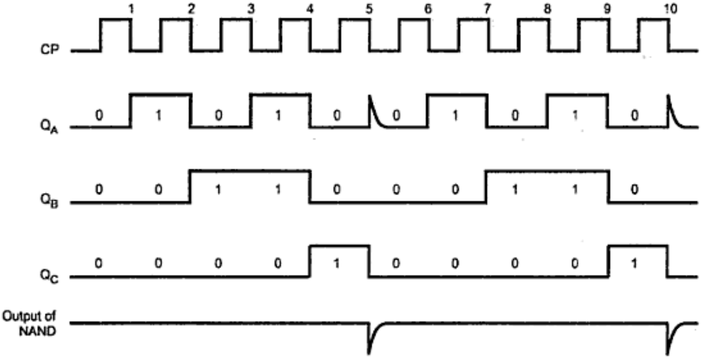
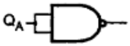
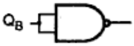
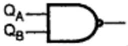
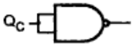


Fig. 8.46 Waveforms for MOD-5 counter

Any desired MOD number can be obtained by changing the NAND gate inputs. The Table 8.7 shows the NAND gate inputs and corresponding MOD-N counter.

NAND Gate Inputs	Counter
	MOD-1 Counter
	MOD-2 Counter
	MOD-3 Counter
	MOD-4 Counter

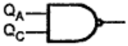
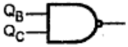
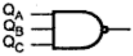
	MOD-5 Counter
	MOD-6 Counter
	MOD-7 Counter

Table 8.7 NAND gate inputs for MOD-N counter

➡ **Example 8.22 :** *A certain counter is being pulsed by a 256 kHz clock signal. The output frequency from the last flip-flop is 2 kHz :*

i) Determine the MOD number.

ii) Determine the counting range.

Solution : Clock frequency = 256 kHz

Output frequency = 2 kHz

$$\therefore \quad \text{Mod number} = n = \frac{256}{2} = 128$$

∴ Counter is Mod-128 counter

Mod-128 counter can count the numbers from 0 to 127.

8.7 Decade Counters

The binary counter has maximum number of states equal to 2^n, where n is the number of flip-flops in the counter. Counters can also be designed to have a number of states in their sequence that is less than 2^n. In decade counters the sequence is truncated upto ten states, 0000 (0 in decimal) through 1001 (9 in decimal). These type of counters are very useful in display applications in which BCD numbers are used.

The truncation in the count sequence is achieved by resetting the counter at particular count instead of going through all of its normal states. In case of BCD decade counter is reset back to the 0000 state after the 1001 state. The resetting of counter is done with the help of reset inputs of each flip-flop. These inputs are activated when desired state is reached. In case of BCD decade counter, reset input is activated using NAND gate when 1010 state is reached. This is illustrated in Fig. 8.47 (a). Fig. 8.47 (b) shows the timing diagram for circuit shown in Fig. 8.47 (a).

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Table 8.8 (c) Reset/Count function table

H : HIGH Level

L : LOW Level

X : Don't Care

Note 1 : Output Q_A is connected to input B for BCD count.

Note 2 : Output Q_D is connected to input A for bi-quinary count.

➠ **Example 8.23 :** *Draw basic internal architecture of IC 7490. Design a divide-by-20 counter using IC 7490.*

Solution : Internal structure of 7490 ripple counter IC is as shown in Fig. 8.50.

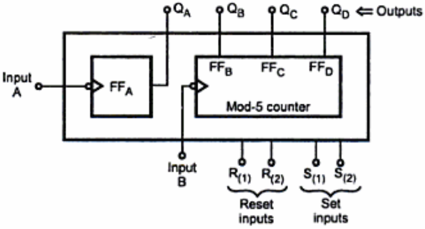


Fig. 8.50 Basic internal structure of IC 7490

We know that, one IC can work as mod-10 (BCD) counter. Therefore we need two ICs. The counter will go through states 0-19 and should be reset on state 20. i.e.

$$\begin{matrix} Q_D \; Q_C \; Q_B \; Q_A \\ \underbrace{0 \quad 0 \quad 1 \quad 0}_{7490\,(2)} \end{matrix} \qquad \begin{matrix} Q_D \; Q_C \; Q_B \; Q_A \\ \underbrace{0 \quad 0 \quad 0 \quad 0}_{7490\,(1)} \end{matrix}$$

The diagram of divide-by-20 counter using IC 7490 is as shown in Fig. 8.51.

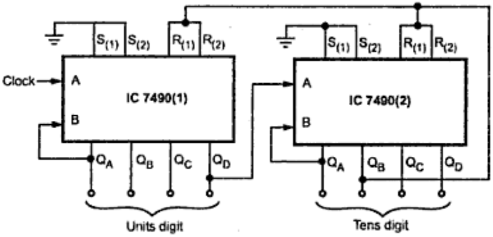

$S_{(1)}$
$S_{(2)}$
$R_{(1)}$
$R_{(2)}$
Clock
A
B
IC 7490(1)
IC 7490(2)
Q_A
Q_B
Q_C
Q_D
Units digit
Tens digit

Fig. 8.51 Divide-by-20 counter using IC 7490

Example 8.24 : *Design a divide-by-96 counter using 7490 ICs.*

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-96 counter, the counter is reset as soon as it becomes 1001 0110. The diagram is shown in Fig. 8.52.

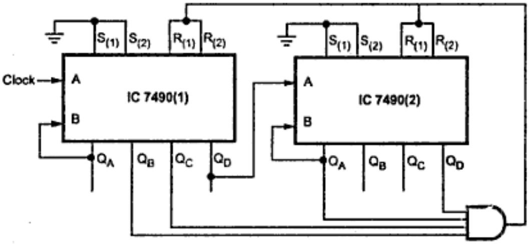

$S_{(1)}$
$S_{(2)}$
$R_{(1)}$
$R_{(2)}$
Clock
A
B
IC 7490(1)
IC 7490(2)
Q_A
Q_B
Q_C
Q_D

Fig. 8.52 Divide-by-96 counter

Example 8.25 : *Design divide-by-93 counter using the same IC.*

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-93 counter, the counter is reset as soon as it becomes 1001 0011. The diagram is shown in the Fig. 8.53.

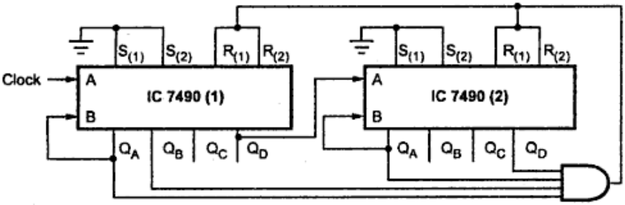

$S_{(1)}$
$S_{(2)}$
$R_{(1)}$
$R_{(2)}$
Clock
A
B
IC 7490 (1)
IC 7490 (2)
Q_A
Q_B
Q_C
Q_D

Fig. 8.53 Divide-by-93 counter

3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Table 8.8 (b) BCD Bi-quinary (5-2) (Note 2)

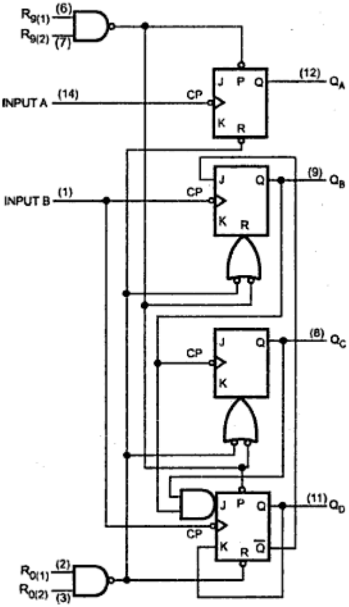

$R_{9(1)}$
(6)
$R_{9(2)}$
(7)
INPUT A
(14)
CP
J
P
Q
K
R
(12)
Q_A
INPUT B
(1)
CP
J
Q
K
R
(9)
Q_B
CP
J
Q
K
(8)
Q_C
J
P
Q
CP
K
R
$\overline{Q}$
(11)
Q_D
$R_{0(1)}$
(2)
$R_{0(2)}$
(3)

Fig. 8.49

$\overline{\text{CLEAR}}$: A LOW level at the $\overline{\text{CLEAR}}$ input sets all four outputs of the flip-flops (Q_A, Q_B, Q_C, Q_D) to LOW levels regardless of the levels at P, T and $\overline{\text{LOAD}}$ inputs.

Ripple carry output :

This output goes high when output of all flip-flops and T input are HIGH. This indicates count overflow. This output remains HIGH for duration approximately equal to the HIGH level output of Q_A.

Timing waveforms :

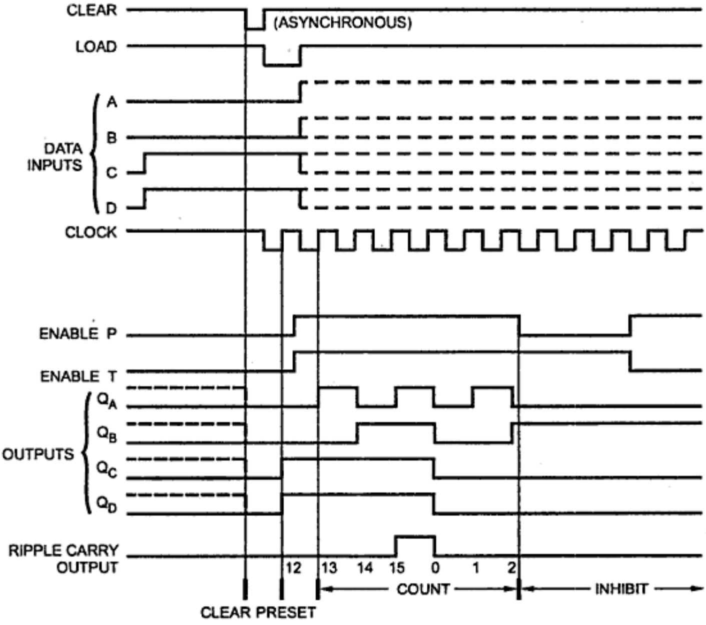

CLEAR
(ASYNCHRONOUS)
LOAD
A
B
C
D
DATA INPUTS
CLOCK
ENABLE P
ENABLE T
Q_A
Q_B
Q_C
Q_D
OUTPUTS
RIPPLE CARRY OUTPUT
12 13 14 15 0 1 2
COUNT
INHIBIT
CLEAR PRESET

Fig. 8.59

➡ **Example 8.30 :** *Sketch the output waveforms of the counter circuit shown in Fig. 8.60. What will be its modulus ?*

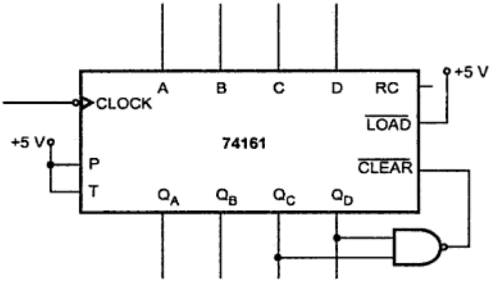

A
B
C
D
RC
CLOCK
+5 V
LOAD
74161
+5 V
P
T
CLEAR
Q_A
Q_B
Q_C
Q_D

Fig. 8.60

Solution :

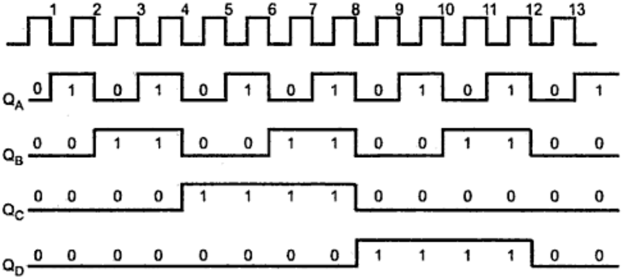


Fig. 8.61

The counter goes through states 0000 (Decimal 0) to 1011 (Decimal 11), i.e., through 12 states. Thus it is a MOD-12 counter.

➡ **Example 8.31 :** *Explain the operation of the circuit shown in Fig. 8.62.*

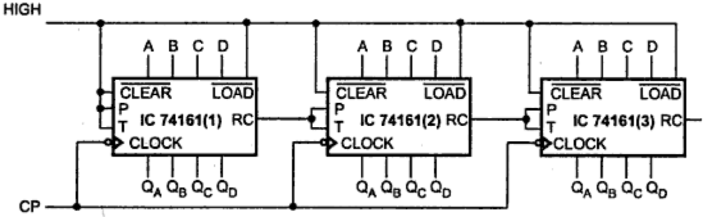

HIGH
A B C D
CLEAR
LOAD
P
T
IC 74161(1)
RC
CLOCK
Q_A Q_B Q_C Q_D
A B C D
CLEAR
LOAD
P
T
IC 74161(2)
RC
CLOCK
Q_A Q_B Q_C Q_D
A B C D
CLEAR
LOAD
P
T
IC 74161(3)
RC
CLOCK
Q_A Q_B Q_C Q_D
CP

Fig. 8.62

Solution : The Fig. 8.63 shows the cascaded connection of 4-bit binary counters. Let us see the circuit operation. The counter IC_1 operates as a counter for counting in the UP direction since CLEAR = LOAD = 1. When the count reaches the maximum value (1111) its RC (Ripple Carry Output) goes HIGH which makes P and T (Enable) inputs of IC_2 HIGH for one clock cycle advancing its output by 1 and making Q outputs of IC_1, 0 at the

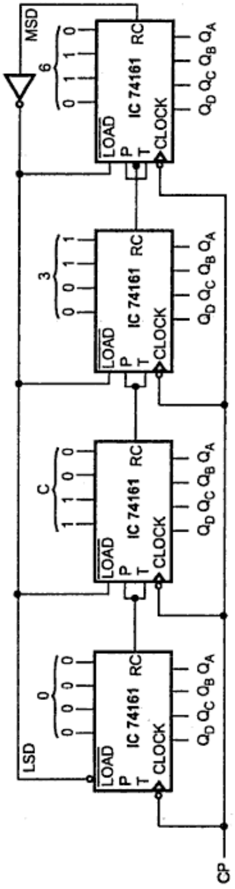

MSD
6
0
1
1
0
LOAD
P
T
CLOCK
IC 74161
RC
Q_D Q_C Q_B Q_A
3
1
1
0
0
LOAD
P
T
CLOCK
IC 74161
RC
Q_D Q_C Q_B Q_A
C
0
0
1
1
LOAD
P
T
CLOCK
IC 74161
RC
Q_D Q_C Q_B Q_A
0
0
0
0
0
LSD
LOAD
P
T
CLOCK
IC 74161
RC
Q_D Q_C Q_B Q_A
CP

Fig. 8.63 Divide-by-40,000 counter using 74161, four bit binary counter

next clock cycle. After this clock cycle P = T = 0 for IC_2 and IC_1 will go on counting the pulses. When the outputs of IC_1 and IC_2 both reach the maximum count, RC outputs of both of these ICs will go HIGH. This will make P = T of IC_3 HIGH and therefore, in the next clock cycle IC_3 count will be incremented and simultaneously IC_1 and IC_2 will be cleared. This way the counting will continue.

➠ **Example 8.32 :** *Design the divide-by-40,000 (modulus 40,000) counter using four 74161 ICs.*

Solution : Cascading four 74161 (each 4-bit) counters we get 16 (4 × 4) bit counter as shown in the Fig. 8.63.

Therefore, we get 2^{16} = 65,536 modulus counter

However, we require divide-by-40,000 counter. The difference between 65,536 and 40,000 is 25,536, which is the number of states those must be skipped from the full modulus sequence. This can be achieved by presetting the counter to value 25,536 (63 CO in hexadecimal). Each time when counter recycles it starts counting from 25,536 upto 65,536 on each full cycle. Therefore, each full cycle of the counter consists of 40,000 states.

8.8.2 4-bit Synchronous Binary Counter (IC 74163)

The IC 74X163 is a synchronous 4-bit binary counter with active-low load and clear inputs. The Fig. 8.64 shows the logic symbol of 74X163 and Table 8.10 summarizes the function using state table. The Fig. 8.64 shows the internal logic diagram of IC 74X163.

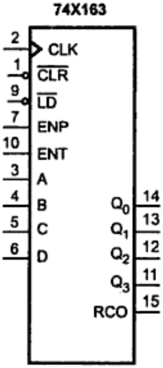


Fig. 8.64 Logic symbol for the IC 74X163

Inputs				Current State				Next State			
$\overline{CLR}$	$\overline{LD}$	ENT	ENP	Q_3	Q_2	Q_1	Q_0	Q_3*	Q_2*	Q_1*	Q_0*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	Q_3	Q_2	Q_1	Q_0
1	1	x	0	x	x	x	x	Q_3	Q_2	Q_1	Q_0
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

Table 8.10 State table for a 74X163 4-bit binary counter

The 74X163 uses D flip-flops to perform load and clear functions. Each D input is driven by a 2-input multiplexer form by the combination of an OR gate and two AND gates. The multiplexer output is 0 if the $\overline{CLR}$ input is asserted. Otherwise, the top AND gate passes the data input (A, B, C or D) to the output if $\overline{LD}$ is asserted. If neither $\overline{CLR}$ nor $\overline{LD}$ is asserted, the bottom AND gate passes the output of an XNOR gate to the multiplexer output.

One input of XNOR gate corresponds of one count bit either Q_A, Q_B, Q_C or Q_D. The XNOR gate gives complement output if and only if both enable ENP and ENT are asserted and all of the lower-order count bits are 1. The ripple carry out (RCO) bit is 1 if all of the count bits are 1 and ENT is asserted. The RCO signal indicates a carry from the most significant bit position.

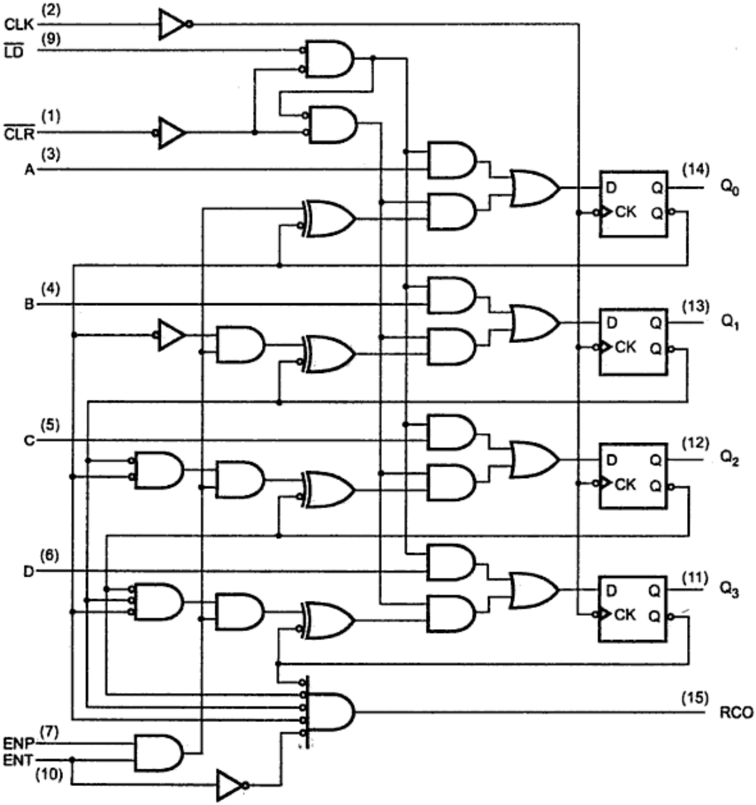

CLK (2)
LD (9)
CLR (1)
A (3)
B (4)
C (5)
D (6)
ENP (7)
ENT (10)
D
CK
Q
(14) Q_0
(13) Q_1
(12) Q_2
(11) Q_3
(15) RCO

Fig. 8.65 Logic diagram for the 74X163 synchronous 4-bit binary counter

Connecting 74X163 in Free-Running Mode

The Fig. 8.66 shows the circuit diagram of 74X163 operating in free-running mode. In this mode, enable inputs are enabled continuously. The Fig. 8.67 shows the resulting output waveform in free-running mode. Looking at the waveforms, we can observe that each signal has half the frequency of the preceding one. Thus, a free-running 74X163 can be used as a divide-by-2, divide-by-4, divide-by-8 or divide by 16 counter.

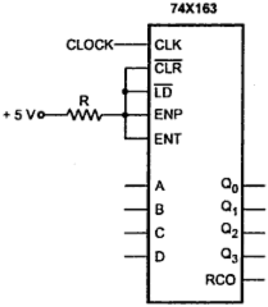


Fig. 8.66 Circuit connection for the 74X163 to operate in a free-running mode

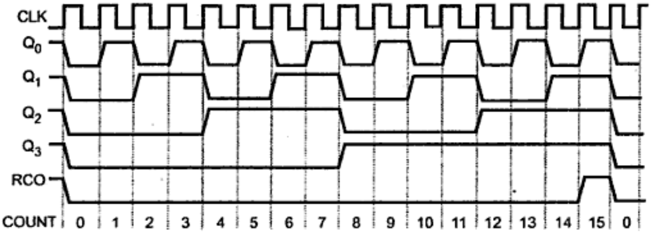


Fig. 8.67 Timing waveform in free-running mode

For 74X163, the clear function is synchronous. A low level at the $\overline{CLR}$ input sets all four outputs of flip-flops (Q_0 - Q_3) to low levels after the next positive-going transition on the clock (CLK) input.

Counter ICs : 74X160, 74X161 and 74X162

The counter 74X160, 74X161, 74X162 and 74X163 have the same pinouts. However, they have some differences in the operation. These are as follows.

- Counters 74X160 and 74162 are the decade counters.
- Counters 74X160 and 74X161 provides asynchronous clear function where as counters 74X162 and 74X163 provides synchronous clear function.

When IC 74X160 and 74X162 are connected in free running mode they count from 0 to 9. The Fig. 8.68 shows the timing waveform for free running divide-by-10 counter using 74X160 and 74X162.

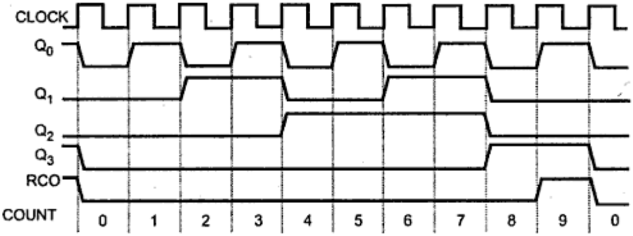


Fig. 8.68 Timing waveforms for divide-by-10 counter

➠ **Example 8.33 :** *Design the modulo-11 counter using 74X163.*

Solution : Although the 74X163 is a modulo-16 counter, it can be made to count in a modulus less than 16 by using the $\overline{CLR}$ or $\overline{LD}$ input to shorten the normal counting sequence. The Fig. 8.69 shows circuit connections for modulo-11 counter. Here, load input is activated upon activation of RCO (ripple-carry-output). Since load input is adjusted to state 5, counter counts from 5 to 15 and then starts at 5 again, for a total of 11 states per counting cycle.

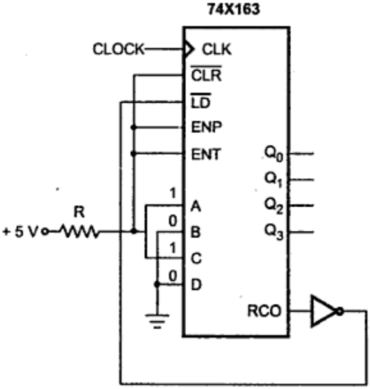


Fig. 8.69 Modulo-11 counter using $\overline{LD}$ input

We can also design modulo-11 counter using $\overline{CLR}$ input as shown in the Fig. 8.70 Here, NAND gate is used to detect state 10 and force the next state to 0. A 2-input gate is used to detect state 10 (binary 1010) by connecting Q_1 and Q_3 to the inputs of the NAND gate.

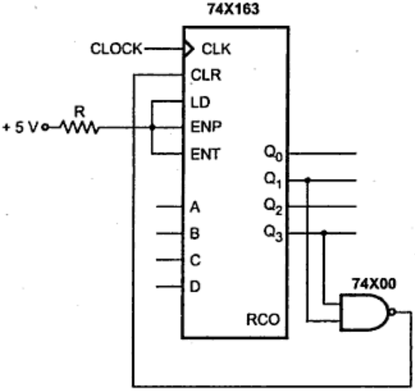

74X163
CLOCK
CLK
CLR
LD
ENP
ENT
R
+ 5 V
A
B
C
D
Q_0
Q_1
Q_2
Q_3
RCO
74X00

Fig. 8.70 Modulo-11 counter using $\overline{CLR}$ input

Example 8.34 : *Design an excess-3 decimal counter using 74X163.*

Solution : An excess-3 decimal counter should start counting from count 3 (binary 0011) and count upto count 12 (binary 1100). Starting count is adjusted by loading 0011 at load inputs. To recycle count from 1100 to 0011, Q_3 and Q_2 output are connected as inputs for 2-input NAND gate. Thus, NAND gate detects state 1100 and forces 0011 to be loaded as the next state. The Fig. 8.72 shows resulting timing waveform.

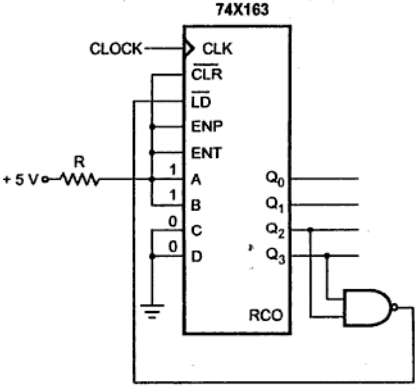

74X163
CLOCK
CLK
$\overline{CLR}$
$\overline{LD}$
ENP
ENT
R
+ 5 V
1
1
0
0
A
B
C
D
Q_0
Q_1
Q_2
Q_3
RCO

Fig. 8.71 Excess-3 decimal counter using 74X163

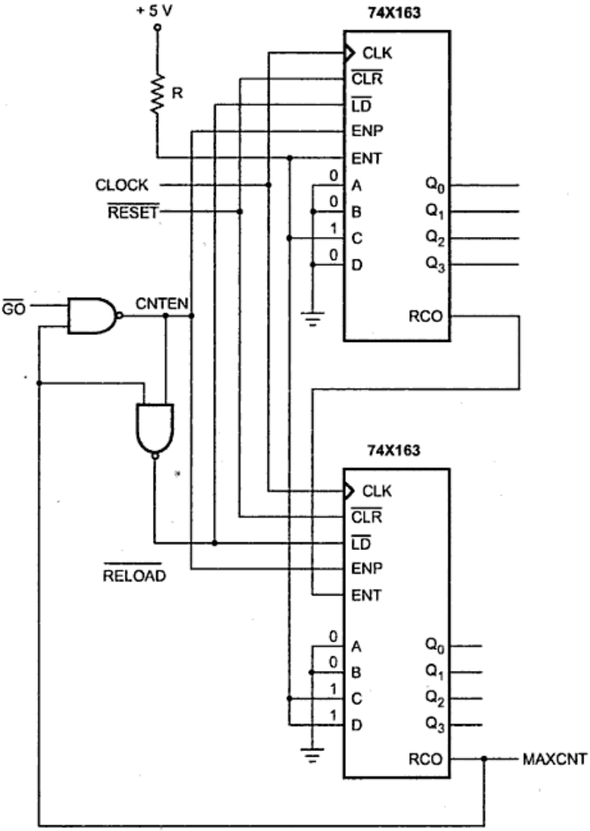

+5 V
R
74X163
CLK
$\overline{CLR}$
$\overline{LD}$
ENP
ENT
CLOCK
$\overline{RESET}$
0
A
0
B
1
C
0
D
Q_0
Q_1
Q_2
Q_3
$\overline{GO}$
CNTEN
RCO
74X163
CLK
$\overline{CLR}$
$\overline{LD}$
ENP
ENT
$\overline{RELOAD}$
0
A
0
B
1
C
1
D
Q_0
Q_1
Q_2
Q_3
RCO
MAXCNT

Fig. 8.73 Modulo-60 counter using two 74X163s

8.8.3 4-bit Bi-directional Synchronous Counter (IC 74169)

IC 74X169 is another 4-bit bi-directional synchronous counter. The Fig. 8.75 shows the logic symbol of 74X169. In 74X169, carry output and enable inputs are active low. Its UP/$\overline{DN}$ input enables to count either up or down. When UP/$\overline{DN}$ input is logic 1, counter count upwards; otherwise it count downwards.

8.9 Counter Design as a Synthesis Problem

Let us see the steps involved in design of synchronous counters.

1. Obtain the transition table from the given circuit information.
2. Determine the number of flip-flops needed.
3. Choose the type of flip-flops to be used.
4. From the transition table, derive the circuit excitation table.
5. Use K-map or any other simplification method to derive the circuit the flip-flop input functions.
6. Draw the logic diagram.

Note : The design procedure of sequential circuit involves few additional steps such as state reduction and state assignment. For simplicity these steps are deliberately not considered here.

8.9.1 Design of a Synchronous Mod-6 Counter using Clocked JK Flip-Flops

The counter with n flip-flops has maximum mod number 2^n. For example, 3-bit binary counter is a mod 8 counter. This basic counter can be modified to produce MOD numbers less than 2^n by allowing the counter to skip states those are normally part of counting sequence. Let us design mod-6 counter using clocked JK flip-flops.

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$.

Here $N = 6 \quad \therefore n = 3$

i.e. Three flip-flops are required.

Step 2 : Write an excitation table for JK flip-flop.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 8.11

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

Step 4 : K-map simplification for flip-flop inputs.

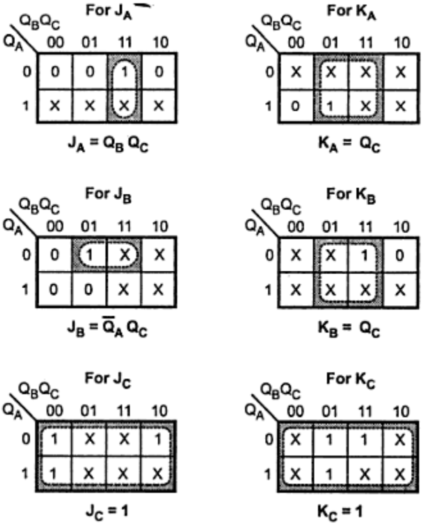

For J_A
Q_BQ_C
Q_A
00 01 11 10
0: 0 0 1 0
1: X X X X
$J_A = Q_B Q_C$
For K_A
Q_BQ_C
Q_A
00 01 11 10
0: X X X X
1: 0 1 X X
$K_A = Q_C$
For J_B
Q_BQ_C
Q_A
00 01 11 10
0: 0 1 X X
1: 0 0 X X
$J_B = \overline{Q}_A Q_C$
For K_B
Q_BQ_C
Q_A
00 01 11 10
0: X X 1 0
1: X X X X
$K_B = Q_C$
For J_C
Q_BQ_C
Q_A
00 01 11 10
0: 1 X X 1
1: 1 X X X
$J_C = 1$
For K_C
Q_BQ_C
Q_A
00 01 11 10
0: X 1 1 X
1: X 1 X X
$K_C = 1$

Fig. 8.77

Step 5 : Implement the counter.

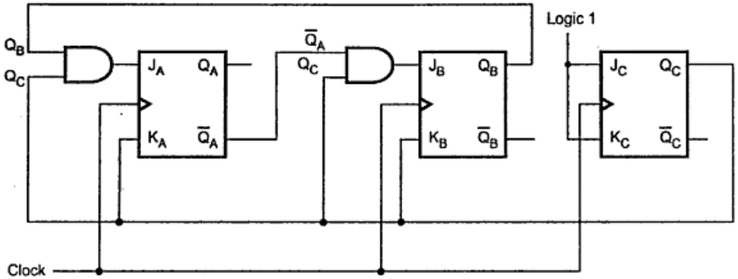

Logic 1
Q_B
Q_C
J_A
Q_A
K_A
$\overline{Q}_A$
$\overline{Q}_A$
Q_C
J_B
Q_B
K_B
$\overline{Q}_B$
J_C
Q_C
K_C
$\overline{Q}_C$
Clock

Fig. 8.78 Implementation of MOD-6 synchronous counter

Note : To avoid crossing of lines and to have better clarity the circuit can also be represented as shown in Fig. 8.79. Here, instead of actual connections only signal names are specified.

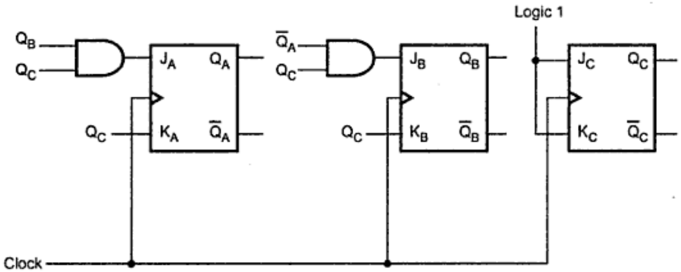

Logic 1
Q_B
Q_C
J_A
Q_A
Q_C
K_A
$\overline{Q}_A$
$\overline{Q}_A$
Q_C
J_B
Q_B
Q_C
K_B
$\overline{Q}_B$
J_C
Q_C
K_C
$\overline{Q}_C$
Clock

Fig. 8.79 Simplified representation of Fig. 8.78

8.9.2 Design of a Synchronous Mod-6 Counter using Clocked D Flip-Flop

Designing with clocked D flip-flop is slightly simpler process than designing with any other flip-flop. Since Q output of D flip-flop follows D input, next state and flip-flop input columns are same and it is not necessary to refer excitation table and determine the flip-flop inputs column in the transition table.

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$

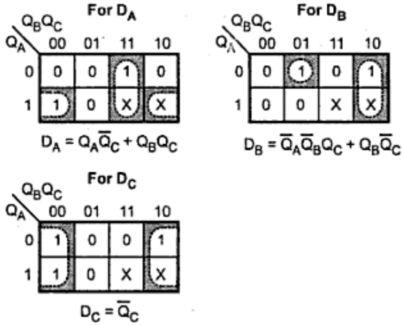
Here $N = 6 \quad \therefore \quad n = 3$

i.e. Three flip-flops are required.

Step 2 : Determine the transition table.

Present state			Next state		
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	x	x	x
1	1	1	x	x	x

Step 3 : K-map simplification for flip-flop inputs.


For D_A
Q_BQ_C
Q_A
00
01
11
10
0
1
0
0
1
0
1
0
X
X
For D_B
Q_BQ_C
Q_A
00
01
11
10
0
1
0
1
0
1
0
0
X
X
For D_C
Q_BQ_C
Q_A
00
01
11
10
0
1
1
0
0
1
1
0
X
X

$D_A = Q_A\overline{Q}_C + Q_BQ_C$

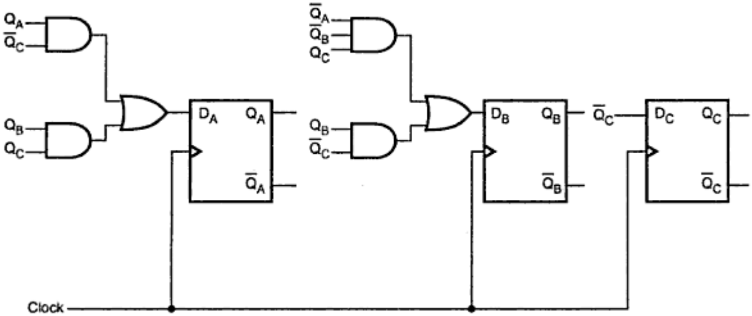
$D_B = \overline{Q}_A\overline{Q}_BQ_C + Q_B\overline{Q}_C$

$D_C = \overline{Q}_C$

Fig. 8.80

Step 4 : Implement the counter.

Note : Eventhough the procedure of implementing counters using D flip-flops is simpler, it requires more circuitry to determine flip-flop inputs.



Q_A
$\bar{Q}_C$
Q_B
Q_C
D_A
Q_A
$\bar{Q}_A$
$\bar{Q}_A$
$\bar{Q}_B$
Q_C
Q_B
$\bar{Q}_C$
D_B
Q_B
$\bar{Q}_B$
$\bar{Q}_C$
D_C
Q_C
$\bar{Q}_C$
Clock

Fig. 8.81

8.9.3 Design of a Synchronous Mod-6 Counter using Clocked T Flip-Flop

For designing of counter using clocked T flip-flop we have to follow a similar procedure as that for the design using clocked JK flip-flop.

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$

Here $N = 6 \quad \therefore \quad n = 3$

i.e. Three flip-flops are required.

Step 2 : Write an excitation table for T flip-flop.

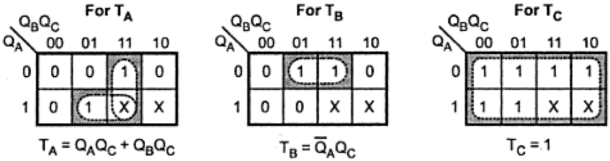
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs		
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1

0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

Step 4 : K-map simplification for flip-flop inputs.


For T_A
Q_BQ_C
Q_A
00 01 11 10
0 | 0 0 1 0
1 | 0 1 X X
For T_B
Q_BQ_C
Q_A
00 01 11 10
0 | 0 1 1 0
1 | 0 0 X X
For T_C
Q_BQ_C
Q_A
00 01 11 10
0 | 1 1 1 1
1 | 1 1 X X

$T_A = Q_AQ_C + Q_BQ_C$

$T_B = \overline{Q}_AQ_C$

$T_C = 1$

Fig. 8.82

Step 5 : Implement the counter.

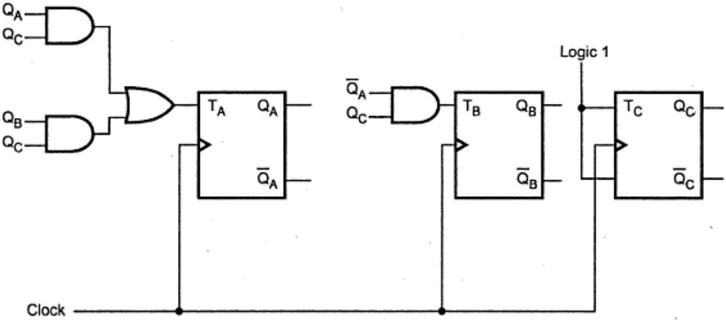

Q_A
Q_C
Q_B
Q_C
T_A
Q_A
$\overline{Q}_A$
$\overline{Q}_A$
Q_C
T_B
Q_B
$\overline{Q}_B$
Logic 1
T_C
Q_C
$\overline{Q}_C$
Clock

Fig. 8.83

8.9.4 Design of a Synchronous Mod-6 Counter using Clocked SR Flip-Flop

For designing of counter using clocked SR flip-flop we have to follow a similar procedure as that for the design using clocked JK and T flip-flops.

Step 1 : Find number of Flip-Flops required to build the counter.

Flip-flops required are : $2^n \geq N$

Here $N = 6 \quad \therefore n = 3$

i.e. Three flip-flops are required

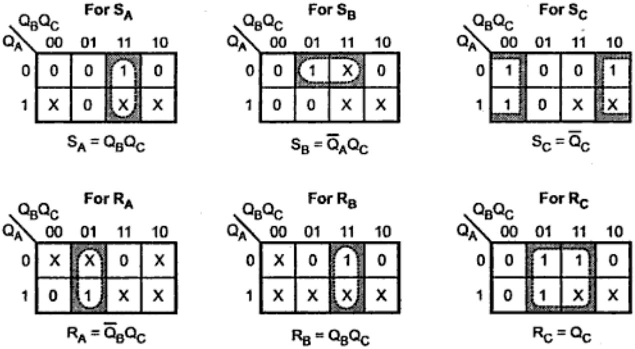
Step 2 : Write an excitation table for SR flip-flop.

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	S_A	R_A	S_B	R_B	S_C	R_C
0	0	0	0	0	1	0	x	0	x	1	0
0	0	1	0	1	0	0	x	1	0	0	1
0	1	0	0	1	1	0	x	x	0	1	0
0	1	1	1	0	0	1	0	0	1	0	1
1	0	0	1	0	1	x	0	0	x	1	0
1	0	1	0	0	0	0	1	0	x	0	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

Step 4 : K-map simplification for flip-flops.


For S_A
For S_B
For S_C
For R_A
For R_B
For R_C
Q_BQ_C
Q_A
00 01 11 10
0
1
0 0 1 0
X 0 X X
0 1 X 0
0 0 X X
1 0 0 1
1 0 X X
X X 0 X
0 1 X X
X 0 1 0
X X X X
0 1 1 0
0 1 X X

$S_A = Q_BQ_C$ $S_B = \overline{Q}_AQ_C$ $S_C = \overline{Q}_C$

$R_A = \overline{Q}_BQ_C$ $R_B = Q_BQ_C$ $R_C = Q_C$

Fig. 8.84

Step 5 : Implement the counter

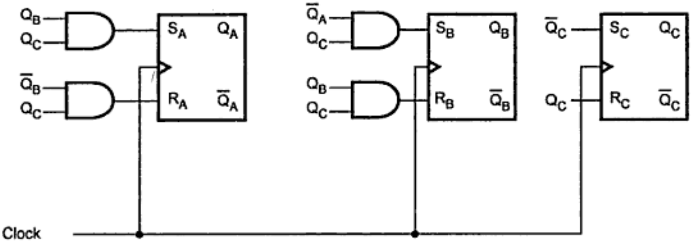


Fig. 8.85

8.9.5 Design of Synchronous Decade Counter

We know that in the decade counters we have to truncate normal counter sequence. Therefore, it is also called MOD-10 counter. Let us design the synchronous decade counter. Here, we will not use clear input to reset the counter after state 1010. Table 8.12 shows the excitation table for synchronous decade counter using T flip-flops.

Excitation table

Present State				Next State				Flip-flop Inputs			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

Table 8.12

K-map simplification

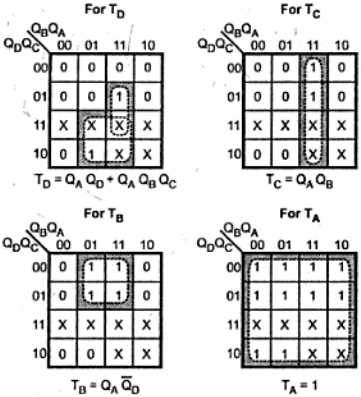

For T_D
Q_BQ_A
Q_DQ_C
00 01 11 10
$T_D = Q_A Q_D + Q_A Q_B Q_C$
For T_C
$T_C = Q_A Q_B$
For T_B
$T_B = Q_A \overline{Q}_D$
For T_A
$T_A = 1$

Fig. 8.86

Logic Diagram

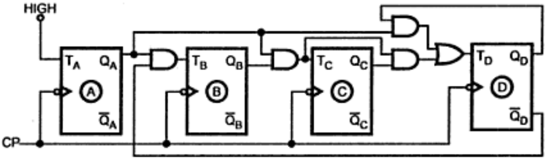

HIGH
CP
T_A Q_A A $\overline{Q}_A$
T_B Q_B B $\overline{Q}_B$
T_C Q_C C $\overline{Q}_C$
T_D Q_D D $\overline{Q}_D$

Fig. 8.87

Fig. 8.88 shows the timing diagram for the synchronous decade counter.

Timing diagram

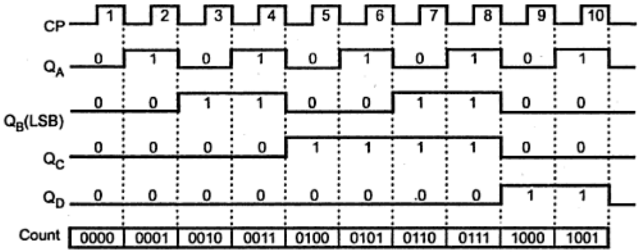


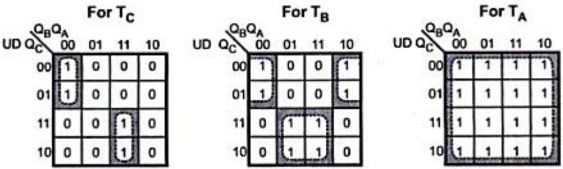
Fig. 8.88

Excitation table

Input	Present State			Next State			Flip-flop Inputs		
UP/$\overline{\text{DOWN}}$ (UD)	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

Table 8.14

K-map simplification


For T_C
Q_BQ_A
UD Q_C
00 01 11 10
00 1 0 0 0
01 1 0 0 0
11 0 0 1 0
10 0 0 1 0
For T_B
Q_BQ_A
UD Q_C
00 01 11 10
00 1 0 0 1
01 1 0 0 1
11 0 1 1 0
10 0 1 1 0
For T_A
Q_BQ_A
UD Q_C
00 01 11 10
00 1 1 1 1
01 1 1 1 1
11 1 1 1 1
10 1 1 1 1

$T_C = \overline{UD}\,\overline{Q}_B\,\overline{Q}_A + UD\,Q_B\,Q_A$

$T_B = \overline{UD}\,\overline{Q}_A + UD\,Q_A$

$T_A = 1$

Fig. 8.89

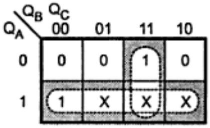
Example 8.39 : *Design mod-5 synchronous counter using T flip-flop.*

Solution : For mod-5 counter we require 3 flip-flops.

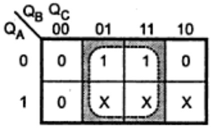
Excitation table

	Present state			Next state			Flip-flops inputs		
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	0	0	0	1	0	0

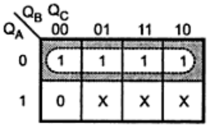
K-map simplification


QB QC
QA
00
01
11
10
0
1
0 0 1 0
1 X X X

$T_A = Q_A + Q_BQ_C$


QB QC
QA
00
01
11
10
0
1
0 1 1 0
0 X X X

$T_B = Q_C$


QB QC
QA
00
01
11
10
0
1
1 1 1 1
0 X X X

$T_C = \overline{Q}_A$

Logic Diagram

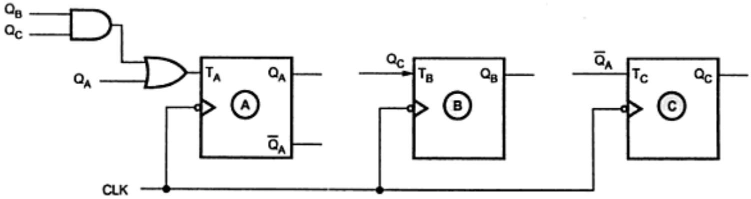

QB
QC
QA
TA
QA
A
Q̄A
QC
TB
QB
B
Q̄A
TC
QC
C
CLK

Fig. 8.92

Example 8.40 : *Design MOD-4 down counter using JK flip-flop.*

Solution : The excitation table for mod-4 down counter is as shown in Table 8.15.

Present state		Next state		Flip-flop inputs			
A	B	A+	B+	J_A	K_A	J_B	K_B
0	0	1	1	1	×	1	×
0	1	0	0	0	×	×	1
1	0	0	1	×	1	1	×
1	1	1	0	×	0	×	1

Table 8.15 Excitation table

K-map simplification

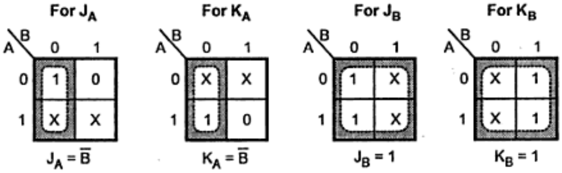

For J_A
For K_A
For J_B
For K_B
A B 0 1
$J_A = \overline{B}$
$K_A = \overline{B}$
$J_B = 1$
$K_B = 1$

Fig. 8.93

Logic Diagram

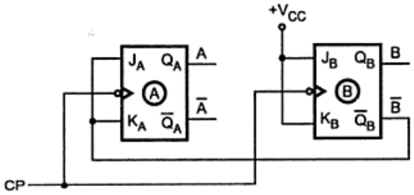

+V_{CC}
J_A Q_A
K_A $\overline{Q}_A$
A
$\overline{A}$
J_B Q_B
K_B $\overline{Q}_B$
B
$\overline{B}$
CP

Fig. 8.94

Example 8.41 : *Design a MOD-12 synchronous counter using D flip-flop.*

Solution : Mod-12 synchronous counter using D flip-flop :

Let Number of flip-flop required = n

$$2^n \geq 12$$

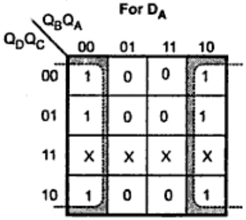
$$n = 4$$

Excitation table

Present state				Next state			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	0

K-map simplification

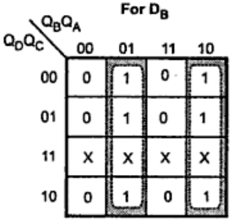
For D_A



Q_DQ_C \ Q_BQ_A	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	0	1

$D_A = \overline{Q}_A$

For D_B

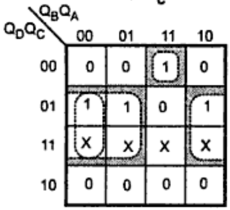


Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	1	0	1

$D_B = \overline{Q}_B Q_A + \overline{Q}_A Q_B$

$= Q_A \oplus Q_B$

For D_C

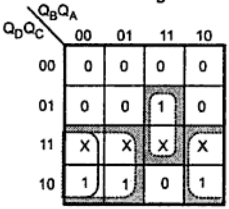


Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	0	0

$D_C = Q_C \overline{Q}_B + Q_C \overline{Q}_A$

$+ \overline{Q}_D \overline{Q}_C Q_B Q_A$

For D_D



Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	1	0	1

$D_D = Q_D \overline{Q}_B + Q_C Q_B Q_A$

$+ Q_D \overline{Q}_A$

Logic Diagram

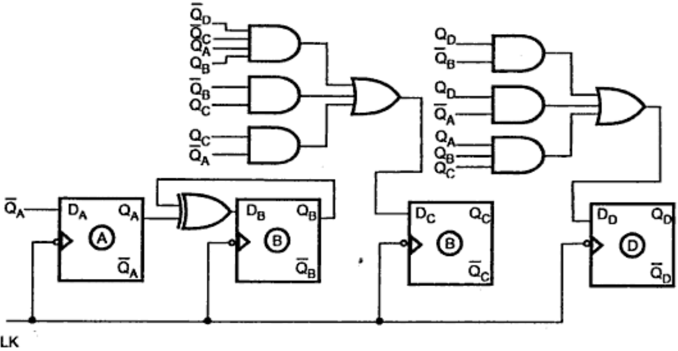

Q̄D
Q̄C
Q̄A
QB
Q̄B
Q̄C
QC
Q̄A
QD
Q̄B
QD
Q̄A
QA
QB
QC
Q̄A
DA
QA
A
Q̄A
DB
QB
B
Q̄B
DC
QC
B
Q̄C
DD
QD
D
Q̄D
CLK

Fig. 8.95

8.11 Ring Counter

Fig. 8.96 shows the logic diagram for four-bit ring counter. As shown in the Fig. 8.96, the Q output of each stage is connected to the D input of the next stage and the output of last stage is fed back to the input of first stage. The $\overline{CLR}$ followed by $\overline{PRE}$ makes the output of first stage to '1' and remaining outputs are zero, i.e. Q_A is one and Q_B, Q_C, Q_D are zero.

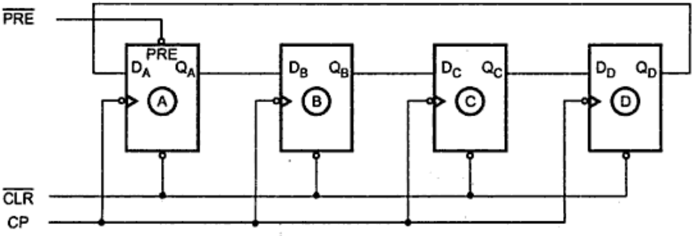

PRE
PRE
DA
QA
A
DB
QB
B
DC
QC
C
DD
QD
D
CLR
CP

Fig. 8.96 Four-bit ring counter

The first clock pulse produces $Q_B = 1$ and remaining outputs are zero. According to the clock pulses applied at the clock input CP, a sequence of four states is produced. These states are listed in Table. 8.16.

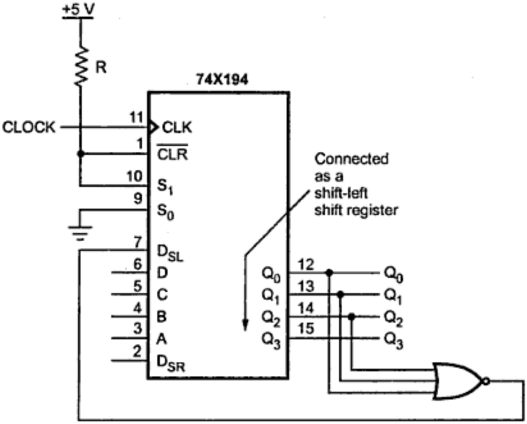

+5 V
R
74X194
CLOCK
11
CLK
1
CLR
10
S_1
9
S_0
7
D_{SL}
6
D
5
C
4
B
3
A
2
D_{SR}
Q_0
Q_1
Q_2
Q_3
12
13
14
15
Connected as a shift-left shift register
Q_0
Q_1
Q_2
Q_3

Fig. 8.98 (a) 4-bit Self correcting ring counter

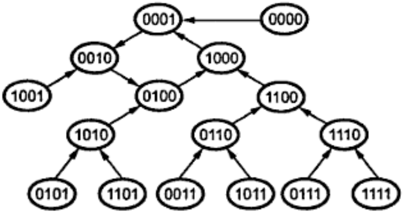

0001
0000
0010
1000
1001
0100
1100
1010
0110
1110
0101
1101
0011
1011
0111
1111

Fig. 8.98 (b) State diagram for self correcting ring counter

The ring counter shown above has a single circulating 1. The ring counter with a single circulating 0 can be designed using NAND gate instead of NOR gate in Fig. 8.98 (a).

➠ **Example 8.42 :** *Design a 4-bit, 4-state ring counter using 74X194.*

Solution : The Fig. 8.99 (a) shows the circuit diagram for a 4-bit, 4-state ring counter with a single circulating 1. Here, 74X194 universal shift register is connected so that it normally performs a left-shift. However, when RESET is asserted it loads 0001. Once RESET is negated, the 74194 shifts left on each clock pulse. The D_{SL} serial input is

Example 8.43 : *Assume that 1011 input data pattern is loaded into a 4-bit ring counter. Sketch the resulting flip-flop Q output waveforms (Assume positive edge triggering).*

Solution :

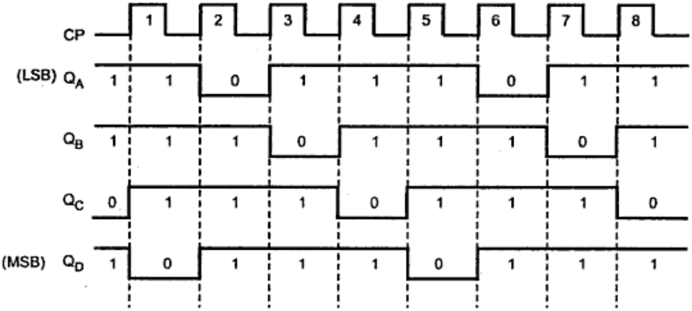


Fig. 8.100

8.12 Johnson or Twisting Ring or Switch Tail Counter

In a Johnson counter, the Q output of each stage of flip-flop is connected to the D input of the next stage. The single exception is that the complement output of the last flip-flop is connected back to the D-input of the first flip-flop as shown in Fig. 8.101.

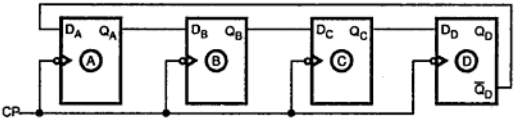


Fig. 8.101 Four-bit Johnson counter

Note : Johnson counter can be implemented with SR or JK flip-flops as well.

As shown in Fig. 8.101, there is a feedback from the rightmost flip-flop complement output to the leftmost flip-flop input. This arrangement produces a unique sequence of states.

Initially, the register (all flip-flops) is cleared. So all the outputs, Q_A, Q_B, Q_C, Q_D are zero. The output of last stage, Q_D is zero. Therefore complement output of last stage, $\overline{Q}_D$ is one. This is connected back to the D input of first stage. So D_A is one. The first falling clock edge produces Q_A=1 and Q_B = 0,Q_C = 0, Q_D = 0 since D_B, D_C, D_D are zero. The next clock pulse produces Q_A=1 ,Q_B =1, Q_C = 0, Q_D = 0. The sequence of states is summarized in Table 8.17. After 8 states the same sequence is repeated.

Clock pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table 8.17 Four-bit Johnson sequence

In this case, four-bit register is used. So the four-bit sequence has a total of eight states. Fig. 8.102 gives the timing sequence for a four-bit Johnson counter.

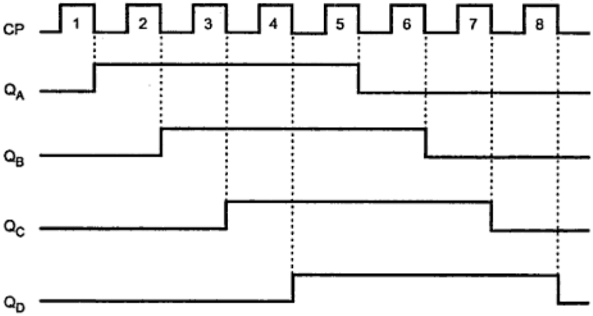


Fig. 8.102 Timing sequence for a four-bit Johnson counter

If we design a counter of five-bit sequence, it has a total of ten states, as shown in Table 8.18.

Clock pulse	Q_A	Q_B	Q_C	Q_D	Q_E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Table 8.18 Five-bit Johnson sequence

So in general we can say that, an n-stage Johnson counter will produce a modulus of $2 \times n$, where n is the number of stages (i.e. flip-flops) in the counter. As shown in tables, the counter will 'fill up' with 1s from left to right and then it will 'fill up' with 0s again.

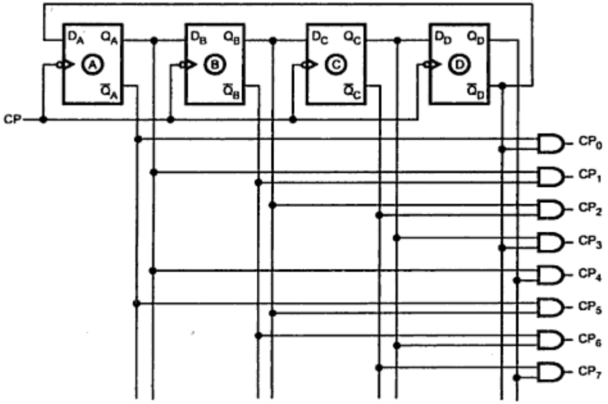

D_A
Q_A
A
$\bar{Q}_A$
D_B
Q_B
B
$\bar{Q}_B$
D_C
Q_C
C
$\bar{Q}_C$
D_D
Q_D
D
$\bar{Q}_D$
CP
CP_0
CP_1
CP_2
CP_3
CP_4
CP_5
CP_6
CP_7

Fig. 8.103 Johnson counter with decoder

One advantage of this type of sequence is that it is readily decoded with two input AND gates. Table 8.19 gives the count sequence and required decoding.

Clock pulse	Q_A	Q_B	Q_C	Q_D	AND Gate required for output
0	0	0	0	0	$\overline{Q}_A \overline{Q}_D$
1	1	0	0	0	$Q_A \overline{Q}_B$
2	1	1	0	0	$Q_B \overline{Q}_C$
3	1	1	1	0	$Q_C \overline{Q}_D$
4	1	1	1	1	$Q_A Q_D$
5	0	1	1	1	$\overline{Q}_A Q_B$
6	0	0	1	1	$\overline{Q}_B Q_C$
7	0	0	0	1	$\overline{Q}_C Q_D$

Table 8.19 Count sequence and required decoding

➠ **Example 8.44 :** *Design a 4-bit, 8-state Johnson counter using IC 74X194. Show how same counter can be modified as self correcting Johnson counter.*

Solution : Johnson counter is basically a twisted ring counter. The Fig. 8.104 (a) shows the basic circuit for a Johnson counter and Fig. 8.104 (b) shows its timing diagram. The Table 8.20 shows the states of a 4-bit Johnson counter.

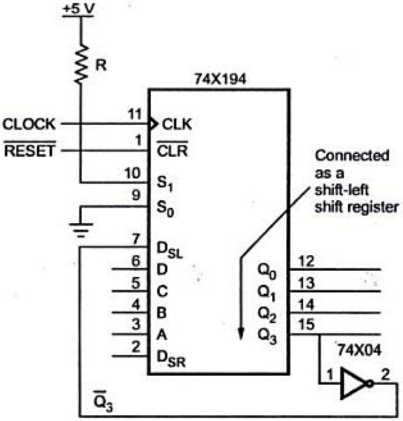

+5 V
R
74X194
CLOCK
RESET
11
CLK
1
CLR
10
S1
9
S0
7
DSL
6
D
5
C
4
B
3
A
2
DSR
Connected as a shift-left shift register
Q0
Q1
Q2
Q3
12
13
14
15
74X04
1
2
Q̄3

Fig. 8.104 (a) 4-bit Johnson counter

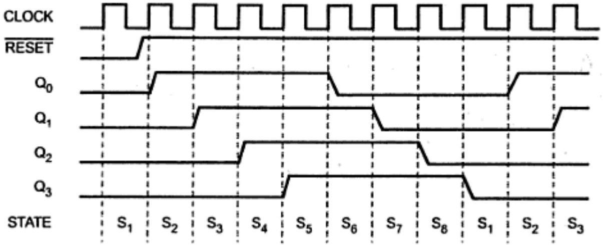


Fig. 8.104 (b) Timing diagram for a 4-bit Johnson counter

State name	Q_3	Q_2	Q_1	Q_0
S_1	0	0	0	0
S_2	0	0	0	1
S_3	0	0	1	1
S_4	0	1	1	1
S_5	1	1	1	1
S_6	1	1	1	0
S_7	1	1	0	0
S_8	1	0	0	0

Table 8.20 States of a 4-bit Johnson counter

This counter can be modified to have self correcting Johnson counter as shown in the Fig. 8.104 (c). Here, the connections are made such that circuit loads 0001 as the next state whenever the current state is 0XX0.

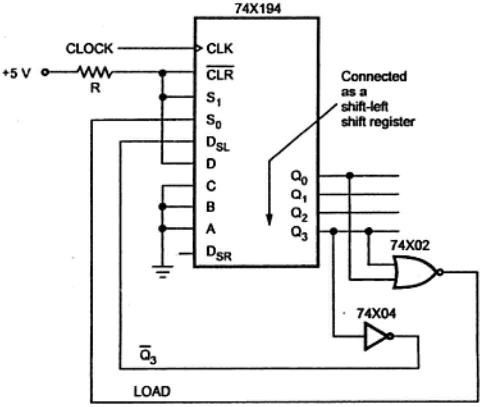

74X194
CLOCK
+5 V
R
CLK
CLR
S_1
S_0
D_{SL}
D
C
B
A
D_{SR}
Connected as a shift-left shift register
Q_0
Q_1
Q_2
Q_3
74X02
74X04
$\overline{Q}_3$
LOAD

Fig. 8.104 (c) Self correcting 4-bit, 8-state Johnson counter

Example 8.45 : *How many flip-flops are required to implement each of following in a Johnson counter configuration :*

i) Mod 10

ii) Mod 16

Solution : Johnson counter will produce a modulus of $2 \times n$ where n is the number of stages (i.e. flip-flops) in the counter. Therefore, Mod 10 requires 5 flip-flops and Mod 16 requires 8 flip-flops.

Review Questions

1. *Explain the working of 4-bit asynchronous counter.*
2. *What is the primary disadvantage of an asynchronous counter?*
3. *A four-bit asynchronous counter consists of flip-flops each of which has a clock to Q propagation delay of 12 ns. How long does it take the counter to recycle from 1111 to 0000 after the triggering edge of the clock pulse?*
4. *Design the following ripple counters using JK flip-flops :*

   a) Divide-by-5 *b) Divide-by-11*
5. *Draw the complete timing diagram for the five stage synchronous binary counter.*
6. *A synchronous counter with three JK flip-flops has the following connections :*

   $J_A = K_A = \overline{Q_C}$, $J_B = K_B = Q_A$, $J_C = Q_A Q_B$, $K_C = Q_C$

   Determine its a) Modulus and b) the count sequence

   [Ans : a) 5 b) $Q_C Q_B Q_A$ = 000,001,010,011,100]
7. *Draw and explain the working of 4-bit UP/$\overline{\text{DOWN}}$ synchronous counter.*
8. *How synchronous counters differ from asynchronous counters ?*
9. *Write a short note on counter applications.*
10. *Draw the four bit Johnson counter and explain the operation.*
11. *Draw a four stage ring counter and explain its operation.*

❑❑❑

9

Op-amp Applications

9.1 Introduction

The operational amplifier, most commonly referred as **'op-amp'** was introduced in 1940s. The first operational amplifier was designed in 1948 using vacuum tubes. In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc. Due to its use in performing mathematical operations it has been given a name operational amplifier. Due to the use of vacuum tubes, the early op-amps were bulky, power consuming and expensive.

Robert J. Widlar at Fairchild brought out the popular 741 integrated circuit (IC) op-amp between 1964 to 1968. The IC version of op-amp uses BJTs and FETs which are fabricated along with the other supporting components, on a single semiconductor chip or wafer which is of a pinhead size. With the help of IC op-amp, the circuit design becomes very simple. The variety of useful circuits can be built without the necessity of knowing about the complex internal circuitry. Moreover, IC op-amps are inexpensive, take up less space and consume less power. The IC op-amp has become an integral part of almost every electronic circuit which uses linear integrated circuit. The modern linear IC op-amp works at **lower voltages.** It is so **low in cost** that millions are now in use, annually. Because of their **low cost, small size, versatility, flexibility,** and **dependability,** op-amps are used in the fields of process control, communications, computers, power and signal sources, displays and measuring systems. The op-amp is basically an excellent high gain d.c. amplifier.

9.2 Op-amp Symbol and Terminals

The symbol for an op-amp along with its various terminals, is shown in the Fig. 9.1.

The op-amp is indicated basically by a triangle which points in the direction of the signal flow.

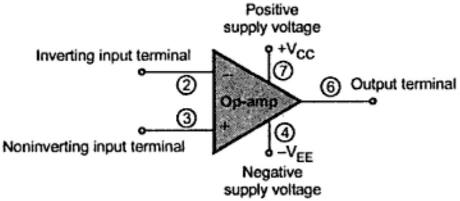

Positive
supply voltage
+V_{CC}
Inverting input terminal
②
⑦
⑥ Output terminal
Op-amp
③
④
Noninverting input terminal
$-V_{EE}$
Negative
supply voltage

Fig. 9.1 Op-amp symbol

All the op-amps have atleast following five terminals :

i. The positive supply voltage terminal V_{CC} or + V.

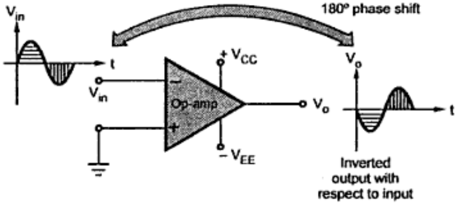
ii. The negative supply voltage terminal $-V_{EE}$ or $-$ V.

iii. The output terminal.

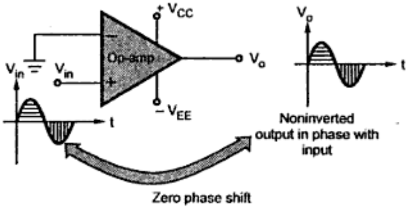
iv. The inverting input terminal, marked as negative.

v. The noninverting input terminal, marked as positive.

The input at inverting input terminal results in opposite polarity (antiphase) output. While the input at noninverting input terminal results in the same polarity (phase) output. This is shown in the Fig. 9.2 (a) and (b). The input and output are in antiphase means having 180° phase difference in between them while inphase input and output means having 0° phase difference in between them.


V_{in}
180° phase shift
t
+ V_{CC}
V_o
V_{in}
Op-amp
V_o
t
$-V_{EE}$
Inverted
output with
respect to input

(a) Input applied to inverting terminal


+ V_{CC}
V_o
V_{in}
V_{in}
Op-amp
V_o
t
t
$-V_{EE}$
Noninverted
output in phase with
input
Zero phase shift

(b) Input applied to noninverting terminal

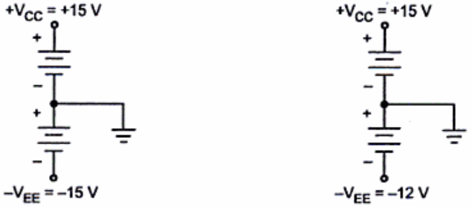
Fig. 9.2

The op-amp is fabricated on a tiny silicon chip and packaged in a suitable case. Fine gauge wires are used to connect the chip to the external leads.

9.2.1 Power Supply

The op-amp works on a dual supply. A **dual supply** consists of two supply voltages both d.c., whose middle point is generally the ground terminal.

The dual supply is generally balanced i.e. the voltages of the positive supply $+V_{CC}$ and that of the negative supply $-V_{EE}$ are same in magnitude. The typical commercially used power supply voltages are ± 15 V. But if the two voltage magnitudes are not same in a dual supply it is called as **unbalanced dual supply.** The balanced and unbalanced types of dual supply are shown in the Fig 9.3 (a) and (b) respectively.



(a) Balanced **(b) Unbalanced**

Fig. 9.3 Types of dual supply

Practically in most of the op-amp circuits balanced dual supply is used. The other popular balanced dual supply voltages are ± 9 V, ± 12 V, ± 22 V etc.

9.3 Ideal Op-amp

The ideal op-amp is basically an amplifier which amplifies the difference between the two input signals. In its basic form, the op-amp is nothing but a differential amplifier. To understand the characteristics of an ideal op-amp, let us discuss the operation of an ideal differential amplifier which is a basic building block of an op-amp.

9.3.1 Ideal Differential Amplifier

The differential amplifier amplifies the difference between two input voltage signals. Hence it is also called **difference amplifier.**

Consider an ideal differential amplifier shown in the Fig. 9.4.

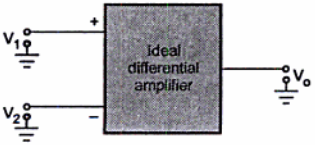


Fig. 9.4 Ideal differential amplifier

V_1 and V_2 are the two input signals while V_o is the single ended output. Each signal is measured with respect to the ground.

In an ideal differential amplifier, the output voltage V_o is proportional to the difference between the two input signals. Hence we can write,

$$V_o \propto (V_1 - V_2) \quad \ldots (1)$$

9.3.2 Differential Gain A_d

From the equation (1) we can write,

$$V_o = A_d (V_1 - V_2)$$

Where A_d is the constant of proportionality. The A_d is the gain with which differential amplifier amplifies the difference between two input signals. Hence it is called **differential gain** of the differential amplifier.

Thus, A_d = Differential gain

The difference between the two inputs $(V_1 - V_2)$ is generally called **difference voltage** and denoted as V_d.

$$\therefore \quad \boxed{V_o = A_d V_d}$$

Hence the differential gain can be expressed as,

$$\boxed{A_d = \frac{V_o}{V_d}}$$

Generally the differential gain is expressed in its decibel (dB) value as,

$$\boxed{A_d = 20 \operatorname{Log}_{10} (A_d) \text{ in dB}}$$

9.3.3 Common Mode Gain A_c

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. $V_1 = V_2$ then ideally the output voltage $V_o = (V_1 - V_2)A_d$, must be zero.

But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs. Such an average level of the two input signals is called **common mode signal** denoted as V_c.

$$\therefore \quad \boxed{V_c = \frac{V_1 + V_2}{2}}$$

Practically, the differential amplifier produces the output voltage proportional to such common mode signal, also. The gain with which it amplifies the common mode signal to produce the output is called **common mode gain** of the differential amplifier denoted as A_c.

$$\therefore \quad \boxed{V_o = A_c V_c}$$

Thus there exists some finite output for $V_1 = V_2$ due to such common mode gain A_c, in case of practical differential amplifiers.

So the total output of any differential amplifier can be expressed as,

$$\therefore \quad \boxed{V_o = A_d V_d + A_c V_c} \quad \text{... total output}$$

This shows that if one input is + 25 μV and other is –25 μV then the output of the amplifier will not be same, with the inputs as 600 μV and 650 μV, though the difference between the two sets of the inputs is 50 μV.

For an ideal differential amplifier, the differential gain A_d must be infinite while the common mode gain must be zero. This ensures zero output for $V_1 = V_2$.

But due to mismatch in the internal circuitry, there is some output available for $V_1 = V_2$ and gain A_c is not practically zero. The value of such common mode gain A_c is very very small while the value of the differential gain A_d is always very large.

At this stage, we can define one important parameter of the differential amplifier known as common mode rejection ratio (CMRR).

9.3.4 Common Mode Rejection Ratio (CMRR)

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signals appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier.

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called **common mode rejection ratio** denoted as CMRR or ρ.

It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_c.

$$\therefore \quad \boxed{\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right|}$$

Ideally the common mode voltage gain is zero, hence the ideal value of CMRR is infinite.

For a practical differential amplifier A_d is large and A_c is small hence the value of CMRR is also very large.

Many a times, CMRR is also expressed in dB, as

$$\therefore \quad \boxed{\text{CMRR in dB} = 20 \log \left| \frac{A_d}{A_c} \right| \text{ dB}}$$

Example 9.1 : *Determine the output voltage of a differential amplifier for the input voltages of 300 μV and 240 μV. The differential gain of the amplifier is 5000 and the value of the CMRR is i) 100 and ii) 10^5.*

Solution : The differential amplifier is represented as shown in the Fig. 9.5.

i) CMRR = 100

$$V_d = V_1 - V_2 = 300 - 240$$

$$= 60 \ \mu V$$

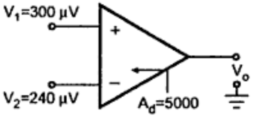


Fig. 9.5

$$V_c = \frac{V_1 + V_2}{2}$$

$$= \frac{300+240}{2}$$

$$= 270 \ \mu V$$

$$\text{CMRR} = \frac{A_d}{A_c}$$

$$\therefore \quad 100 = \frac{5000}{A_c}$$

$$\therefore \quad A_c = 50$$

$$\therefore \quad V_o = A_d \ V_d + A_c \ V_c = 5000 \times 60 + 50 \times 270$$

$$= 313500 \ \mu V = \mathbf{313.5 \ mV}$$

ii) CMRR = 10^5

$$\therefore \quad A_c = \frac{A_d}{\text{CMRR}} = \frac{5000}{10^5} = 0.05$$

$$\therefore \quad V_o = A_d V_d + A_c V_c = 5000 \times 60 + 0.05 \times 270$$

$$= 300013.5 \ \mu V = \mathbf{300.0135 \ mV}$$

Ideally A_c must be zero and output should be only $A_d V_d$ which is $5000 \times 60 \times 10^{-6}$ i.e. 300 mV. It can be seen that higher the value of CMRR, the output is almost proportional to the difference voltage V_d, rejecting the common mode signal. So ideal value of CMRR for a differential amplifier is ∞.

9.4 Saturable Property of Op-amp

The open loop gain of op-amp is very high. While every op-amp has a property that its output can swing between two levels decided by the supply voltages i.e. $+V_{CC}$ and $-V_{EE}$. Thus if output tries to rise more than $+V_{CC}$ or less than $-V_{EE}$ then it gets clipped and gets saturated at the levels almost equal to $+V_{CC}$ and $-V_{EE}$, on positive and negative side respectively.

Key Point : *The property by which op-amp output saturates at the two saturation levels* $(\pm V_{sat})$, *decided by the supply voltages, is called saturable property of an op-amp.*

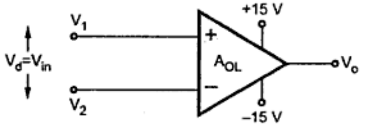


Fig. 9.6

Consider an op-amp shown in the Fig. 9.6. The value of A_{OL} is very high. Let it be 10^5. And supply voltages are ±15 V.

Now $V_o = V_d \times A_{OL}$

$$\therefore \quad V_d = \frac{V_o}{A_{OL}}$$

As the supply voltages are ±15 V, the op-amp has property to saturate the output at about ±15 V. Output cannot be produced exceeding the saturation voltage levels.

Key Point: *Thus* $V_o = \pm V_{sat}$ *in ideal condition.*

$$\therefore V_d = \frac{\pm V_{sat}}{A_{OL}} = \frac{\pm 15}{10^5} = \pm 150 \ \mu V$$

Thus only for the differential input of few μV, the output saturates to $+V_{sat}$ or $-V_{sat}$ depending on which input V_1 or V_2 is dominating. So if a sine wave of 1 mV is applied as the input then the output will be sine wave which is clipped at $\pm V_{sat} = \pm 15$ V, for the op-amp considered. This is shown in the Fig. 9.7.

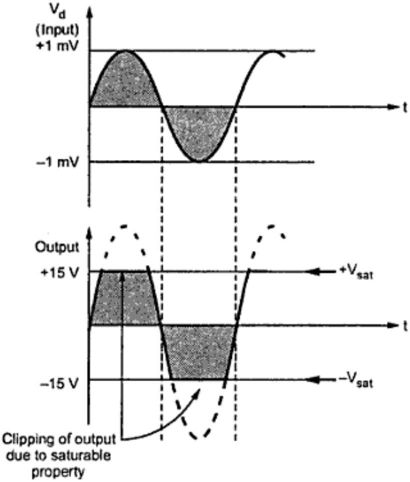


Fig. 9.7 Effect of saturable property

The expected amplitude of output sine wave is $10^5 \times 1\text{ mV} = 100\text{ V}$ but it gets clipped at ±15 V due to saturable property of the op-amp.

Key Point : *Practically the saturation voltage levels are about 90 % of the supply voltage levels.*

Thus for an op-amp of supply ±15 V the saturation voltage levels are 90 % of (± 15 V) i.e. 13.5 V.

9.5 Parameters of Ideal Op-amp

With the background of an ideal differential amplifier and CMRR, let us study the ideal op-amp characteristics.

The Fig. 9.8 shows an ideal op-amp. It has two input signals V_1 and V_2 applied to non-inverting and inverting terminals, respectively.

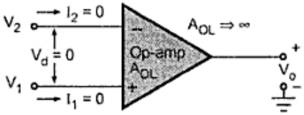


Fig. 9.8 Ideal op-amp

The following things can be observed for the ideal op-amp shown in the Fig. 9.8.

1) An ideal op-amp draws no current at both the input terminals i.e. $I_1 = I_2 = 0$. Thus its input impedance is infinite. Any source can drive it and there is no loading on the driver stage.
2) The gain of an ideal op-amp is infinite (∞), hence the differential input $V_d = V_1 - V_2$ is essentially zero for the finite output voltage V_o.
3) The output voltage V_o is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits.

These properties are expressed generally as the characteristics of an ideal op-amp. The various characteristics of an ideal op-amp are :

a) Infinite voltage gain : ($A_{OL} = \infty$)

It is denoted as A_{OL}. It is the differential open loop gain and is infinite for an ideal op-amp.

b) Infinite input impedance : ($R_{in} = \infty$)

The input impedance is denoted as R_{in} and is infinite for an ideal op-amp. This ensures that no current can flow into an ideal op-amp.

c) Zero output impedance : ($R_o = 0$)

The output impedance is denoted as R_o and is zero for an ideal op-amp. This ensures that the output voltage of the op-amp remains same, irrespective of the value of the load resistance connected.

d) Zero offset voltage : ($V_{ios} = 0$)

The presence of the small output voltage though $V_1 = V_2 = 0$ is called an offset voltage. It is zero for an ideal op-amp. This ensures zero output for zero input signal voltage.

e) Infinite bandwidth :

The range of frequency over which the amplifier performance is satisfactory is called its **bandwidth**. The bandwidth of an ideal op-amp is infinite. This means the operating frequency range is from 0 to ∞. This ensures that the gain of the op-amp will be constant over the frequency range from d.c. (zero frequency) to infinite frequency. So op-amp can amplify d.c. as well as a.c. signals.

f) Infinite CMRR : ($\rho = \infty$)

The ratio of differential gain and common mode gain is defined as CMRR. Thus infinite CMRR of an ideal op-amp ensures zero common mode gain. Due to this common mode noise output voltage is zero for an ideal op-amp.

g) Infinite slew rate : ($S = \infty$)

This ensures that the changes in the output voltage occur simultaneously with the changes in the input voltage.

The slew rate is important parameter of op-amp. When the input voltage applied is step type which changes instantaneously then the output also must change rapidly as input changes. If output does not change with the same rate as input then there occurs distortion in the output. Such a distortion is not desirable. **Infinite slew rate indicates that output changes simultaneously with the changes in the input voltage.**

The parameter slew rate is actually defined as the maximum rate of change of output voltage with time and expressed in V/µs.

$$\boxed{\text{Slew rate} = S = \left.\frac{dV_o}{dt}\right|_{\text{maximum}}}$$

Its ideal value is infinite for the op-amp.

h) No effect of temperature :

The characteristics of op-amp do not change with temperature.

i) Power supply rejection ratio : (PSRR = 0)

The power supply rejection ratio is defined as the ratio of the change in input off set voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called **power supply sensitivity.**

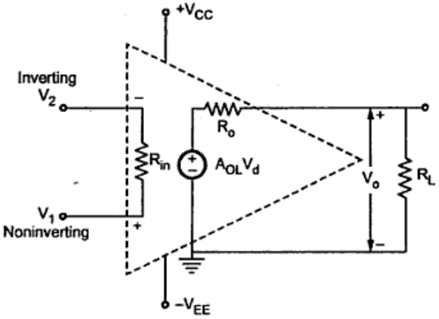


Fig. 9.9 Equivalent circuit of an op-amp

V_1 = Noninverting input voltage with respect to ground.

V_2 = Inverting input voltage with respect to ground.

R_i = Input resistance of op-amp

R_o = Output resistance of op-amp

The output voltage is directly proportional to the difference voltage V_d.

It is to be noted that the op-amp amplifies difference voltage and not the individual input voltages. Thus the output polarity gets decided by the polarity of the difference voltage V_d.

The voltage source $A_{OL} V_d$ is the Thevenin's equivalent voltage source while R_o is the Thevenin's equivalent resistance looking back into the output terminals.

The equivalent circuit plays an important role in analysing various op-amp applications as well as in studying the effects of feedback on the performance of op-amp.

9.7 Parameters of Practical Op-amp

The characteristics of an ideal op-amp can be approximated closely enough, for many practical op-amps. But basically the practical op-amp characteristics are little bit different than the ideal op-amp characteristics.

The various characteristics of a practical op-amp can be described as below.

a) Open loop gain : It is the voltage gain of the op-amp when no feedback is applied. Practically it is several thousands.

b) Input impedance : It is finite and typically greater than 1 MΩ. But using FETs for the input stage, it can be increased upto several hundred MΩ.

Example 9.3 : *For a particular op-amp, the input offset current is 20 nA while input bias current is 60 nA. Calculate the values of two input bias currents.*

Solution : $I_{ios} = 20$ nA, $I_b = 60$ nA

Now $I_{ios} = I_{b1} - I_{b2} = 20$

$$I_b = \frac{I_{b1} + I_{b2}}{2} = 60$$

$\therefore \quad I_{b1} + I_{b2} = 120$

$\therefore \quad 2I_{b1} = 140$

$\therefore \quad I_{b1} = \mathbf{70\ nA}, \quad I_{b2} = \mathbf{50\ nA}$

h) Power supply rejection ratio :

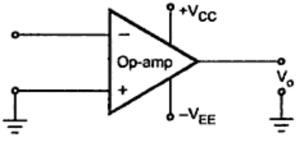


Fig. 9.12

The **Power Supply Rejection Ratio (PSRR)** is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called **power supply sensitivity (PSV).**

Now if V_{EE} is constant and due to certain change in V_{CC}, there is change in input offset voltage then PSRR is defined as,

$$\boxed{\text{PSRR} = \left.\frac{\Delta V_{ios}}{\Delta V_{CC}}\right|_{\text{constant } V_{EE}}} \quad \text{... (3)}$$

For a fixed V_{CC}, if there is a change in V_{EE} then

$$\boxed{\text{PSRR} = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{\text{constant } V_{CC}}} \quad \text{... (4)}$$

As input offset voltage is very small, PSRR is expressed in mV/V or µV/V.

The typical value of PSRR for IC 741 op-amp is 30 µV/V.

i) Slew rate :

The slew rate is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/µ sec. Thus

$$\boxed{\text{Slew rate} = S = \left.\frac{dV_o}{dt}\right|_{\max}} \quad \text{... (5)}$$

Thus the practical voltage transfer curve is as shown in the Fig. 9.14.

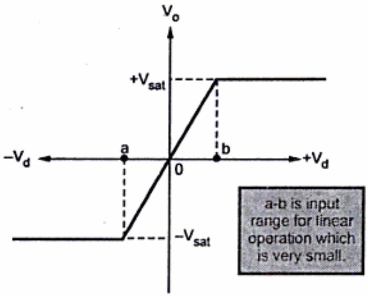


Fig. 9.14 Practical voltage transfer curve

Thus,

i) If V_d is greater than corresponding to b, the output attains $+ V_{sat}$.

ii) If V_d is less than corresponding to a, the output attains $- V_{sat}$.

iii) Thus range a-b is input range for which output varies linearily with the input. But as A_{OL} is very high, practically this range is very small.

9.9 Open Loop Configuration of Op-amp

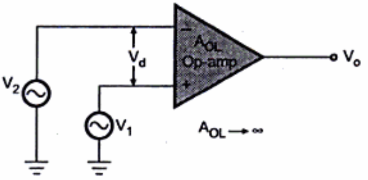


Fig. 9.15 Open loop operation of an op-amp

The simplest possible way to use an op-amp is in the open loop mode. The Fig. 9.15 shows an op-amp in the open loop condition.

We know that the d.c. supply voltages applied to the op-amp are V_{CC} and $-V_{EE}$ and the output varies linearily only between V_{CC} and $-V_{EE}$.

Since gain is very large in open loop condition, the output voltage V_o is either at its positive saturation voltage ($+ V_{sat}$) or negative saturation voltage ($- V_{sat}$) as $V_1 > V_2$ or $V_2 > V_1$ respectively. This is shown in the Fig. 9.16.

Thus very small noise voltage present at the input also gets amplified due to its high open loop gain and op-amp gets saturated.

9.11 Realistic Simplifying Assumptions

We can make two assumptions which are realistic and simplify the analysis of op-amp circuits to a great extent.

9.11.1 Zero Input Current

The current drawn by either of the input terminals (inverting and non-inverting) is zero.

In practice, the current drawn by the input terminals is very small, of the order μA or nA. Hence the assumption of zero input current is realistic.

9.11.2 Virtual Ground

This means the differential input voltage V_d between the noninverting and inverting input terminals is essentially zero.

This is obvious because even if output voltage is few volts, due to large open loop gain of op-amp, the difference voltage V_d at the input terminals is almost zero.

e.g. if output voltage is 10 V and the A_{OL} i.e. open loop gain is 10^4 then

$$V_o = V_d A_{OL}$$

$$\therefore \quad V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1 \text{ mV}$$

Hence V_d is very small. As $A_{OL} \rightarrow \infty$, the difference voltage $V_d \rightarrow 0$ and realistically assumed to be zero for analyzing the circuits.

$$\therefore \quad V_d = \frac{V_o}{A_{OL}}$$

$$\therefore \quad (V_1 - V_2) = \frac{V_o}{\infty} = 0$$

$$\therefore \quad V_1 = V_2 \qquad \text{... (1)}$$

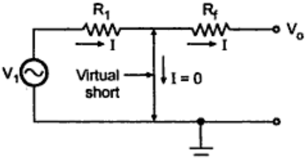


Fig. 9.18 Concept of virtual ground in an op-amp

Thus we can say that under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same. No current flows from the input terminals to the ground. The Fig. 9.18 shows the concept of the virtual ground. The thick line indicates the virtual short circuit between the input terminals.

Now if the noninverting terminal is grounded, by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection between the inverting terminal and the ground. This is the **principle of virtual ground.**

> **Key Point:** *Thus from the equation (1), **the voltage at the noninverting input terminal of an op-amp can be realistically assumed to be equal to the voltage at the inverting input terminal.***

The realistic simplifying assumptions are always used to analyse the practical op-amp applications. The steps of analysis based on the assumptions are,

Step 1 : Input current of the ideal op-amp is always zero. Using this, the current distribution in the circuit is obtained.

Step 2 : The input terminals of the op-amp are always at the same potential. Thus if one is grounded, the other can be treated to be virtually grounded. From this, the expressions for various branch currents can be obtained.

Step 3 : Analyzing the various expressions obtained, eliminating unwanted variables, the output expression in terms of input and circuit parameters can be obtained.

9.12 Op-amp Applications

The countless simple circuits using one or more operational amplifiers, some external resistors and the capacitors can be constructed. Such op-amp applications are classified as linear and nonlinear type of applications.

In the linear applications, output voltage varies linearily with respect to the input voltage. The negative feedback is the base of linear applications. Some of the linear applications are voltage follower, differential amplifier, instrumentation amplifier, inverting amplifier, noninverting amplifier etc.

In the nonlinear applications, a feedback is provided from the output to the input terminal. The feedback may be provided to the inverting input terminal using nonlinear elements like diodes, transistors etc. The nonlinear input to output characteristics is the feature of nonlinear applications. The typical nonlinear applications are precision rectifiers, comparators, clampers, limiters, schmitt trigger circuit etc.

While deriving the expressions and analysing such circuits, the **realistic assumptions** can be conviniently used. The op-amp input current is zero while the potential difference between inverting and noninverting terminals is zero. Thus if one terminal is grounded, then potential of other terminal can be assumed zero i.e. it is also at ground potential. This is the concept of virtual ground, which plays an important role in analysing the op-amp application circuits.

9.13 Basic Op-amp Applications

The basic op-amp applications can be the part of the complicated op-amp applications. Thus it is necessary to revise the circuits and expressions of output voltages of these basic applications. Such basic applications are given in Table 9.3.

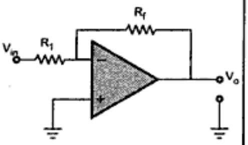
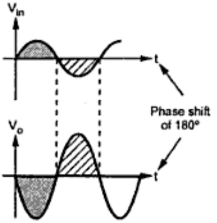
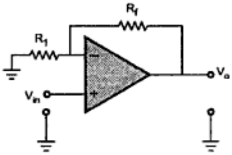
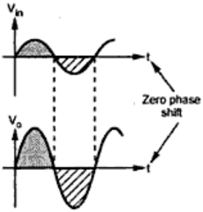
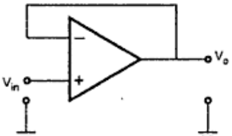
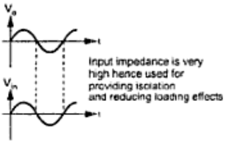
Application	Circuit Diagram	Output Voltage	Waveforms
Inverting amplifier		$V_o = -\frac{R_f}{R_1} V_{in}$	
Noninverting amplifier		$V_o = \left(1+\frac{R_f}{R_1}\right) V_{in}$	
Voltage follower		$V_o = V_{in}$ Unity gain or buffer amplifier	

Table 9.3 Basic op-amp applications

9.14 Op-amp as a Comparator

The op-amp in open loop configuration can be used as a basic comparator. When two inputs are applied to the open loop op-amp then it compares the two inputs. Depending upon the comparison, it produces output voltage which is either positive saturation voltage ($+ V_{sat}$) or negative saturation voltage ($- V_{sat}$).

A **comparator** is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input, and produce either a high or a low output voltage, depending on which input is higher. As comparator output has two voltage levels, either high or low, it is not linearly proportional to input voltage.

There are two types of comparator circuits which are,

1. Non-inverting comparator
2. Inverting comparator.

9.14.1 Basic Non-inverting Comparator

In this comparator, the input voltage is applied to the non-inverting terminal and no reference voltage is applied to other terminal. So inverting terminal is grounded. The input voltage is denoted as V_{in} while the voltage applied to other terminal with which V_{in} is compared is denoted as V_{ref}. In the basic comparator, $V_{ref} = 0$ V. The **basic non-inverting comparator** is shown in the Fig. 9.19.

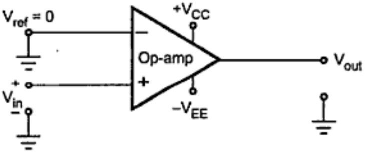


Fig. 9.19 Basic non-inverting comparator

In the non-inverting comparator, if V_{in} is greater than V_{ref} then output is $+ V_{sat}$ i.e. almost equal to $+ V_{CC}$. While if V_{in} is less than V_{ref} then output is $- V_{sat}$ i.e. almost equal to $- V_{EE}$.

Thus for Fig. 9.19, as $V_{ref} = 0$ V when V_{in} is positive then $V_o = + V_{sat} \approx + V_{CC}$ while when V_{in} is negative then $V_o = - V_{sat} \approx - V_{EE}$. This is because, as open loop gain op-amp (A_{OL}) is very very high even for very small V_{in} the op-amp output saturates.

Thus the two possible output levels of the comparator are $+ V_{sat}$ and $- V_{sat}$, indicating whether the input voltage is greater than or less than the reference voltage. Such type of the comparator, in which the operation is at saturation level is known as **saturating** type of comparator. Assuming symmetrical conditions, the two possible output levels of the saturating type comparator are $+ V_{sat}$ and $- V_{sat}$.

Note that no feedback is applied to the op-amp and it is operated in open loop conditions, because of which the op-amp is operating in saturating conditions.

The point at which the transfer characteristics is straight line is called a **trip point**. The trip point is the input voltage at which the output changes its states from low to high or high to low. In the basic comparator this trip point is zero as at $V_{in} = 0$, the output changes its states.

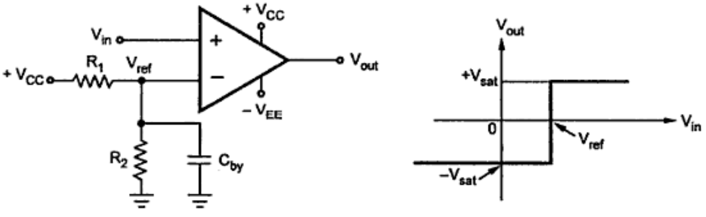
Key Point: *So we can say that when V_{in} is greater than trip point, the output is high while if V_{in} is less than the trip point the output is low.*

As this change over occurs at $V_{in} = 0$, the basic comparator can be used to detect occurrence of zero in the input voltage. Hence this circuit is called zero crossing detector. But in practice it is possible to change the trip point from zero to other voltage. This is achieved by some modifications in the basic comparator circuit.

Moving a Trip Point

By application of a reference voltage to the inverting input rather than grounding it, the trip point can be moved.

The Fig. 9.22 shows the application of reference voltage to the inverting input of a basic comparator using a potential divider consisting of resistors R_1 and R_2.



(a) Positive trip point circuit (b) Transfer characteristics

Fig. 9.22

The reference voltage V_{ref} is derived using supply $+ V_{CC}$ and potential divider R_1 and R_2. Mathematically V_{ref} is expressed as,

$$V_{ref} = \frac{+ V_{CC}}{R_1 + R_2} \cdot R_2$$

Now as long as input voltage V_{in} is less than V_{ref}, the output is low i.e. $- V_{sat}$. When V_{in} becomes slightly greater than V_{ref}, the op-amp output becomes high i.e. $+ V_{sat}$. Thus the trip point is moved from $V_{in} = 0$ to $V_{in} = V_{ref}$ due to reference voltage applied to the inverting input terminal.

A bypass capacitor is used on the inverting input to reduce the amount of power supply ripple and noise appearing at the inverting input of op-amp. For effective bypassing of ripple and noise, the critical frequency of the bypass circuit must be much lower than the ripple frequency of power supply.

9.14.2 Inverting Comparator

The Fig. 9.25 shows inverting comparator in which the reference voltage V_{ref} is applied to the non-inverting (+) input and signal voltage (V_{in}) is applied to the inverting (–) input of the op-amp. The V_{ref} can be set using a battery and potential divider as discussed earlier for non-inverting comparator.

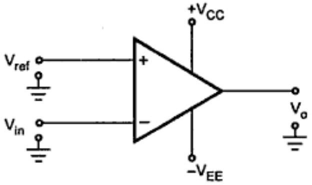


Fig. 9.25 Basic inverting comparator with V_{ref} = 0 V

When V_{in} is less than V_{ref}, the output voltage V_o is at $+V_{sat}$ ($\cong +V_{CC}$) because the voltage at the inverting input (–) is less than that at the non-inverting (+) input. On the other hand, when V_{in} is greater than V_{ref}, the non-inverting (+) input becomes negative with respect to the inverting (–) input, and V_o goes to $-V_{sat}$ ($\cong -V_{EE}$). The Fig. 9.26 shows the input and output waveforms for inverting comparator.

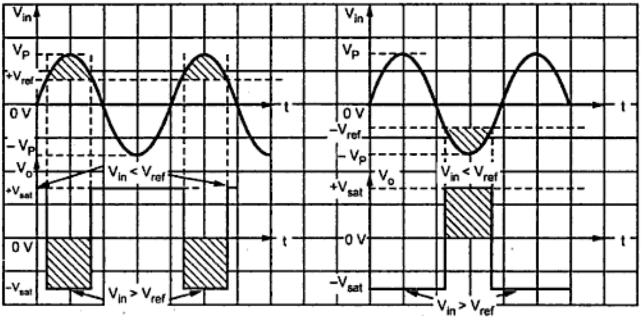


Fig. 9.26 Input and output waveforms for inverting comparator

Transfer characteristics for inverting comparator with $+V_{ref}$ is shown in the Fig. 9.27.

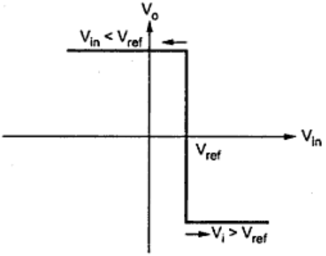


Fig. 9.27 Transfer characteristics for inverting comparator

9.14.3 Practical Comparator

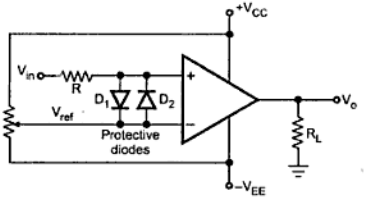


Fig. 9.28 Practical comparator circuit

The Fig. 9.28 shows practical comparator circuit. It consists of protective diodes and potentiometer to adjust the reference voltage.

As shown in Fig. 9.28 diode D_1 and diode D_2 are connected to protect the op-amp from damage due to excessive input voltage V_{in}. Because of these diodes, the difference input voltage V_{id} is always less than 0.7 V or –0.7 V. In case of excess input voltage, the difference input voltage V_{id} of the op-amp is clamped to either 0.7 V or – 0.7 V due to the forward biasing of one of the diodes. Hence, these diodes are also called as **clamp diodes**. Some op-amps have built-in input protection circuitry; they don't require external clamp diodes. The resistance R in series with V_{in} is used to limit the current through D_1 and D_2. The potentiometer acts as a voltage divider and allows reference voltage to set any value between $+V_{CC}$ to $-V_{EE}$.

9.15 Schmitt Trigger (Regenerative Comparator)

We have seen that in a basic comparator, a feedback is not used and the op-amp is used in the open loop mode. As open loop gain of op-amp is large, very small noise voltages also can cause triggering of the comparator, to change its state. Such a false triggering may cause lot of problems in the applications of comparator as zero crossing detector. This may give a wrong indication of zero crossing due to zero crossing of noise voltage rather than zero crossing of input wanted signal. Such unwanted noise causes the output to jump between high and low states. The comparator circuit used to avoid such unwanted triggering is called **regenerative comparator** or **Schmitt trigger**, which basically uses a **positive feedback**.

9.15.1 Basic Inverting Schmitt Trigger Circuit

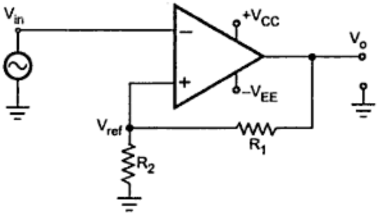


Fig. 9.29 Inverting Schmitt trigger

The Fig. 9.29 shows the basic Schmitt trigger circuit. As the input is applied to the inverting terminal, it is also called inverting Schmitt trigger circuit. The inverting mode produces opposite polarity output. This is fedback to the non-inverting input which is of same polarity as that of output. This ensures positive feedback.

When V_{in} is slightly positive than V_{ref}, the output gets driven into negative saturation at $-V_{sat}$ level.

When V_{in} becomes more negative than $-V_{ref}$, then output gets driven into positive saturation at $+V_{sat}$ level.

Thus output voltage is always at $+V_{sat}$ or $-V_{sat}$ but the voltage at which it changes its state now can be controlled by the resistance R_1 and R_2. Thus V_{ref} can be obtained as per the requirement.

Now R_1 and R_2 forms a potential divider and we can write,

$$+V_{ref} = \frac{V_o}{R_1+R_2} \times R_2 = \frac{+V_{sat}}{R_1+R_2} \times R_2 \quad \text{.... positive saturation}$$

$$-V_{ref} = \frac{V_o}{R_1+R_2} \times R_2 = \frac{-V_{sat}}{R_1+R_2} \times R_2 \quad \text{.... negative saturation}$$

$+V_{ref}$ is for positive saturation when $V_o = +V_{sat}$ and is called **upper threshold voltage** denoted as V_{UT}. $-V_{ref}$ is for negative saturation when $V_o = -V_{sat}$ and is called **lower threshold voltage** denoted as V_{LT}. The values of these threshold voltage levels can be determined and adjusted by selecting proper values of R_1 and R_2.

Thus
$$\boxed{V_{UT} = \frac{+V_{sat}\ R_2}{(R_1+R_2)}}$$

and
$$\boxed{V_{LT} = \frac{-V_{sat}\ R_2}{(R_1+R_2)}}$$

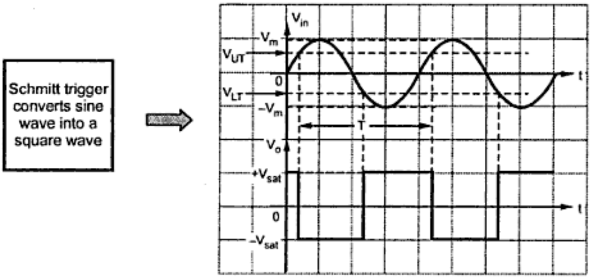


Fig. 9.31 Input and output waveforms of inverting Schmitt trigger

Design steps : Let the current through R_1 and R_2 is I_2. The op-amp input current is assumed zero.

$$\boxed{R_2 = \frac{\text{Trigger voltage}}{I_2}}$$

Where I_2 is selected much higher than op-amp input bias current.

While $$\boxed{R_1 = \frac{V_o - (\text{Trigger voltage})}{I_2}} \quad \dots V_o = V_{sat}$$

For BiFET op-amps, select largest of the two resistors as 1 MΩ and then calculate other.

Example 9.4 : *Design an inverting Schmitt trigger to have trigger voltages of ± 4 V. Use op-amp 741 with supply of ± 15 V.*

Solution : $V_{UT} = +4\text{ V}, \; V_{LT} = -4\text{ V}, \; \text{Supply} = \pm 15\text{ V}$

$$\pm V_{sat} = 0.9 \times [\text{Supply}] = \pm 13.5\text{ V} = V_o$$

For op-amp 741, $I_{B(max)} = 500\text{ nA}$

$$\therefore \quad I_2 = 100\, I_{B(max)} = 50\,\mu\text{A} \quad \dots I_2 \text{ must be high}$$

$$\therefore \quad R_2 = \frac{V_{UT}}{I_2} = \frac{4}{50 \times 10^{-6}} = 80\text{ k}\Omega \text{ (Use } \mathbf{82\text{ k}\Omega} \text{ standard)}$$

$$\text{Recalculate } I_2, \quad I_2 = \frac{V_{UT}}{R_2} = \frac{4}{82 \times 10^{3}} = 48.78\,\mu\text{A}$$

$$\therefore \quad R_1 = \frac{V_o - V_{UT}}{I_2} = \frac{+V_{sat} - V_{UT}}{I_2} = \frac{13.5 - 4}{48.78 \times 10^{-6}}$$

$$= \mathbf{194.75\text{ k}\Omega \text{ (Use 180 k}\Omega \text{ standard)}}$$

Now V_A = Voltage at point A $= I_{in} R_2$

$= V_{UT}$

As op-amp input current is zero, I_{in} entirely passes through R_1.

$$\therefore \quad I_{in} = \frac{V_o}{R_1} = \frac{+V_{sat}}{R_1}$$

$$\therefore \quad \boxed{V_{UT} = I_{in}\ R_2 = \frac{R_2}{R_1}(+V_{sat}) = V_{sat}\ \frac{R_2}{R_1}}$$

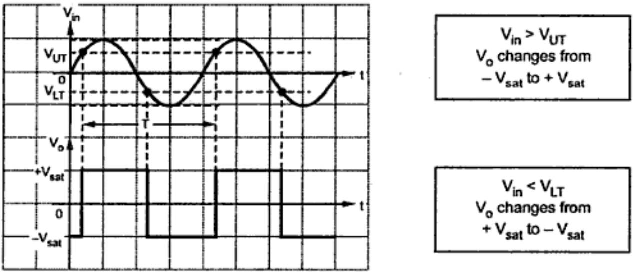
and

$$V_{LT} = \frac{R_2}{R_1}(-V_{sat}) = -V_{sat}\ \frac{R_2}{R_1}$$

and

$$H = V_{UT} - V_{LT} = 2\ V_{sat}\ \frac{R_2}{R_1}$$

If sinusoidal input is applied to the noninverting Schmitt trigger, the input and output waveforms can be shown as in the Fig. 9.35.



$V_{in} > V_{UT}$
V_o changes from
$-V_{sat}$ to $+V_{sat}$

$V_{in} < V_{LT}$
V_o changes from
$+V_{sat}$ to $-V_{sat}$

Fig. 9.35 Input and output waveforms

➡ **Example 9.5 :** *For a Schmitt trigger shown in the Fig. 9.36, calculate threshold voltage levels and hysteresis. Assume* $V_{sat} = 0.9\ V_{CC}$.

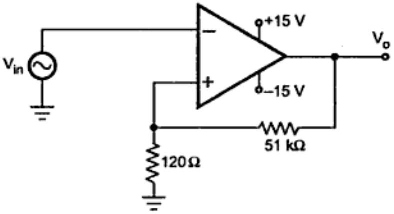


Fig. 9.36

Solution :

$$V_{CC} = +15\ V$$

$$\therefore\quad V_{sat} = 0.9\ V_{CC} = 0.9\times15 = 13.5\ V$$

$$R_1 = 51\ k\Omega, \qquad R_2 = 120\ \Omega$$

$$V_{UT} = \frac{+V_{sat}\ R_2}{R_1+R_2} = \frac{13.5\times120}{51\times10^3+120} = \mathbf{0.03169\ V}$$

$$V_{LT} = \frac{-V_{sat}\ R_2}{R_1+R_2} = \frac{-13.5\times120}{51\times10^3+120} = \mathbf{-0.03169\ V}$$

$$H = V_{UT}-V_{LT} = 0.03169-(-0.03169)$$

$$= 0.06338\ V = \mathbf{63.38\ mV}$$

Example 9.6 : *For a non-inverting regenerative comparator shown in the Fig. 9.37, calculate tripping voltages. Assume* $V_{sat} = \pm 13.5\ V$.

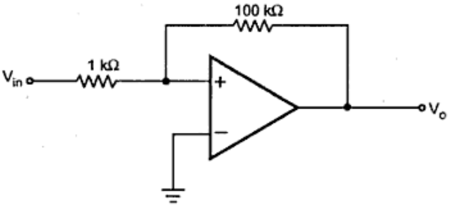


Fig. 9.37

Solution : As input is applied to the non-inverting terminal, the circuit is non-inverting Schmitt trigger.

$$R_1 = 100\ k\Omega, \qquad R_2 = 1\ k\Omega$$

$$\therefore\quad V_{UT} = +V_{sat}\ \frac{R_2}{R_1} = 13.5\times\frac{1}{100} = \mathbf{0.135\ V}$$

$$V_{LT} = -V_{sat}\ \frac{R_2}{R_1} = \frac{-13.5\times1}{100} = \mathbf{-0.135\ V}$$

9.16 Schmitt Trigger Applications

We have already seen one important application of Schmitt trigger as sine to square wave converter. It can be used to eliminate comparator chatter in signal shaping and in ON/OFF control. It is a building block of relaxation oscillators.

9.16.1 Schmitt Triggers for Eliminating Comparator Chatter

Chattering can be defined as production of multiple output transition as the input signal swings through the threshold region of a comparator. This happens due to the fact that a.c. noise is present in the practical circuits. Fig. 9.38 shows input signal with a.c. noise and how comparator output chatters. Even if noise is very less, it takes a very small noise spike to cause chatter due to high comparator gains.

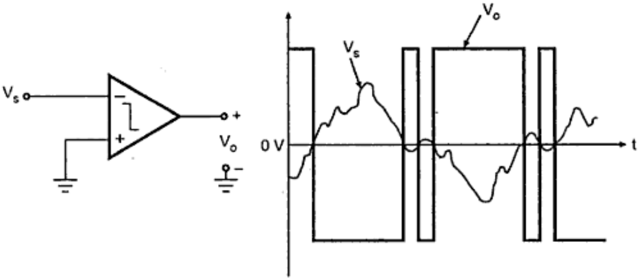


Fig. 9.38

This problem can be solved by using Schmitt trigger circuits. This is because they exhibit Hysteresis. In case of Hysteresis, as soon as the input signal crosses the present threshold level once, the output changes its state and activates the other threshold level, so that the input signal must swing back to the new threshold in order to make the output of the circuit to change its state again. Refer Fig. 9.39. By making Hysteresis width greater than the maximum peak amplitude of noise, a dead zone is created such that noise within this zone no longer causes multiple output transitions.

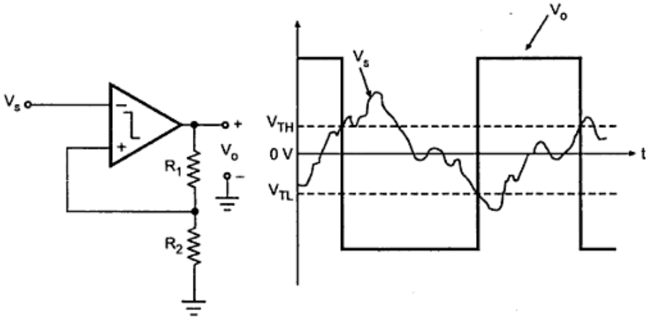


Fig. 9.39

➠ Example 9.8 : *A Schmitt trigger with Hysteresis width 2 V and LTP of – 1.5 V converts a 1 kHz sine wave of 5 V peak into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.*

Solution : Let us draw the input and output waveforms as shown in the Fig. 9.43.

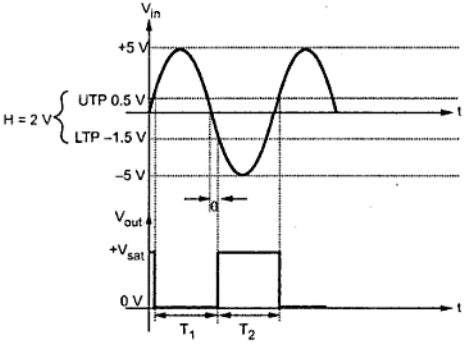


Fig. 9.43

$$LTP = -1.5\text{ V} \quad \text{and}$$

$$H = 2\text{ V}$$

Now $\quad H = UTP - LTP$

$\therefore \quad 2 = UTP - (-1.5)$

$\therefore \quad UTP = 0.5\text{ V}$

$$V_p = 5\text{ V}$$

In the Fig. 9.47, the angle θ can be obtained from equation of sine wave. Sine wave is represented as,

$V_{in} = V_p \sin(\pi + \theta)$ when $\pi < \omega t < 2\pi$

At LTP, $\quad -1.5 = 5 \sin(\pi + \theta)$

$$= -5 \sin\theta$$

$\therefore \quad \sin\theta = 0.3$

$\therefore \quad \theta = 17.45°$

The time period of sine wave is,

$$T = \frac{1}{f} = \frac{1}{1 \times 10^3} = 1\text{ ms}$$

At UTP, $\quad 0.5 = V_p \sin\theta$

$\therefore \quad 0.5 = 5 \sin\theta$

$\therefore \quad \sin\theta = 0.1$

$\therefore \quad \theta = 5.739°$

The time T_1 for output is from 5.739° to (180° + 17.45°)

$\therefore \quad T_1 = 197.45° - 5.739° = 191.71°$

i.e. $$T_1 = \frac{191.71° \times 1\text{ms}}{360°} = \mathbf{0.5325\ ms}$$

and $$T_2 = T - T_1 = 1 - 0.5325$$

$$= \mathbf{0.4674\ ms}$$

Example 9.9 : *For the circuit shown in the Fig. 9.44 calculate the values of R_1 and R_2 if saturation voltages are +12 V and –12 V. Assume hysteresis width = 6 V.*

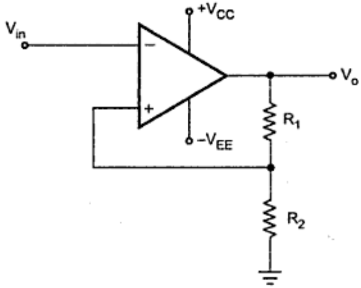


Fig. 9.44

Solution : Given $+V_{sat} = 12$ V $-V_{sat} = -12$ V $V_H = 6$ V

We know that Hysteresis width is given as

$$V_H = \frac{R_2}{R_1 + R_2}[+V_{sat} - V_{sat}]$$

$$\therefore \quad \frac{R_2}{R_1+R_2} = \frac{V_H}{[+V_{sat} - V_{sat}]}$$

$$\therefore \quad \frac{R_2}{R_1+R_2} = \frac{6}{[12-(-12)]}$$

$$\therefore \quad \frac{R_2}{R_1+R_2} = 0.25$$

$$\therefore \quad R_2 = 0.25\,R_1 + 0.25\,R_2$$

$$\therefore \quad 0.75\,R_2 = 0.25\,R_1$$

$$\therefore \quad \frac{R_2}{R_1} = 0.3333$$

Assuming $$R_2 = \mathbf{10\ k\Omega}$$

$$R_1 = \frac{10000}{0.3333} = \mathbf{30\ k\Omega}$$

Example 9.10 : *For the Schmitt trigger shown in the Fig. 9.45, calculate the trip points and hysteresis, if $V_{sat} = \pm 13.5$ V. If the resistances have a tolerance of ± 5 %, what is the minimum Hysteresis?.*

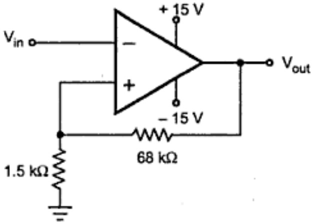


Fig. 9.45

Solution : From the Fig. 9.45, $R_1 = 68$ kΩ, $R_2 = 1.5$ kΩ and $V_{sat} = 13.5$ V

$$V_{UT} = \frac{R_2}{R_1+R_2} V_{sat} = \frac{1.5}{1.5+68} \times 13.5 = \mathbf{0.2913\ V}$$

$$V_{LT} = \frac{-R_2}{R_1+R_2} V_{sat} = \mathbf{-\ 0.2913\ V}$$

$$\therefore \quad H = V_{UT} - V_{LT} = 0.2913 - (-0.2913) = \mathbf{+\ 0.5828\ V}$$

Now $$H = \frac{2R_2}{R_1+R_2} \cdot V_{sat}$$

For minimum H, R_2 must be minimum and R_1 must be maximum

$$\therefore \quad R_{2\,min} = R_2 - 5\%\ R_2 = 1.5 \times 10^3 - 0.05 \times 1.5 \times 10^3 = 1.425\ \text{k}\Omega$$

and $$R_{1\,max} = R_1 + 5\%\ R_1 = 68 \times 10^3 + 0.05 \times 68 \times 10^3 = 71.4\ \text{k}\Omega$$

$$\therefore \quad H_{min} = \left[\frac{2 \times 1.425 \times 10^3}{71.4 \times 10^3 + 1.425 \times 10^3}\right] \times 13.5 = \mathbf{0.528\ V}$$

Example 9.11 : *Design a Schmitt trigger whose V_{LT} and V_{UT} are ± 5 V. Draw its waveforms.*

Solution : Choose op-amp LM318 with V_{sat} as ± 13.5 V with supply voltage ± 15 V.

$$V_{UT} = +5\ \text{V}$$

Now $$V_{UT} = \frac{R_2}{R_1+R_2} V_{sat}$$

$$\therefore \quad 5 = \frac{R_2}{R_1+R_2} \times 13.5$$

$$\therefore \quad R_1 + R_2 = 2.7\, R_2$$

$$\therefore \quad R_1 = 1.7\, R_2 \qquad \ldots(1)$$

Choose $R_2 = 10\ \text{k}\Omega$

$$\therefore \quad R_1 = 1.7 \times 10 = 17\ \text{k}\Omega$$

The designed circuit is shown in the Fig. 9.46 (a) while its waveforms are shown in the Fig. 9.46 (b).

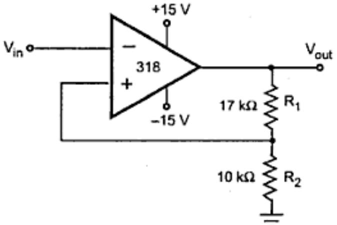


Fig. 9.46 (a)

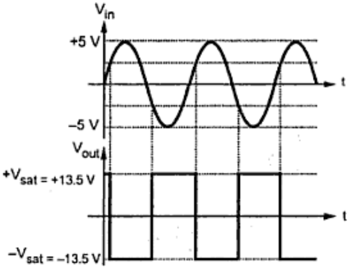


Fig. 9.46 (b)

9.18 Schmitt Trigger with Different UTP and LTP Levels

Uptill now the Schmitt trigger circuits with equal magnitudes of trigger levels are discussed . But for many practical application, the Schmitt trigger with different UPT and LTP levels are necessary. By using diodes in the basic circuits, modified Schmitt trigger circuits can be achieved.

9.18.1 Modified Inverting Schmitt Trigger

By using single diode in series with the resistance R_1, any positive level of UTP with zero LTP level can be achieved as shown in the Fig. 9.47.

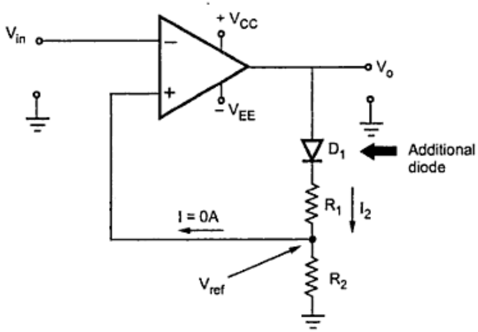


Fig. 9.47 Modified inverting Schmitt trigger

When the output is negative saturation voltage ($-V_{sat}$), the diode D_1 is reverse biased and current I_2 is almost zero. Thus the drop across R_2 which decides V_{ref} is zero. This gives,

$$V_{LT} = LTP = 0\text{ V}$$

When the output is positive saturtion voltage ($+V_{sat}$), the diode D_1 is forward biased.

Then the drop across R_2 due to I_2 decides the V_{ref} i.e. UTP level of the circuit.

Let V_F = The drop across forward biased diode ≈ 0.7 V.

$$I_2 = \frac{V_0 - V_F}{R_1 + R_2}$$

$$\therefore \quad \boxed{UTP = V_{UT} = \frac{V_o - V_F}{R_1 + R_2} \times R_2} \qquad \text{Where } V_o = +V_{sat}$$

The diode D_1 must have peak inverse voltage rating more than the supply voltage.

PIV of D_1 > Supply voltage

The maximum reverse recovery time (t_{rr}) of the diode must be very much smaller than the minimum pulse width of the input signal.

$$\therefore \quad \boxed{t_{rr} \le \frac{\text{Minimum pulse width}}{10}}$$

Key Point: *By reversing the direction of the diode D_1, any negative level of LTP with zero UTP level can be achieved.*

By using two diodes, in series with two different resistances, two different UTP and LTP levels can be achieved. This is shown in the Fig. 9.48.

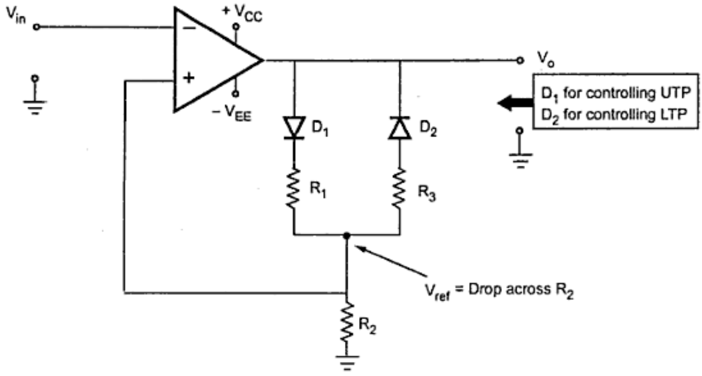

V_in
+V_CC
-V_EE
V_o
D_1 for controlling UTP
D_2 for controlling LTP
D_1
D_2
R_1
R_3
V_ref = Drop across R_2
R_2

Fig. 9.48 Achieving different UTP and LTP levels in an inverting Schemitt trigger

When the output is positive , D_1 is forward biased and drop across R_2 decides UTP levels.

$$\boxed{\text{UTP} = \frac{V_o - V_F}{R_1 + R_2} \times R_2}$$

When the output is negative , D_2 is forward biased and drop across R_2 decides LTP levels,

$$\boxed{\text{LTP} = \frac{V_o - V_F}{R_2 + R_3} \times R_2}$$

By varing the values of R_1 and R_3 , any desired UTP and LTP levels can be achieved.

9.18.2 Modified Noninverting Schmitt Trigger

Similar to an inverting Schmitt trigger, a diode in series with resistor R_1, can be used to achieve any desired positive UTP level with zero LTP level. The circuit is shown in the Fig. 9.49.

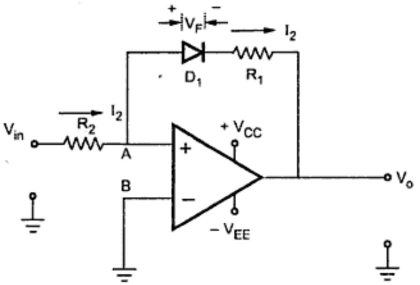

+
−
V_F
I₂
D₁
R₁
I₂
V_in
R₂
A
B
+
−
+ V_CC
− V_EE
V_o

Fig. 9.49 Modified noninverting Schmitt trigger

When the output is positive, the diode D_1 is reverse biased. Thus the voltage of node A is V_{in}. The output switches from positive to negative saturation level, when v_{in} just goes negative. When the output is negative, the diode is forward biased and UTP level is then decided as,

$$\boxed{\text{UTP} = I_2 R_2 = \frac{|V_o| - V_F}{R_1} \times R_2}$$

Where V_F is the drop across the forward biased diode.

Key Point: *By reversing the direction of diode D_1, any negative levels of LTP with zero UTP level can be achieved.*

By using two diodes , in series with two different resistances R_1 and R_3 , two different UTP and LTP levels can be achieved. This is shown in the Fig. 9.50.

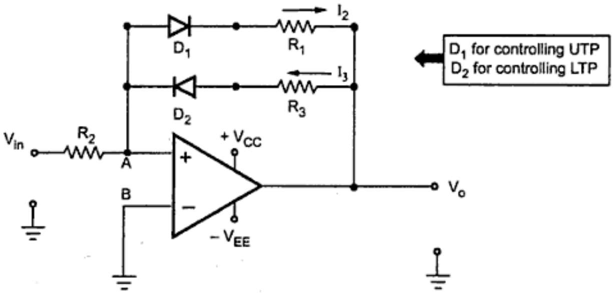

I₂
D₁
R₁
I₃
D₂
R₃
D₁ for controlling UTP
D₂ for controlling LTP
V_in
R₂
A
B
+
−
+ V_CC
− V_EE
V_o

Fig. 9.50 Achieving different UTP and LTP levels in noninverting Schmitt Trigger

The UTP and LTP levels are given by,

$$\boxed{\text{UTP} = \frac{|V_o|-V_F}{R_1}\times R_2 \quad \text{and} \quad \text{LTP} = \frac{|V_o|-V_F}{R_3}\times R_2}$$

9.19 Another Method of Obtaining Different UTP and LTP Levels

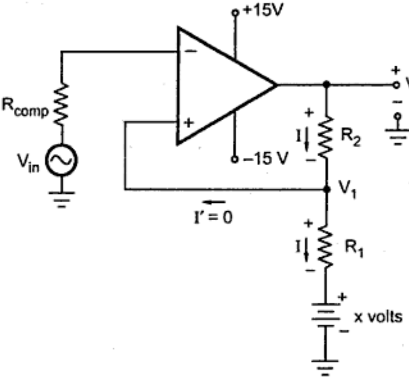


Fig. 9.51

Uptill now Schmitt trigger with equal positive and negative values of UPT and LTP values is studied. In practice, it is required to have different UTP and LTP levels for the Schmitt trigger.

In such a case, the basic Schmitt trigger circuit is modified as shown in the Fig. 9.51.

An additional voltage source of 'x' volts is connected in series between R_1 and ground. The voltage V_1 now depends on 'x' and decides the UTP and LTP levels. For $\pm V_{sat}$, two different values of V_1 can be obtained. Thus the circuit acts as a Schmitt trigger with different UTP and LTP levels. For designing such circuit, apply KVL to the output circuit, neglecting op-amp input current.

$$-IR_2 - IR_1 - x + V_o = 0$$

$$\therefore \quad I = \frac{V_o - x}{R_1 + R_2} \quad \text{... (1)}$$

$$\text{And} \quad V_1 = IR_1 + x \quad \text{... (2)}$$

$$\therefore \quad V_1 = \frac{(V_o - x)\,R_1}{R_1 + R_2} + x \quad \text{... (3)}$$

$$\text{For} \quad V_1 = V_{UT},\ V_o = +V_{sat}$$

$$\therefore \quad \boxed{V_{UT} = \frac{(+V_{sat} - x)\,R_1}{R_1 + R_2} + x} \quad \text{... (4)}$$

$$\text{For} \quad V_1 = V_{LT},\ V_o = -V_{sat}$$

$$\therefore \quad \boxed{V_{LT} = \frac{(-V_{sat} - x) R_1}{R_1 + R_2} + x} \quad \text{... (5)}$$

Subtracting (5) from (4),

$$\boxed{(V_{UT} - V_{LT}) = \frac{2V_{sat} R_1}{R_1 + R_2}} \quad \text{... (6)}$$

This gives the relation between R_1 and R_2. Substituting $(R_1 + R_2)$ interms of R_1 in equation (4), the value of x can be obtained. Then by choosing R_1, the value of R_2 can be obtained.

Finally, $R_{comp} = R_1 || R_2$

If value of 'x' is negative, it should be connected with opposite polarity in the circuit, compared to what is shown in the Fig. 9.54.

Example 9.12 : *Design an op-amp Schmitt trigger with the following specifications : UTP = 2 V, LTP = – 4 V and the output swings between ± 10 V.*

If input is 5 sin ωt, plot the waveforms of input and output.

Solution : For the Schmitt trigger

$V_{UT} = 2$ V, $V_{LT} = -4$ V, $\pm V_{sat} = \pm 10$ V

For unequal UTP and LTP values, a modified circuit is required as shown in the Fig. 9.52.

The voltage V_1 decides the UTP and LTP levels. Applying KVL to the output circuit and neglecting op-amp input current we can write,

$$-IR_2 - IR_1 - x + V_o = 0$$

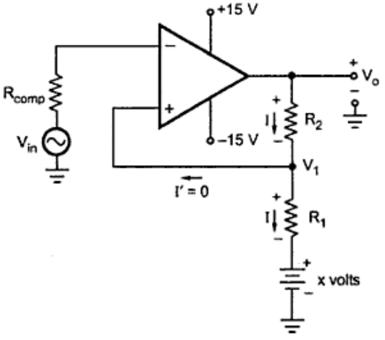


Fig. 9.52

$$\therefore \quad I = \frac{V_o - x}{R_1 + R_2} \quad \text{... (7)}$$

And $V_1 = IR_1 + x$ ... (8)

$$\therefore \quad V_1 = \frac{V_o - x}{R_1 + R_2} \cdot R_1 + x \quad \text{... (9)}$$

For $+V_{sat} = 10$ V,

$V_1 = V_{UT} = 2$ V,

$V_o = 10$ V

$$\therefore \quad 2 = \frac{10 - x}{R_1 + R_2} \cdot R_1 + x \quad \text{... (10)}$$

For $-V_{sat} = -10$ V,

$V_1 = V_{LT} = -4$ V,

The diode D_1 is clamping diode connected across C. The diode clamps the capacitor voltage to 0.7 V when the output is at $+V_{sat}$. A narrow negative triggering pulse V_t is applied to the noninverting input terminal, through diode D_2.

Let us see the operation of the circuit.

To understand the operation of the circuit, let us assume that the output V_o is at $+V_{sat}$ i.e. in its stable state. The diode D_1 conducts and the voltage across the capacitor C i.e. V_C gets clamped to 0.7 V. The voltage at the non-inverting input terminal is controlled by potentiometric divider of R_1R_2 to βV_o i.e. $+\beta V_{sat}$ in the stable state.

Now if V_t, a negative trigger of amplitude V_t is applied to the non-inverting terminal, so that the effective voltage at this terminal is less than 0.7 V $(+\beta V_{sat} + (-V_t))$ then the output of the op-amp changes its state from $+V_{sat}$ to $-V_{sat}$.

The diode is now reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The time constant of this charging is $\tau = RC$.

The voltage at the non-inverting input terminal is now $-\beta V_{sat}$. When the capacitor voltage V_C becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp changes its state back to $+V_{sat}$.

The capacitor now starts charging towards $+V_{sat}$ through R until V_C reaches 0.7 V as capacitor gets clamped to the voltage.

The waveforms are shown in the Fig. 9.55.

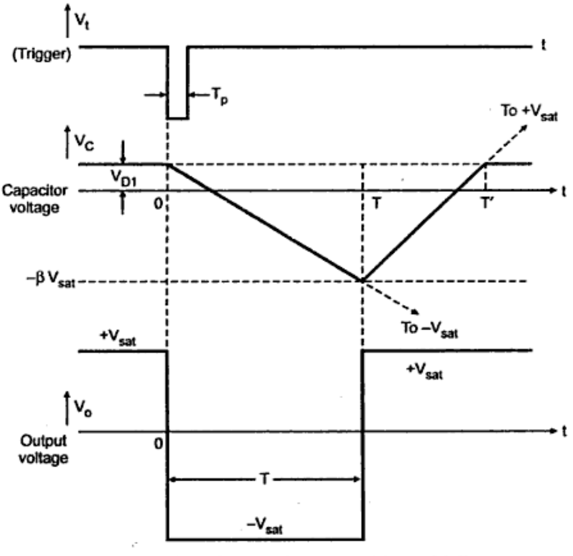


Fig. 9.55 Waveforms of monostable multivibrator

9.21.1 Expression for Pulse Width T

For a low pass RC circuit let,

V_i = Initial value of the voltage

V_f = Final value of the voltage

Then the general solution is given by,

$$V_o = V_f + (V_i - V_f)\, e^{-t/RC} \qquad \dots (1)$$

Now for the monostable multivibrator discussed above, the values of V_f and V_i are,

$$V_f = -V_{sat} \text{ and } V_i = V_{D1} \text{ (diode forward voltage)}$$

while V_o = Output = Capacitor voltage = V_C

$$\therefore \quad V_C = -V_{sat} + (V_{D1} - [-V_{sat}])\, e^{-t/RC} \qquad \dots (2)$$

$$\text{at } t = T, \quad V_C = -\beta V_{sat} \qquad \dots (3)$$

$$\therefore \quad -\beta V_{sat} = -V_{sat} + (V_{D1} + V_{sat})\, e^{-T/RC} \qquad \dots (4)$$

$$\therefore \quad (V_{D1} + V_{sat})\, e^{-T/RC} = V_{sat}(1-\beta)$$

$$\therefore \quad e^{-T/RC} = \frac{V_{sat}(1-\beta)}{(V_{D1} + V_{sat})}$$

$$\therefore \quad \boxed{T = RC\, ln\left[\frac{1 + V_{D1}/V_{sat}}{1-\beta}\right]} \qquad \dots (5)$$

This is obtained by absorbing negative sign inside the natural logarithm.

The potential divider decides the value of β given by,

$$\beta = \frac{R_2}{R_1 + R_2} \qquad \dots (6)$$

If $V_{sat} >> V_{D1}$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$\boxed{T = 0.69\ RC} \qquad \dots (7)$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator.

The diode D_2 is not essential but it is used to avoid malfunctioning if any positive noise spikes are present in the triggering line. It can be seen from the waveform that the voltage V_C does not reach its quiescent value V_{D1} until time $T' > T$. Hence it is necessary that a recovery time $T' - T$ be allowed to elapse before the next triggering signal is applied.

9.22 Astable Multivibrator using Op-amp

In this section we are going to study astable multivibrator operation using op-amp. Fig. 9.56 shows astable multivibrator circuit using op-amp. It looks like a comparator with Hysteresis (Schmitt trigger), except that the input voltage is replaced by a capacitor. The circuit has a time dependent elements such as resistance and capacitor to set the frequency of oscillation.

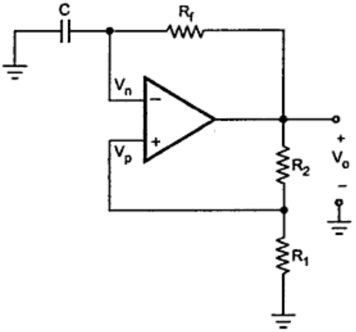


Fig. 9.56 Astable multivibrator using op-amp

As shown in the Fig. 9.56 the comparator and positive feedback resistors R_1 and R_2 form an inverting Schmitt trigger.

When V_o is at $+V_{sat}$, the feedback voltage is called the upper threshold voltage V_{UT} and is given as

$$V_{UT} = \frac{R_1 \cdot (+V_{sat})}{R_1 + R_2} \qquad \dots (1)$$

When V_o is at $-V_{sat}$, the feedback voltage is called the lower-threshold voltage V_{LT} and is given as

$$V_{LT} = \frac{R_1 \cdot (-V_{sat})}{R_1 + R_2} \qquad \dots (2)$$

When power is turn ON, V_o automatically swings either to $+V_{sat}$ or to $-V_{sat}$ since these are the only stable states allowed by the Schmitt trigger. Assume it swings to $+V_{sat}$. With

$V_o = +V_{sat}$ we have $V_P = V_{UT}$ and capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f to the inverting (–) input. This is illustrated in Fig. 9.57 (a). As long as the capacitor voltage V_C is less than V_{UT}, the output voltage remains at $+V_{sat}$.

As soon as V_C charges to a value slightly greater than V_{UT}, the (–) input goes positive with respect to the (+) input. This switches the output voltage from $+V_{sat}$ to $-V_{sat}$ and we have $V_P = V_{LT}$, which is negative with respect to ground. As V_o switches to $-V_{sat}$, capacitor starts discharging via R_f, as shown in the Fig. 9.57 (b).

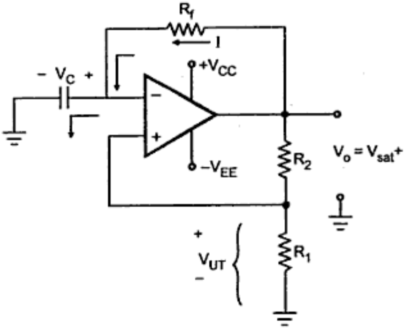


Fig. 9.57 (a) When $V_o = +V_{sat}$, capacitor charges towards V_{UT}

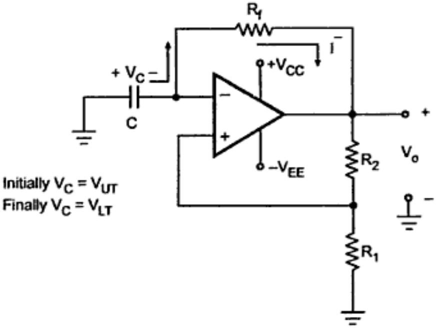


Fig. 9.57 (b) When $V_o = -V_{sat}$, capacitor charges towards V_{LT}

The current I^- discharges capacitor to 0 V and recharges capacitor to V_{LT}. When V_C becomes slightly more negative than the feedback voltage V_{LT}, output voltage V_o switches back to $+V_{sat}$. As a result, the condition in Fig. 9.57 (a) is reestablished except that capacitor now has a initial charge equal to V_{LT}. The capacitor will discharge from V_{LT} to 0 V and then recharge to V_{UT}, and the process is repeating. Once the initial cycle is completed, the waveforms become periodic, as shown in the Fig. 9.57(c).

$$\therefore \qquad T_1 = -R_f\ C\ ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$= R_f\ C\ ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right) \qquad \text{... (5)}$$

The time taken by capacitor to charge from V_{UT} to V_{LT} is same as time required for charging capacitor from V_{LT} to V_{UT}. Therefore, total time required for one oscillation is given as

$$T = 2T_1 \qquad \text{... (6)}$$

$$\therefore \qquad \boxed{T = 2R_f\ C\ ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)} \qquad \text{... (7)}$$

The frequency of oscillation can be determined as $f_o = 1/T$, where T represents the time required for one oscillation.

Substituting the value of T we get,

$$\boxed{f_o = \frac{1}{2\,R_f\ C\ ln\left(\dfrac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)}} \qquad \text{... (8)}$$

Substituting the values of V_{UT} and V_{LT} we get,

$$T = 2\,R_f\ C\ ln\left[\frac{+V_{sat} - (R_1 \times - V_{sat})/R_1 + R_2}{+V_{sat} - (R_1 \times + V_{sat})/R_1 + R_2}\right]$$

If magnitudes of + V_{sat} and – V_{sat} are equal,

$$T = 2\,R_f\ C\ ln\left[\frac{+V_{sat}\left(1 + \dfrac{R_1}{R_1 + R_2}\right)}{+V_{sat}\left(1 - \dfrac{R_1}{R_1 + R_2}\right)}\right]$$

$$\therefore \qquad \boxed{T = 2\,R_f\ C\ ln\left(\frac{2R_1 + R_2}{R_2}\right)}$$

9.22.2 Non-symmetrical Square Wave Generation

The astable multivibrator can be used to obtain non-symmetrical square wave by modifying the circuit as shown in the Fig. 9.58.

➠ **Example 9.13 :** *For the circuit shown in Fig. 9.66 if $R_2 = 100\ k\Omega$, $R_1 = 86\ k\Omega$, $+V_{sat} = 15\ V$, $-V_{sat} = -15\ V$, $R_f = 100\ k\Omega$ and $C = 0.1\ \mu F$, find*

a) V_{UT} b) V_{LT} and c) frequency of oscillation

Solution : a) We know that,

$$V_{UT} = \frac{R_1 \times +V_{sat}}{R_1 + R_2} = \frac{86\ K \times 15}{86\ K + 100\ K} = \mathbf{6.94\ V}$$

b) We know that,

$$V_{LT} = \frac{R_1 \times -V_{sat}}{R_1 + R_2} = \frac{86\ K \times (-15)}{86\ K + 100\ K} = \mathbf{-6.94\ V}$$

c) We know that,

$$f_o = \frac{1}{2 R_f\ C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)} = \frac{1}{2 \times 100\ k \times 0.1\ \mu F \times ln\left(\frac{15-(-6.94)}{15-(6.94)}\right)}$$

$$= \frac{1}{0.02} = \mathbf{50\ Hz}$$

➠ **Example 9.14 :** *For circuit shown in Fig. 9.56 show that $T = 2R_fC$ when $R_1 = 0.86\ R_2$.*

Solution : We know that,

$$T = 2\ R_f\ C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)$$

Substituting the values of V_{UT} and V_{LT} we get,

$$T = 2R_f\ C\, ln\left(\frac{+V_{sat} - (R_1 \times -V_{sat}) / (R_1 + R_2)}{+V_{sat} - (R_1 \times +V_{sat}) / (R_1 + R_2)}\right)$$

If the magnitudes of $+V_{sat}$ and $-V_{sat}$ are equal, the term in parentheses simplifies to

$$T = 2\ R_f\ C\, ln\left(\frac{+V_{sat}\left(1 + \frac{R_1}{R_1 + R_2}\right)}{+V_{sat}\left(1 - \frac{R_1}{R_1 + R_2}\right)}\right)$$

$$= 2\ R_f\ C\, ln\left(\frac{\frac{2R_1 + R_2}{R_1 + R_2}}{\frac{R_2}{R_1 + R_2}}\right) = 2\ R_f\ C\, ln\left(\frac{2R_1 + R_2}{R_2}\right)$$

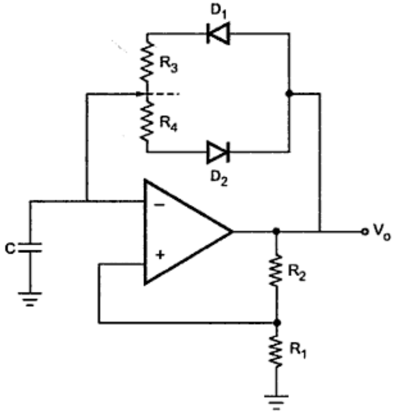


Fig. 9.61

And $V_o = \pm V_{sat} = \pm 15$ V. When $V_o = +V_{sat} = +15$ V then C will charge through R_3 due to forward biased diode D_1.

And when $V_o = -V_{sat} = -15\,V$. C will discharge through R_4 due to forward biased diode D_2. Selecting different combinations of R_3 and R_4, charging and discharging time can be varied and non-symmetrical square wave can be obtained.

Now

$$V_{UT} = \frac{R_1(+V_{sat})}{R_1+R_2}$$

$$= 0.5\times 15 = 7.5\ V$$

$$V_{LT} = \frac{R_1(-V_{sat})}{R_1+R_2}$$

$$= 0.5\times -15 = -7.5\ V$$

Choose $C = 0.1\ \mu F$

The charging equation is,

$$V_{UT} = +V_{sat} + (V_{LT} - V_{sat})\, e^{-T_{ON}/R_3C}$$

$$\therefore \quad 7.5 = 15 + (-7.5 - 15)\, e^{-T_{ON}/R_3C}$$

$$\therefore \qquad -\frac{T_{ON}}{R_3 C} = \ln(0.333)$$

Now assume 50 % duty cycle and design hence $R_3 = R_4$ and,

$$T_{ON} = \frac{1}{2}T = \frac{1}{2}\times\frac{1}{f}$$

$$= \frac{1}{2}\times\frac{1}{2.5\times10^3} = 2\times10^{-4} \text{ sec}$$

$$\therefore \qquad R_3 = \frac{-2\times10^{-4}}{0.1\times10^{-6}\times\ln(0.333)}$$

$$= \mathbf{1.8203\ k\Omega}$$

$$\therefore \qquad R_4 = \mathbf{1.8203\ k\Omega}$$

Now to vary the duty cycle from 30% to 70% divide $R_3 + R_4$ in the ratio 3 : 4 : 3 as shown in the Fig. 9.62. The modified circuit will give f = 2.5 kHz with variable duty cycle from 30 % to 70 %.

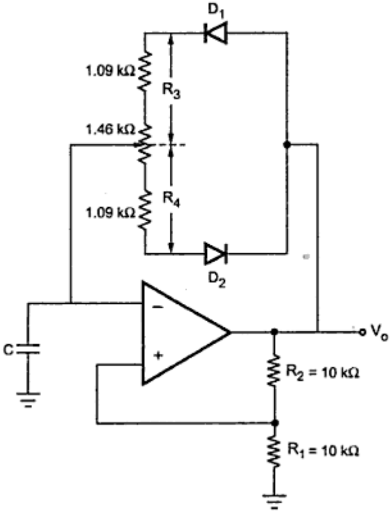


Fig. 9.62

Example 9.17 : *Design an op-amp circuit to generate a pulse waveform of frequency 2 kHz.*

Solution : The monostable multivibrator using op-amp produces the pulse waveform. The pulse width is given by,

$$T = RC\, ln\left[\frac{1+V_{D1}/V_{sat}}{1-\beta}\right]$$

where $V_{D1} = 0.7\ V,\ V_{sat} = \pm 12\ V$ for op-amp 741

$$\beta = \frac{R_2}{R_1+R_2} = 0.5 \text{ with } R_1 = R_2$$

$$T = \frac{1}{f} = \frac{1}{2\times 10^3} = 5\times 10^{-4} \text{ sec}$$

Choose $C = \mathbf{0.1\ \mu F}$

$\therefore$ $$5\times 10^{-4} = R\times 0.1\times 10^{-6}\, ln\left[\frac{1+(0.7/12)}{1-0.5}\right]$$

$\therefore$ $$R = 6.66\ k\Omega \approx \mathbf{6.7\ k\Omega}$$

Choose $R_1 = R_2 = \mathbf{10\ k\Omega}$

The designed circuit is shown in the Fig. 9.63.

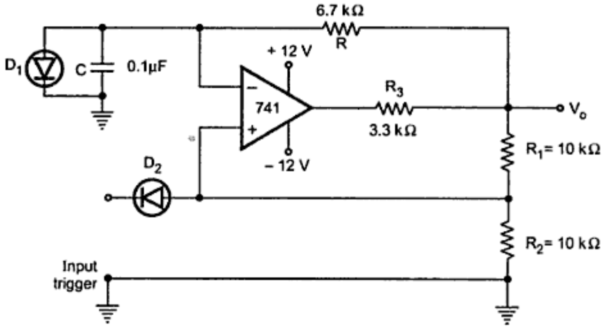


Fig. 9.63

9.23 Block Schematic of Timer

The Fig. 9.64 shows the block schematic of timer. It consists of three input signals, one output signal and three units : charging unit, comparator and output unit.

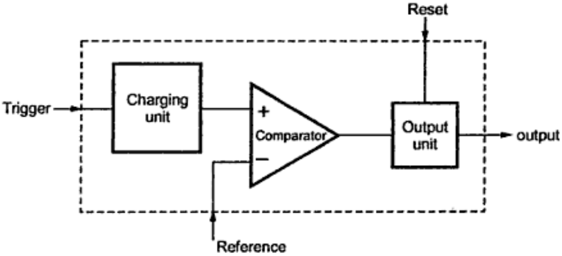

Reset
Trigger
Charging unit
+
Comparator
−
Output unit
output
Reference

Fig. 9.64 Block schematic of timer

The charging unit consists of RC circuit as shown in the Fig. 9.65. It is associated with trigger input. The trigger input is activated by pressing switch (push to ON). Pressing this switch momentarily, the capacitor can be discharged completely so that voltage across capacitor can be made zero volt. Immediately after the switch is released capacitor starts charging through resistance R, with time constant RC. The voltage across capacitor is applied to the +ve input of the comparator. The comparator compares this voltage with reference voltage applied at the reference input.

When the voltage across capacitor is greater than reference voltage; output is low; otherwise output is high. Immediately after trigger, output jumps to its high level and remains high until capacitor charges above level of reference voltage, as shown in the Fig. 9.66.

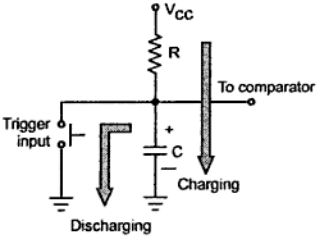

V_{CC}
R
To comparator
Trigger input
+
C
−
Charging
Discharging

Fig. 9.65 Charging Unit

9.24.2 Basic Timing Circuit

The Fig. 9.69 shows the basic timing circuit, which uses R-S flip-flop along with some other elements.

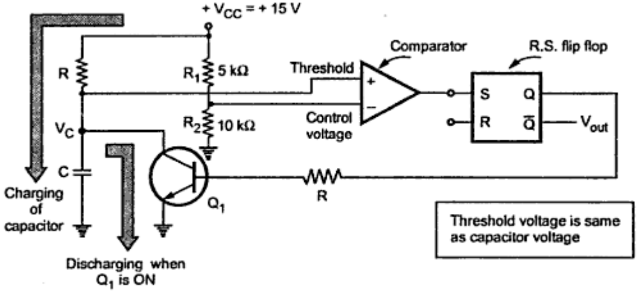

+ V_CC = + 15 V
Comparator
R.S. flip flop
R
R1 5 kΩ
Threshold
+
−
S
Q
R
Q̄
V_out
V_C
R2 10 kΩ
Control voltage
C
Charging of capacitor
Q1
R
Threshold voltage is same as capacitor voltage
Discharging when Q1 is ON

Fig. 9.69 Basic timing circuit

To understand the operation, consider that the output Q is high. This drives the base of Q_1 and as it is high it drives Q_1 into saturation. It makes the capacitor voltage zero and as other end of capacitor is grounded, the capacitor is shorted. In this condition it can not be charged.

The circuit uses a comparator. The noninverting input of comparator is called **threshold voltage.** While its inverting input is called **control voltage.** The R_1 and R_2 forms a potential divider which maintains control voltage constant at +10 V. As Q is high and transistor Q_1 is in saturation, the threshold voltage is zero.

As $R_1 = 5\ k\Omega$ and $R_2 = 10\ k\Omega$

$$\textbf{Control voltage} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{10}{5+10} \times 15 = \textbf{10 V constant}$$

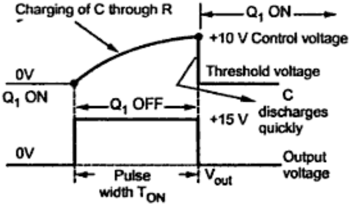


Fig. 9.70 Waveforms of basic timing circuit

Now if high voltage is applied to the reset (R) input of flip-flop then it resets R-S flip-flop and output Q goes low. This drives the transistor Q_1 in cut-off. Now the capacitor is free to charge and starts charging through resistance R. The threshold voltage thus starts increasing. When it becomes just greater than +10 V which is the control voltage, the comparator output goes high. This high signal is driving the set (S) input of R-S flip flop. This changes the state of output Q back to high. This drives transistor Q_1 into saturation which quickly discharges the capacitor C.

The Fig. 9.70 shows the waveforms of threshold voltage and output voltage V_{out}. The charging of capacitor is exponential hence the threshold voltage is also exponential in nature. When Q goes low, the $\bar{Q}$ becomes high and positive going pulse appears at V_{out}. Similarly when capacitor voltages increases more than the control voltage, Q becomes high and $\bar{Q}$ becomes low. This brings V_{out} to zero instantly. Thus a rectangular output gets produced.

It can be observed that output remains high for the time which is required by the capacitor to charge upto control voltage, through R. Thus by varying R or C, the output pulse width can be varied. This is the working principle of timer IC 555.

9.25 Block Diagram of IC 555

The Fig. 9.71 (a) and (b) show the pin diagram and the block diagram of the IC NE 555 timer. This is 8 pin IC timer.

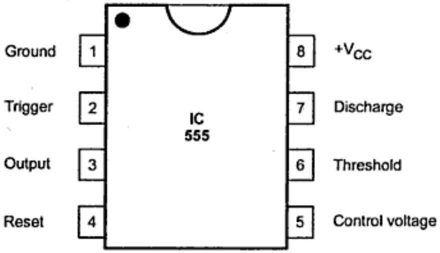


Fig. 9.71 (a) Pin diagram

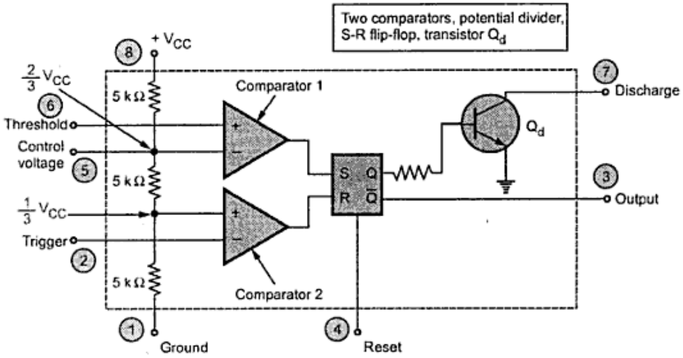

Two comparators, potential divider, S-R flip-flop, transistor Q_d
8
$+V_{CC}$
$\frac{2}{3}V_{CC}$
6
Threshold
Control voltage
5
$\frac{1}{3}V_{CC}$
Trigger
2
5 kΩ
5 kΩ
5 kΩ
Comparator 1
Comparator 2
S
Q
R
$\bar{Q}$
Q_d
7
Discharge
3
Output
1
Ground
4
Reset

Fig. 9.71 (b) Block diagram of IC 555 timer

9.25.1 Functions of Pins

The pin numbers of IC 555 and their functions are discussed below :

Pin 1 : Ground

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger

The IC 555 uses two comparators. The voltage divider consists of three equal resistances. Due to voltage divider, the voltage of noninverting terminal of comparator 2 is fixed at V_{CC} / 3. The inverting input of comparator 2 which is compared with $V_{CC}/3$, is nothing but trigger input brought out as pin number 2. When the trigger input is slightly less than V_{CC} /3 the comparator 2 output goes high. This output is given to reset input of R-S flip-flop. So high output of comparator 2 resets the flip-flop.

Pin 3 : Output

The complementary signal output ($\bar{Q}$) of the flip-flop goes to pin 3 which is the output. The load can be connected in two ways. One between pin 3 and ground while other between pin 3 and pin 8.

Pin 4 : Reset

This is an interrupt to the timing device. When pin 4 is grounded, it stops the working of device and makes it off. Thus, pin 4 provides on/off feature to the IC 555. This reset input overrides all other functions within the timer when it is momentarily grounded.

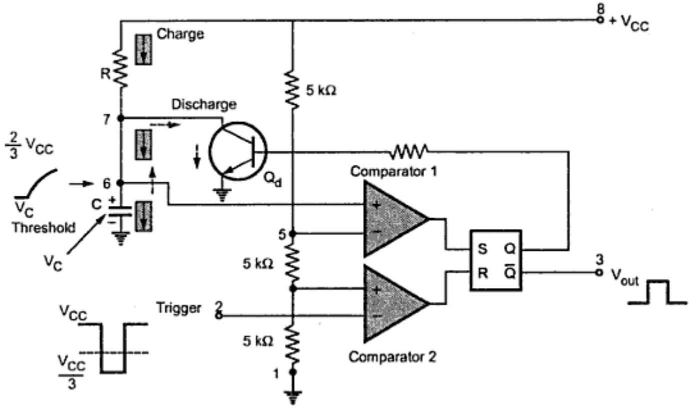


Fig. 9.72 Monostable operation of 555

The circuit has **only one stable state**. When trigger is applied, it produces a pulse at the output and returns back to its stable state. The duration of the pulse depends on the values of R and C. As it has only one stable state, it is called one shot multivibrator.

9.26.1 Operation

The flip-flop is initially set i.e. Q is high. This drives the transistor Q_d in saturation. The capacitor discharges completely and voltage across it is nearly zero. The output at pin 3 is low.

When a trigger input, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is greater than $1/3\ V_{CC}$. When it becomes less than $1/3\ V_{CC}$, then comparator 2 output goes high. This resets the flip-flop so Q goes low and $\overline{Q}$ goes high. Low Q makes the transistor Q_d off. Hence capacitor starts charging through resistance R, as shown by dark arrows in the Fig. 9.72.

The voltage across capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6. When this voltage becomes more than $2/3\ V_{CC}$, then comparator 1 output goes high. This sets the flip-flop i.e. Q becomes high and $\overline{Q}$ low. This high Q drives the transistor Q_d in saturation. Thus capacitor C quickly discharges through Q_d as shown by dotted arrows in the Fig. 9.73.

So it can be noted that V_{out} at pin 3 is low at start, when trigger is less than $1/3\ V_{CC}$ it becomes high and when threshold is greater than $2/3\ V_{CC}$ again becomes low, till next trigger pulse occurs. So a rectangular wave is produced at the output. The pulse width of this rectangular pulse is controlled by the charging time of capacitor. This depends on the time constant RC. **Thus RC controls the pulse width.** The waveforms are shown in the Fig. 9.73.

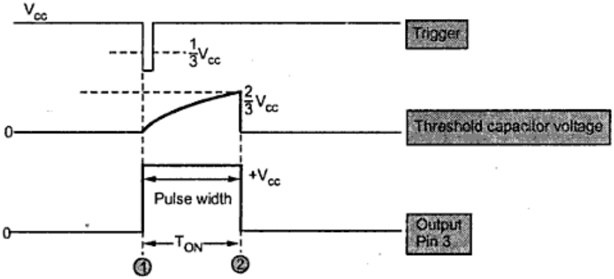

V_{cc}
$\frac{1}{3}V_{cc}$
Trigger
$\frac{2}{3}V_{cc}$
0
Threshold capacitor voltage
$+V_{cc}$
Pulse width
0
Output Pin 3
T_{ON}
①
②

Fig. 9.73 Waveforms of monostable operation

9.26.2 Derivation of Pulse Width

The voltage across capacitor increases exponentially and is given by

$$V_C = V(1 - e^{-t/CR})$$

If $$V_C = 2/3\ V_{CC}$$

then $$\frac{2}{3} V_{CC} = V_{CC}(1 - e^{-t/CR})$$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$\therefore$ $$-\frac{t}{CR} = -1.0986$$

$\therefore$ $$t = +1.0986\ CR$$

$\therefore$ $$t \approx 1.1\ CR$$

where C in farads, R in ohms, t in seconds.

Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e. 1.1 RC

Thus the pulse width denoted as W is given by,

$$\boxed{W = 1.1\ RC}$$

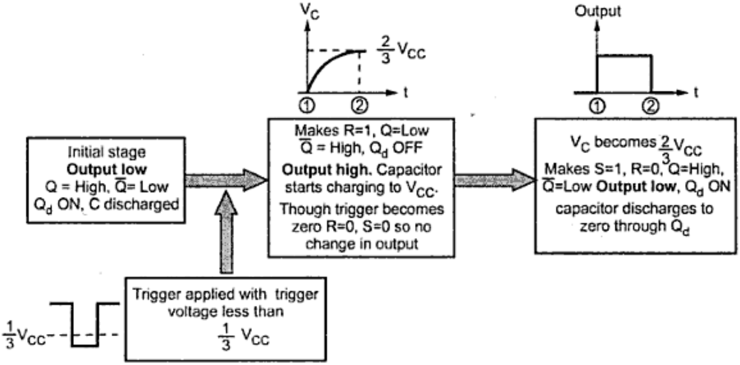

V_C
$\frac{2}{3} V_{CC}$
t
① ②
Output
t
① ②
Initial stage
Output low
Q = High, $\overline{Q}$= Low
Q_d ON, C discharged
Makes R=1, Q=Low
$\overline{Q}$ = High, Q_d OFF
Output high. Capacitor starts charging to V_{CC}.
Though trigger becomes zero R=0, S=0 so no change in output
V_C becomes $\frac{2}{3} V_{CC}$
Makes S=1, R=0, Q=High,
$\overline{Q}$=Low Output low, Q_d ON
capacitor discharges to zero through Q_d
Trigger applied with trigger voltage less than $\frac{1}{3} V_{CC}$
$\frac{1}{3} V_{CC}$

Fig. 9.74 Summary of monostable operation

9.26.3 Schematic Diagram

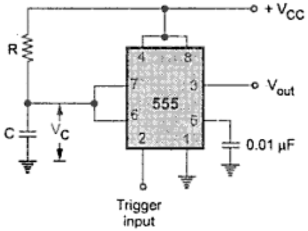

+ V_{CC}
R
4
8
7
3
V_{out}
555
6
5
C
V_C
2
1
0.01 µF
Trigger input

Fig. 9.75 555 timer as monostable multivibrator

Generally a schematic diagram of the IC 555 circuits is shown which does not include comparators, flip-flop etc. It only shows the external components to be connected to the 8 pins of IC 555. Thus, the schematic diagram of IC 555 as a monostable multivibrator is shown in the Fig. 9.75.

The external components R and C are shown. To avoid accidental reset, pin 4 is connected to pin 8 which is supply $+V_{CC}$. To have the noise filtering of control voltage, the pin 5 is grounded through a small capacitor of 0.01 µF.

9.26.4 Applications of Monostable Multivibrator

9.26.4.1 Frequency Divider

We know that, in monostable multivibrator, application of trigger pulse gives a positive going pulse on the output. The same monostable circuit can be used as a frequency divider if the timing interval is adjusted to be longer than the period of the input signal, as shown in the Fig. 9.76.

The Fig. 9.76 shows monostable multivibrator as a divider-by-2 circuit. Here, timing interval 't' is kept slightly larger than the time period T of the trigger input signal.

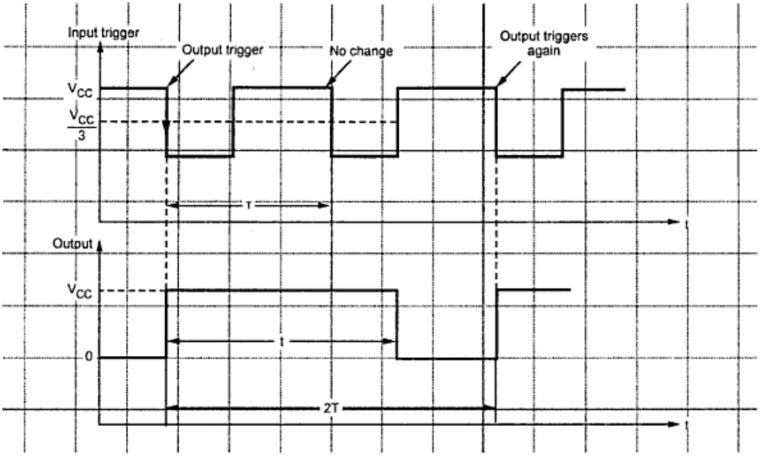


Fig. 9.76 Input and output waveforms of the monostable multivibrator as a divide-by-2 circuit

The monostable multivibrator will be triggered by the first negative going edge of the trigger input, which will make output to go in its high state. The output will remain high for the period equal to 'timing interval'. As timing interval is greater than time period of the trigger input, output will still be high when the second negative going pulse occurs. The monostable will, however, be re-triggered on the third negative-going pulse. Therefore, monostable triggers on every other pulse of the trigger input, so there is only one output for every two input pulses, thus trigger signal is, divided by 2. In this way, by adjusting the timing interval, the monostable circuit can be made integral fractions of the frequency of the input trigger signal.

9.26.4.2 Pulse Width Modulation

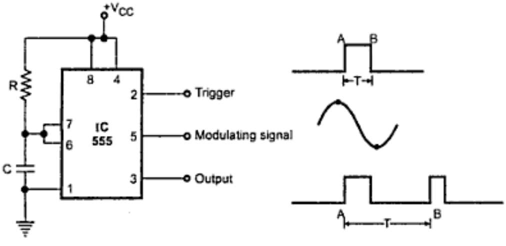


Fig. 9.77 Pulse width modulator

The Fig. 9.77 shows pulse width modulator. It is basically a monostable multivibrator with a modulating input signal applied at the control voltage input (pin 5). Internally, the control voltage is adjusted to the 2/3 V_{CC}. Externally applied modulating signal changes the control voltage, and hence the threshold voltage level of the upper comparator (comparator 1). As a result, time period required to charge the capacitor upto threshold voltage level changes, giving pulse width modulated signal at the output as shown in the Fig. 9.77 (a).

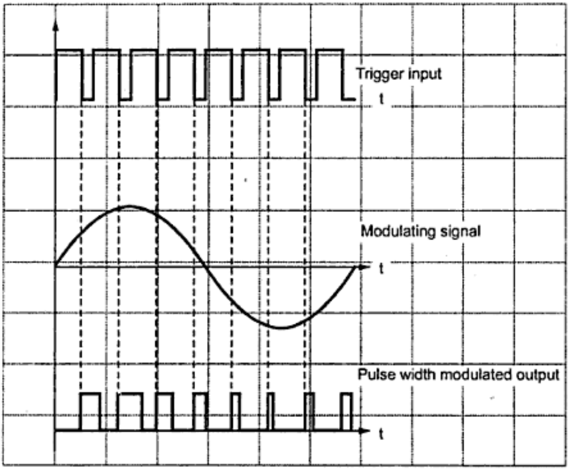


Fig. 9.77 (a) Pulse width modulator waveforms

It may be noted from the output waveform that the pulse duration varies according to the modulating signal level, but the frequency of the output pulses is same as that of the trigger input signal.

The width of the output pulse is given by,

$$\boxed{W = -RC\, ln\left(1-\frac{UTP}{V_{CC}}\right)} \quad \text{... (1)}$$

Due to modulating signal, the upper threshold level is,

$$\boxed{UTP = \frac{2\,V_{CC}}{3} + v_{mod}} \quad \text{... (2)}$$

The time period of output is same as that of the trigger input clock.

$$\therefore \quad \boxed{T = \frac{1}{f_{clock}}} \quad \text{... (3)}$$

While the duty cycle is given by,

$$\boxed{D = \frac{W}{T}} \qquad \text{... (4)}$$

Example 9.18 : *Design a monostable for a pulse width of 10 ms by using IC 555.*

Solution : The required pulse width is,

$$W = 10 \text{ ms}$$

The pulse width is given by,

$$W = 1.1\ RC$$

$$\therefore \quad 10 \times 10^{-3} = 1.1\ RC$$

$$\therefore \quad RC = 9.0909 \times 10^{-3}$$

$$\text{Choose} \quad C = \mathbf{0.1\ \mu F}$$

$$\therefore \quad R = 90.909\ k\Omega \approx \mathbf{91\ k\Omega}$$

The designed circuit is shown in the Fig. 9.78.

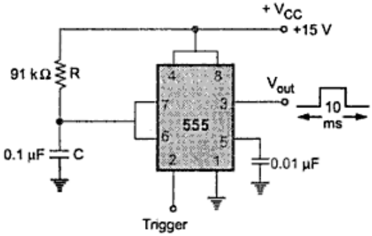


Fig. 9.78

Example 9.19 : *Design a timer, which should turn ON heater immediately after pressing a push button and should hold heater in 'ON-state' for 5 seconds.*

Solution : Fig. 9.79 shows monostable circuit used to drive the relay.

This relay should be energized for 5 seconds to hold heater 'ON' for 5 seconds. Thus, T_{ON} for monostable is 5 seconds.

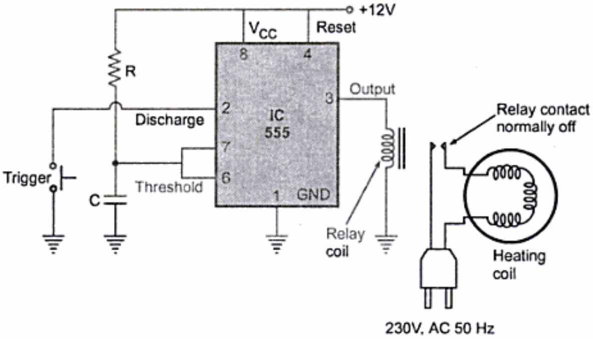

+12V
VCC
Reset
8
4
R
Output
3
2
Discharge
IC
555
Relay contact
normally off
7
Trigger
6
Threshold
C
1
GND
Relay
coil
Heating
coil
230V, AC 50 Hz

Fig. 9.79 Monostable multivibrator used to switch 'ON' relay for specific time

We know that the pulse width is given by,

$$W = 1.1\ RC$$

$$\therefore \quad 5 = 1.1\ RC$$

Now, there are two unknowns. In this case, we have to select value for capacitor and with the selected value we have to find the value of resistance from the formula.

∴ If capacitor value is **10 μF**

$$\text{then} \quad 5 = 1.1 \times R \times 10\ \mu F$$

$$\therefore \quad R = \frac{5}{1.1 \times 10 \mu\ F}$$

$$= 454545.45\ \Omega = \mathbf{454.54\ k\Omega}$$

The calculated value is not standard value, but we can adjust this value by connecting variable resistance i.e. potentiometer.

Example 9.20 : *Draw the circuit diagram of Timer using IC 555. Calculate the component values if the controlled door should remain open for 15 secs after a trigger signal is received. The dc voltage available is either 10 or 15 volts.*

Solution : The requirement is that the door must be open for 15 sec after receiving a trigger signal and then gets shut down automatically. This requires IC 555 in a monostable mode with a pulse width of 15 sec.

$$\therefore \quad W = 15 \text{ sec.}$$

$$\text{Now} \quad W = 1.1\ RC$$

$$\therefore \quad 15 = 1.1\ RC$$

Choose $C = 100\ \mu F$

$\therefore$ $R = 136.363\ k\Omega$

The designed circuit is shown in the Fig. 9.80.

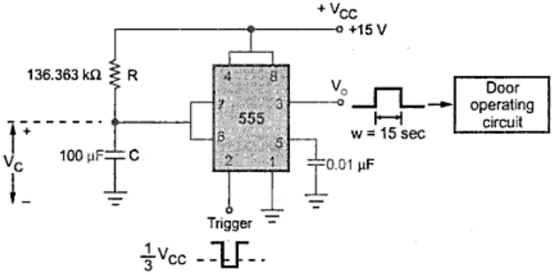

+ V_{CC}
+15 V
136.363 kΩ
R
4
8
7
3
555
6
5
2
1
V_o
w = 15 sec
Door operating circuit
+
V_C
–
100 μF
C
0.01 μF
Trigger
$\frac{1}{3}V_{CC}$

Fig. 9.80

The supply voltage 10 or 15 V has no effect on the operation of the circuit or the values of R and C selected.

9.26.4.3 Linear Ramp Generator

When a capacitor is charged with a constant current source then linear ramp is obtained. This concept is used in linear ramp generator. The circuit is shown in the Fig. 9.81.

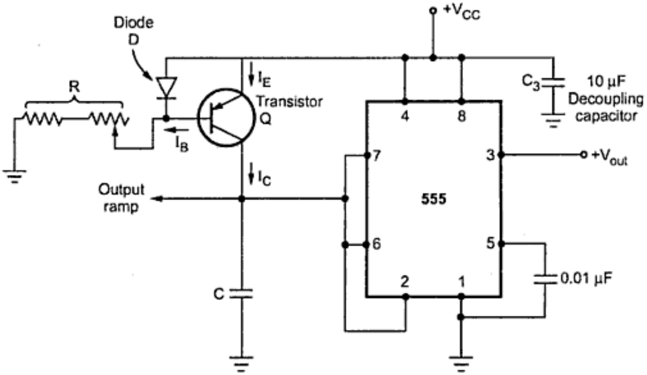

Diode
D
R
I_E
Transistor
Q
I_B
I_C
Output ramp
+V_{CC}
C_3
10 μF
Decoupling capacitor
4
8
7
3
+V_{out}
555
6
5
2
1
0.01 μF
C

Fig. 9.81 Linear ramp generator

The circuit is used to obtain constant current I_C is a current mirror circuit, using transistor Q and diode D. The current I_C, charges capacitor C at a constant rate towards $+V_{CC}$. But when voltage at pin 6 i.e. capacitor voltage V_C becomes $\left(2/3V_{CC}\right)$, the comparator makes internal transistor Q_1 ON within no time. But while discharging when V_C becomes $\left(1/3V_{CC}\right)$, the second comparator makes Q_1 OFF and C starts its charging again. As discharging time of capacitor C is very small, the time period of ramp is assumed practically same as that of charging time of capacitor.

The waveforms are shown in the Fig. 9.82.

The time period of the ramp is approximately given by,

$$T = \frac{V_{CC}\,C}{3I_C}\ \text{sec}$$

where $$I_C = \text{Charging current} = \frac{V_{CC}-V_D}{R} = \frac{V_{CC}-V_{BE}}{R}$$

Hence the frequency is given by,

$$\boxed{f = \frac{1}{T} = \frac{3I_C}{V_{CC}\,C}\ \text{Hz}}$$

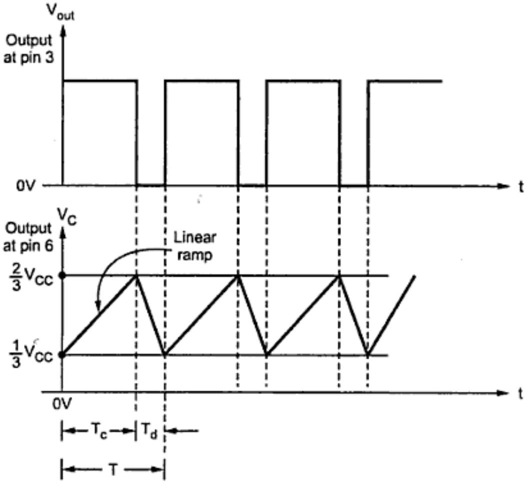


Fig. 9.82 Waveforms of ramp generator

9.26.4.4 Missing Pulse Detector

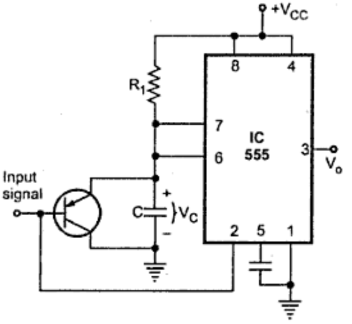


Fig. 9.83 (a) Missing pulse detector

The Fig. 9.83 (a) shows the circuit diagram for missing pulse detector. When signal input is at ground level (0V), the emitter diode of transistor T_1 forward biases and clamps capacitor voltage V_C to 0.7 V. This forces output voltage to stay in its high state. When signal input goes high, the transistor cuts off and capacitor C begins to charge. If input signal again goes low before the 555 completes its timing cycle, the voltage across C is reset to 0.7 V. If, however, input signal does not go low before the 555 completes its timing cycle, the 555 enters its normal state and output voltage goes low. This is illustrated in Fig. 9.83 (b).

For this circuit timing interval is adjusted such that it is slightly longer than the period of input signal. The continuous low going pulses of the period less than the timing interval do not allow capacitor to charge upto 2/3 V_{CC}. As a result, output voltage remains high. In case of missing pulse (pulse 4), capacitor charges upto 2/3 V_{CC} and forces output voltage in to its low state, as shown in the Fig. 9.83 (b). This type of circuit can be used to detect a missing heart beat.

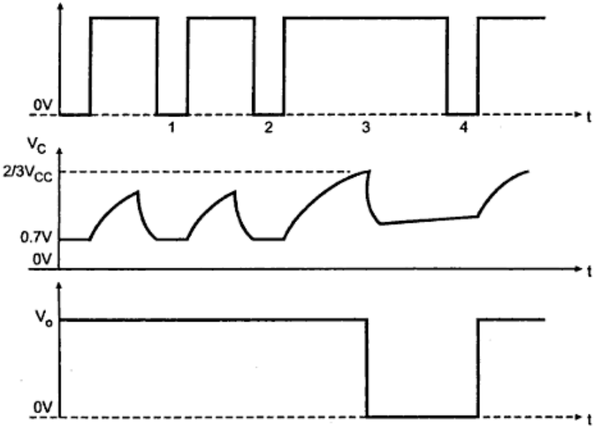


Fig. 9.83 (b) Waveforms for missing pulse detector

9.26.4.5 Pulse Position Modulation (PPM)

In pulse position modulation, the amplitude and width of the pulses are kept constant, while the position of each pulse with reference to the position of a reference pulse, is changed according to the instantaneous sampled value of the modulating signal.

The Fig. 9.84 (a) shows the pulse position modulator.

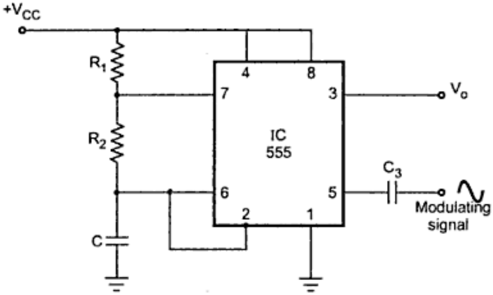

+V_{CC}
R_1
R_2
C
4
8
7
3
IC
555
6
5
2
1
V_o
C_3
Modulating signal

Fig. 9.84 (a) Pulse position modulator

With this type of circuit, the position of each pulse changes. Both width and period of pulses vary with the modulating signal. Due to modulating signal at pin 5, the UTP level changes to,

$$UTP = \frac{2\,V_{CC}}{3} + v_{mod} \qquad \text{... (5)}$$

when v_{mod} increases, the UTP level increases and hence pulse width also increases. If v_{mod} decreases, UTP level decreases and pulse width also decreases. Thus the pulse width varies as shown in the Fig. 9.84 (b).

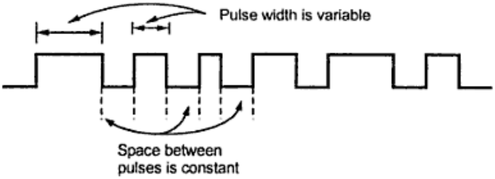

Pulse width is variable
Space between pulses is constant

Fig. 9.84 (b) Output of PPM

The pulse width is given by,

$$\boxed{W = -(R_1 + R_2)\,C\ln\left[\frac{V_{CC} - UTP}{V_{CC} - 0.5\,UTP}\right]} \qquad \text{... (6)}$$

The period is given by,

$$\boxed{T = W + 0.693 R_2 C} \quad \text{... (7)}$$

The space between the pulses which is constant is given by 0.693 R_2C.

The circuit is used in communication applications for transferring voice or data.

9.27 Astable Multivibrator using IC 555

The Fig. 9.85 shows the IC 555 connected as an astable multivibrator. The threshold input is connected to the trigger input. Two external resistances R_A, R_B and a capacitor C is used in the circuit.

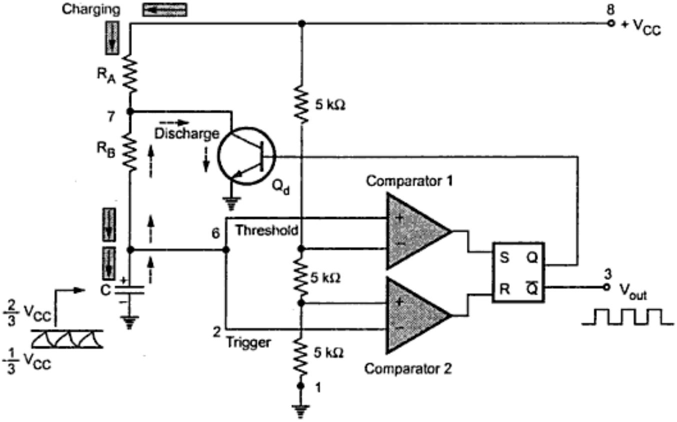


Fig. 9.85 Astable operation of 555

This circuit has no stable state. The circuits changes its state alternately. Hence the operation is also called free running nonsinusoidal oscillator.

9.27.1 Operation

When the flip-flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than 1/3 V_{CC}, comparator 2 output goes high. This resets the flip-flop hence Q goes low and $\overline{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and V_{CC}. The charging path is shown by thick arrows in the Fig. 9.85. As total resistance in the charging path is (R_A + R_B), the charging time constant is (R_A + R_B) C.

Now the capacitor voltage is also a threshold voltage. While charging, capacitor voltage increases i.e. the threshold voltage increases. When it exceeds 2/3 V_{CC}, then the comparator 1 output goes high which sets the flip-flop. The flip-flop output Q becomes high and output at pin 3 i.e. $\bar{Q}$ becomes low. High Q drives transistor Q_d in saturation and capacitor starts discharging through resistance R_B and transistor Q_d. This path is shown by dotted arrows in the Fig. 9.85. Thus the discharging time constant is R_B C. When capacitor voltage becomes less than 1/3 V_{CC}, comparator 2 output goes high, resetting the flip-flop. This cycle repeats.

Thus when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling. The waveforms are shown in the Fig. 9.86.

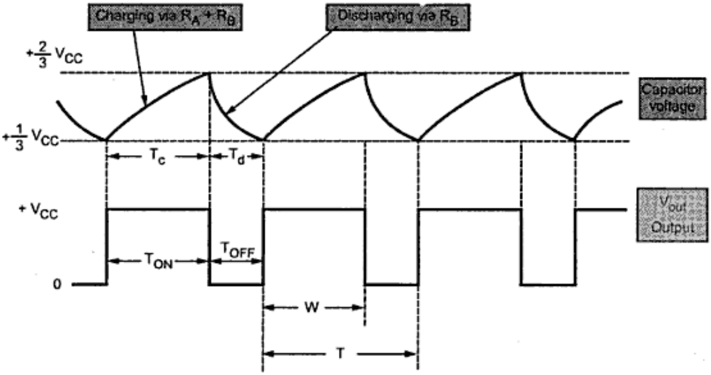


Fig. 9.86 Waveforms of astable operation

9.27.2 Duty Cycle

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveform is not symmetric. The high output remains for longer period than low output. The ratio of high output period and low output period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON time i.e. high output to the total time of one cycle. As shown in the Fig. 9.86.

$$W = \text{Time for output is high} = T_{ON}$$

$$T = \text{Time of one cycle}$$

$$\therefore \quad D = \text{Duty cycle} = \frac{W}{T}$$

$$\therefore \quad \boxed{\% D = \frac{W}{T} \times 100\ \%}$$

The charging time for the capacitor is given by,

$$T_c = \text{Charging time} = 0.693\ (R_A + R_B)\ C$$

While the discharge time is given by,

$$T_d = \text{Discharging time} = 0.693\ R_B\ C$$

Hence the time for one cycle is,

$$T = T_c + T_d = 0.693\ (R_A + R_B)\ C + 0.693\ R_B\ C$$

$$\therefore \quad \boxed{T = 0.693\ (R_A + 2\ R_B)\ C}$$

while $$W = T_c = 0.693\ (R_A + R_B)\ C$$

$$\therefore \quad \%D = \frac{W}{T} \times 100 = \frac{0.693\ (R_A + R_B)\ C}{0.693\ (R_A + 2\ R_B)\ C} \times 100$$

$$\therefore \quad \boxed{\% D = \frac{(R_A + R_B)}{(R_A + 2\ R_B)} \times 100}$$

While the frequency of oscillations is given by,

$$f = \frac{1}{T} = \frac{1}{0.693 (R_A + 2\ R_B) C}$$

$$\therefore \quad \boxed{f = \frac{1.44}{(R_A + 2\ R_B) C}\ \text{Hz}}$$

If R_A is much smaller than R_B, duty cycle approaches to 50% and output waveform approaches to square wave.

9.27.3 Schematic Diagram

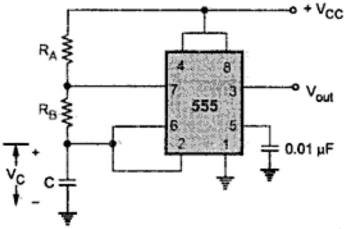


Fig. 9.87 555 timer as astable multivibrator

The Fig. 9.87 shows the schematic diagram of astable timer circuit. It shows only the external components R_A, R_B and C. The pin 4 is tied to pin 8 and pin 5 is grounded through a small capacitor.

The important application of astable multivibrator is voltage controlled oscillator (VCO).

Example 9.21 : *A 555 timer is configured to run in astable mode with $R_A = 4\ k\Omega$, $R_B = 4\ k\Omega$ and $C = 0.01\ \mu F$. Determine the frequency of the output and duty cycle.*

Solution : The frequency of output is given by,

$$f = \frac{1.44}{(R_A + 2\,R_B)C} = \frac{1.44}{(4+2\times4)\times10^3\times0.01\times10^{-6}}$$

$$= \textbf{12 kHz}$$

The duty cycle is given by,

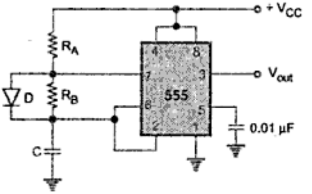
$$D = \frac{R_A + R_B}{R_A + 2\,R_B} = \frac{4+4}{4+(2\times4)} = 0.6667$$

Thus the duty cycle is **66.67 %.**

9.27.4 Applications of Astable Multivibrator

9.27.4.1 Square Wave Generator

It can be observed from the expression of duty cycle that in astable operation exact 50% duty cycle is not possible to achieve. To get exactly 50 % duty cycle i.e. square wave output it is necessary to modify the astable timer circuit.

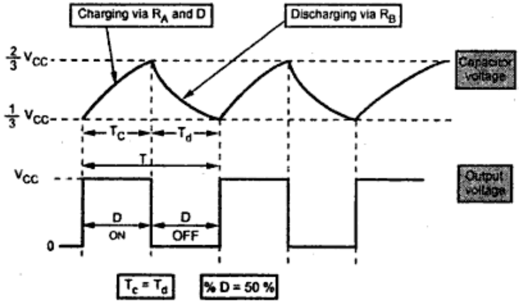


+ V_{CC}
R_A
R_B
D
C
555
4
8
7
3
6
5
2
1
V_{out}
0.01 μF

Fig. 9.88 Square wave generator

The modified astable circuit used to obtain the square wave output is shown in the Fig. 9.88.

In the modified circuit, the capacitor C charges through R_A and diode D and discharges through R_B. To obtain square wave (50 % duty cycle) resistance R_B is adjusted such that it is equal to the summation of resistance R_A and the forward resistance of diode D. Usually, potentiometer is used for exact adjustments of resistors.



Charging via R_A and D
Discharging via R_B
$\frac{2}{3}$ V_{CC}
$\frac{1}{3}$ V_{CC}
Capacitor voltage
T_c
T_d
T
V_{CC}
0
D ON
D OFF
Output voltage
$T_c = T_d$
% D = 50 %

Fig. 9.89 Waveforms of square wave generator

The waveforms of square wave generator are shown in the Fig. 9.89.

This relay should be energized for 3 seconds and then de-energize by 1 seconds. Hence charging time of capacitor is 3 seconds which is a pulse width W.

$$\therefore \quad W = 3 \text{ seconds}$$

While total time of one cycle is,

$$\therefore \quad T = 3 + 1 = 4 \text{ seconds}$$

$$\therefore \quad D = \frac{W}{T} = \frac{3}{4} = \text{Duty cycle}$$

$$= 0.75$$

But $$D = \frac{R_A + R_B}{R_A + 2\,R_B}$$

$$\therefore \quad 0.75 = \frac{R_A + R_B}{R_A + 2\,R_B}$$

$$\therefore \quad R_A + 2\,R_B = 1.33 R_A + 1.33\,R_B$$

$$\therefore \quad 0.667\,R_B = 0.333\,R_A$$

$$\therefore \quad R_A = 2\,R_B \qquad \ldots (1)$$

Now the charging time is given by,

$$T_c = 0.693\,(R_A + R_B)\,C$$

$$\therefore \quad 3 = 0.693\,(R_A + R_B)\,C$$

Choose $$C = 10\,\mu F$$

$$\therefore \quad R_A + R_B = \frac{3}{0.693 \times 10 \times 10^{-6}}$$

$$\therefore \quad R_A + R_B = 4.329 \times 10^5 \qquad \ldots (2)$$

Solving (1) and (2) we get,

$$R_A = \mathbf{288.6\ k\Omega}, \quad R_B = \mathbf{144.3\ k\Omega}$$

The values are not standard but can be adjusted using the potentiometers.

Example 9.23 : *Design a 555 based square wave generator to produce a symmetrical square wave of 1 kHz. If $V_{CC} = 12$ V, draw the voltage across timing capacitor and the output.* **(UPTU : 2004-05)**

Solution : The circuit used for the square wave generator is shown in the Fig. 9.94.

For square wave, charging and discharging resistors must be equal.

Using (1) and (3),

$$70 = \frac{4.32 \times 10^3 + R_2}{14400} \times 100$$

$$\therefore \qquad R_2 = 5.76 \text{ k}\Omega$$

Using (1) $\qquad R_3 = 4.32 \text{ k}\Omega$

Thus the various component values are,

C = 0.1 μF, $R_1 = R_3 =$ 4.32 kΩ, $R_2 =$ 5.76 kΩ.

9.28 555 Timer as a Schmitt Trigger

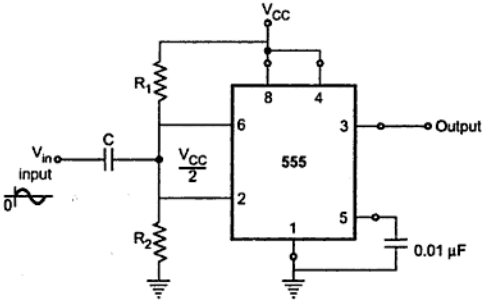


Fig. 9.97 555 as a schmitt trigger

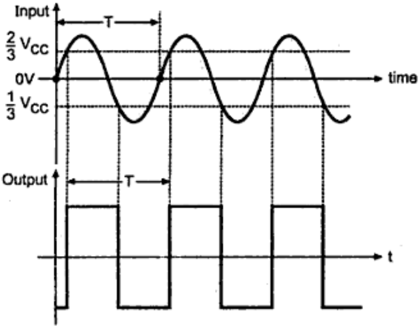


Fig. 9.98

The Fig. 9.97 shows the use of 555 timer as a schmitt trigger.

The input is given to the pins 2 and 6 which are tied together. Pins 4 and 8 are connected to supply voltage $+V_{CC}$. The common point of two pins 2 and 6 is externally biased at $V_{CC}/2$ through the resistance network R_1 and R_2. Generally $R_1 = R_2$ to get the biasing of $V_{CC}/2$. The upper comparator will trip at 2/3 V_{CC} while lower comparator at 1/3 V_{CC}. The bias provided by R_1 and R_2 is centred within these two thresholds.

Thus when sine wave of sufficient amplitude, greater than $V_{CC}/6$ is applied to the ciruit as input, it causes the internal flip-flop to alternately set and reset. Due to this, the circuit produces the square wave at the output, as shown in the Fig. 9.98.

Example 9.26 : *Draw the circuit diagram of an astable multivibrator to generate the output signal with frequency of 1 kHz and the duty cycle of 75%.*

Solution :

$$f = 1 \text{ kHz}$$

$$D = 75\ \% = 0.75$$

Now $$f = \frac{1.44}{(R_A + 2R_B)C} \text{ Hz}$$

$$\therefore \quad 1 \times 10^3 = \frac{1.44}{(R_A + 2R_B)C}$$

$$\therefore \quad (R_A + 2\,R_B)\,C = 1.44 \times 10^{-3} \quad \text{...(1)}$$

$$\therefore \text{ while} \quad \%\,D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

$$\therefore \quad 0.75 = \frac{R_A + R_B}{R_A + 2R_B}$$

$$\therefore \quad R_A + 2\,R_B = \frac{(R_A + R_B)}{0.75}$$

$$\therefore \quad R_A + 2\,R_B = 1.33\,(R_A + R_B)$$

$$\therefore \quad 0.66\,R_B = 0.33\,R_A$$

$$\therefore \quad R_B = 0.5\,R_A \quad \text{...(2)}$$

Choose $$C = 0.1\ \mu F$$

Substituting in (1),

$$(R_A + 2\,R_B) \times 0.1 \times 10^{-6} = 1.44 \times 10^{-3}$$

$$\therefore \quad R_A + 2\,R_B = 14400 \quad \text{...(3)}$$

Substituting (2) in (3),

$$R_A + 2\,(0.5\,R_A) = 14400$$

$$\therefore \quad R_A = \mathbf{7.2\ k\Omega}$$

$$\therefore \quad R_B = \mathbf{3.6\ k\Omega}$$

and $$C = 0.1\ \mu F$$

Hence the circuit diagram is as shown in the Fig. 9.100.

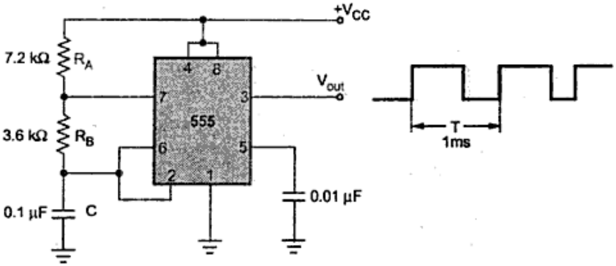


Fig. 9.100

Example 9.27 : *An astable multivibrator is to be designed for getting rectangular waveform with $t_{ON} = 0.6$ ms. Draw the circuit diagram with various component values. Also calculate frequency of oscillations and duty cycle. Assume total time period (T) to be 1 ms.*

Solution : $T_{ON} = 0.6$ ms, T = 1 ms

$$\therefore \quad D = \frac{t_{ON}}{T} = \frac{0.6}{1} = 60\%$$

$$\text{Now} \quad D = \frac{R_A + R_B}{R_A + 2R_B} = 0.6$$

$$\therefore \quad R_A + R_B = 0.6\,R_A + 1.2\,R_B$$

$$\therefore \quad 0.4\,R_A = 0.2\,R_B$$

$$\therefore \quad R_B = 2\,R_A \qquad \dots (1)$$

$$f = \frac{1.44}{(R_A + 2R_B)C} = \frac{1}{T} = 1000$$

Choose C = **0.1 μF**

$$\therefore \quad R_A + 2R_B = 14400$$

$$\text{Using (1),} \quad 5R_A = 14400$$

$$\therefore \quad R_A = \mathbf{2.88\ k\Omega}, \quad R_B = \mathbf{5.77\ k\Omega}$$

The circuit is shown in the Fig. 9.101.

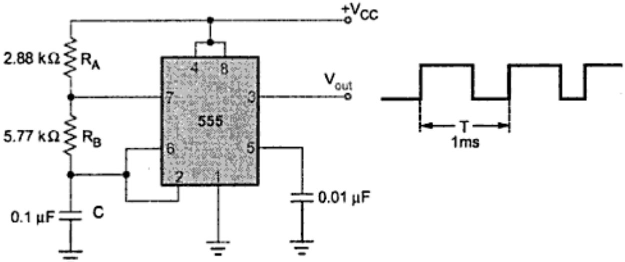


Fig. 9.101

Example 9.28 : *Draw the circuit diagram of IC 555 used as the astable mode to generate square wave of 1 kHz frequency, giving output equal to 5 V for* $\frac{1}{2}$ *msec and output equal to 0V for next* $\frac{1}{2}$ *msec. Connect one red lamp and one green lamp so that for* $\frac{1}{2}$ *msec red lamp is ON and green is OFF and for next* $\frac{1}{2}$ *msec green lamp is ON and red is OFF. Lamps have ratings of 5 V and 50 mA.*

Solution : $T_{ON} = T_{OFF} = 0.5 \text{ msec}$

$\therefore$ $T = T_{ON} + T_{OFF} = 1 \text{ msec}$

i.e. $f = \frac{1}{T} = 1 \text{ kHz}$

Now $T_d = T_{OFF} = 0.69 \, R_B C$

Choose $C = 0.1 \, \mu F$

$\therefore$ $0.5 \times 10^{-3} = 0.69 \, R_B \times 0.1 \times 10^{-6}$

$\therefore$ $R_B = 7.246 \text{ k}\Omega$

Now duty cycle is 50% so $R_A = R_B = 7.246 \text{ k}\Omega$

Practically a modified circuit is required for 50% duty cycle where diode is connected across R_B and charging takes place through R_A and diode. And R_B must be equal to sum of R_A and diode forward resistance. So to have perfect square wave, R_A is kept variable i.e. pot of say 10 kΩ, in this case. It is then adjusted to obtain precise square wave. The resistance required in series with LED to be connected is,

$$R = \frac{V_o - V_{LED}}{I_{LED}}$$

Assuming $V_{LED} = 0.7\ \text{V}$

Current limiting $R = \frac{5-0.7}{50\times10^{-3}} = 86\ \Omega \approx 100\ \Omega$

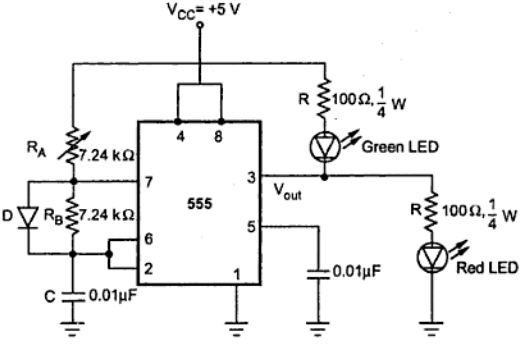
The wattage of R is

$$P = \left(50\times10^{-3}\right)^2 \times 100$$

$$= 0.25\ \text{W}$$

Both resitors R can be of $\frac{1}{4}$ W.

The required circuit is shown in the Fig. 9.102.



V_CC = +5 V
R
100 Ω, 1/4 W
Green LED
4
8
R_A
7.24 kΩ
7
3
V_out
555
D
R_B
7.24 kΩ
5
R
100 Ω, 1/4 W
6
2
1
0.01μF
Red LED
C
0.01μF

Fig. 9.102

Example 9.29 : *Design a ramp generator using 555 timer having output frequency of 5 kHz, with $V_{CC} = +5\,V$.*

Solution : $f = 5$ kHz, $V_{CC} = +5$ V

Assume $V_D = V_{BE} = 0.7$ V

$$\therefore \quad I_C = \frac{V_{CC}-V_D}{R} = \frac{V_{CC}-0.7}{R} = \frac{4.3}{R} \qquad \text{... (1)}$$

and $$f = \frac{3\,I_C}{V_{cc}\,C}$$

$$\therefore \quad 10\times10^{-3} = 1.1\,R\times0.22\times10^{-6}$$

$$\therefore \quad R = 41.4\ k\Omega$$

Now the output of timer is given as,

$$V_o = V_{CC} - 2V_{BE} - V_{CE\,sat}$$

Let $V_{CC} = 15$ V, $V_{BE} = 0.7$ V and $V_{CEsat} = 0.2$ V

$$\therefore \quad V_o = 15 - 2\times0.7 - 0.2$$

$$= 13.4\ V$$

Now the drop across LED is 1.4 V. There must be resistance in series with LED say R_{LED}. The LED current is 20 mA.

$$\therefore \quad R_{LED} = \frac{V_o - V_{LED}}{I_{LED}} = \frac{13.4-1.4}{20\times10^{-3}} = 600\ \Omega$$

To improve the noise immunity, connect a 0.01 μF capacitor between pin No.5 and ground. The designed circuit is shown in the Fig. 9.105.

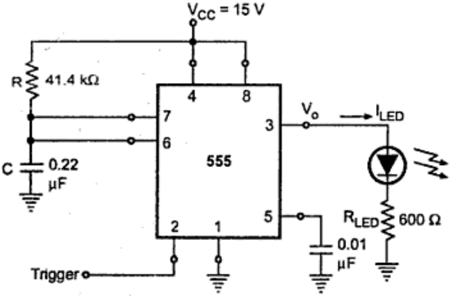


Fig. 9.105

The second circuit is an astable with frequency 1 kHz and 95% duty cycle.

$$\because \quad f = \frac{1.44}{(R_A+2R_B)C}$$

$$\therefore \quad 1\times10^{3} = \frac{1.44}{(R_A+2R_B)C}$$

Let $C = 0.01$ μF

$$\therefore \quad R_A + 2R_B = \frac{1.44}{1\times10^{3}\times0.01\times10^{-6}}$$

$$\therefore \quad R_A + 2R_B = 144 \times 10^3 \quad \text{... (1)}$$

$$\text{Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B}$$

$$\therefore \quad 0.95(R_A + 2R_B) = R_A + R_B$$

$$\therefore \quad 0.9\, R_B = 0.05\, R_A$$

$$\therefore \quad R_B = 0.0555\, R_A \quad \text{... (2)}$$

Substituting in (1),

$$R_A + 2 \times 0.0555 R_A = 144 \times 10^3$$

$$\therefore \quad R_A = \mathbf{129.6\ k\Omega}$$

$$\text{and} \quad R_B = \mathbf{7.19\ k\Omega}$$

The designed circuit is shown in the Fig. 9.106.

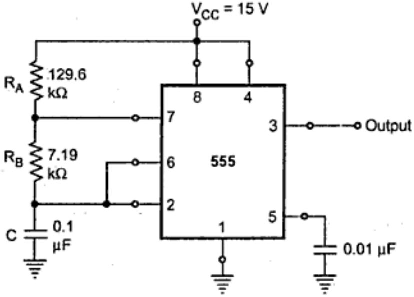

V_{CC} = 15 V
R_A
129.6 kΩ
R_B
7.19 kΩ
C
0.1 µF
8
4
7
3
Output
6
555
2
5
1
0.01 µF

Fig. 9.106

9.32 D/A Converters

A DAC (Digital to Analog Converter) accepts an n-bit input word $b_1, b_2, b_3, \ldots b_n$ in binary and produce an analog signal proportional to it. Fig. 9.107 shows circuit symbol and input-output characteristics of a 4-bit DAC. There are four digital inputs, indicating 4-bit DAC. Each digital input requires an electrical signal representing either a logic 1 or a logic 0. The b_n is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB.

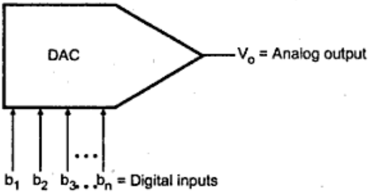

DAC
V_o = Analog output
b_1 b_2 b_3 . . b_n = Digital inputs

Fig. 9.107 (a) DAC circuit symbol

Fig. 9.107 (b) shows analog output voltage V_o is plotted against all 16 possible digital input words.

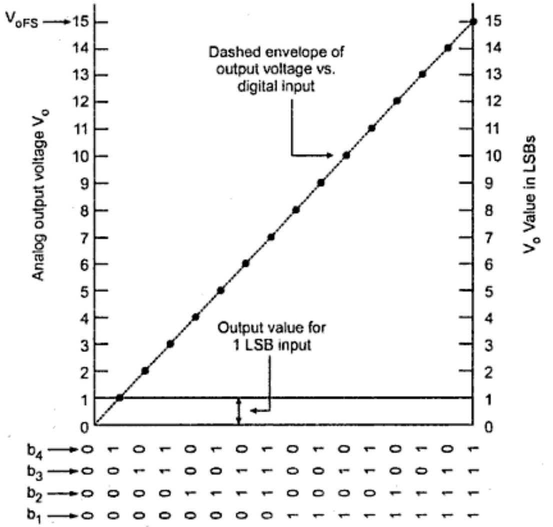


Fig. 9.107 (b)

9.33 Performance Parameters of DAC

The various performance parameters of DAC are,

Resolution

Resolution is defined in two ways.

- Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC

$$\text{Resolution} = 2^n \qquad \text{... (1)}$$

- Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} \qquad \text{... (2)}$$

where, V_{oFS} = Full scale output voltage

Settling Time

This is the time required for the output of the DAC to settle to within ± 1/2 LSB of the final value for a given digital input i.e. zero to full scale.

Stability

The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

Example 9.32 : *An 8 bit DAC has an output voltage range of 0 - 2.55 V. Define its resolution in two ways.*

Solution : For the given DAC,

$$n = \text{Number of bits} = 8$$

i) $$\text{Resolution} = 2^n = 2^8 = 256$$

i.e. the output voltage can have 256 different values including zero.

ii) $$V_{oFS} = \text{Full scale output voltage} = 2.55\text{ V}$$

$$\therefore \quad \text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{2.55}{2^8 - 1} = \frac{10\text{mV}}{1\text{ LSB}}$$

Thus an input change of 1 LSB causes the output to change by **10 mV.**

Example 9.33 : *The digital input for a 4-bit DAC is 0110. Calculate its final output voltage.*

Solution : For given DAC,

$$n = 4$$

$$\therefore \quad V_{oFS} = 15\text{ V}$$

$$\therefore \quad \text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{15}{2^4 - 1} = 1\text{ V/LSB}$$

$$\therefore \quad V_o = \text{Resolution} \times D$$

Now $$D = \text{Decimal of } (0110)_2 = 6$$

$$\therefore \quad V_o = 1\text{ V/LSB} \times 6 = \mathbf{6\text{ V}}$$

Example 9.34 : *An 8 bit DAC has resolution of 20 mV/LSB. Find* V_{oFS} *and* V_o *if the input is* $(10000000)_2$.

Solution : Resolution $= \dfrac{V_{oFS}}{2^n - 1}$

$\therefore$ $20 = \dfrac{V_{oFS}}{2^8 - 1}$

$\therefore$ $V_{oFS} = 5.1\ V$

$D =$ Equivalent of $(10000000) = 128$

$\therefore$ $V_o =$ Resolution $\times D = 20 \times 128 =$ **2.56 V**

Example 9.35 : *Find out stepsize and analog output for 4-bit R-2R ladder DAC when input is 1000 and 1111. Assume* $V_{ref} = +5V$.

Solution : For given DAC, $n = 4$, $V_{OFS} = +5\ V$

Resolution $= \dfrac{V_{oFS}}{2^n - 1} = \dfrac{5}{2^4 - 1} = \dfrac{1}{3}\ V/LSB$

$\therefore$ $V_o =$ Resolution $\times D$

For $D =$ Decimal of $(1000)_2 = 8$

$V_o = \dfrac{1}{3} \times 8 = 2.6667\ V$

For $D =$ Decimal of $(1111)_2 = 15$

$V_o = \dfrac{1}{3} \times 15 =$ **5 V.**

Example 9.36 : *A 12-bit DAC has a step size of 8 mV. Determine the full scale output voltage and percentage resolution. Also find the output voltage for the input of 010101101101?*

Solution : For 12-bit DAC, step size is 8 mV.

$V_{OFS} = 8\ mV \times 2^{12} - 1 = 32.76\ V$

% Resolution $= \dfrac{8\ mV}{32.76V} \times 100 = 0.02442$

The output voltage for the input 010101101101 is $= 8\ mV \times (1389)_{10} =$ **11.112 V**

9.34 Basic Conversion Techniques

There are mainly two techniques used for analog to digital conversion

- Binary weighted resistor D/A converter
- R/2R ladder D/A converter

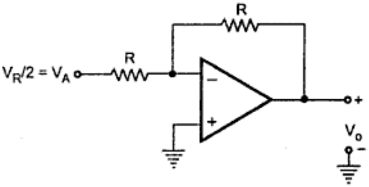


Fig. 9.113 (b)

Therefore, the output voltage is $V_R/2$, which is equivalent to binary input 100.

In general, the expression for V_o can be obtained as,

Let I_{out} = Output current

R_f = Feedback resistance of op-amp

$\therefore$ $V_o = -I_{out} R_f$

Now I_{out} = Current resolution × D

$\therefore$ V_o = – (Current resolution × D) R_f

$\therefore$ V_o = – (Current resolution × R_f) × D ... (8)

The coefficient of D is the voltage resolution and can be called as simple resolution.

$\therefore$ V_o = – Resolution × D ... (9)

In terms of actual circuit elements, output can be written as,

$$V_o = -\left(\frac{V_R}{R} \times \frac{1}{2^n} R_f\right) \times D \quad \text{...(10)}$$

The resolution of R/2R ladder type DAC with current output is,

$$\text{Resolution} = \frac{1}{2^n} \times \frac{V_R}{R} \quad \text{... (11)}$$

while the resolution fo R/2R ladder type DAC with voltage output is,

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f \quad \text{...(12)}$$

➠ **Example 9.37 :** *Suggest the values of resistors and reference voltage if resolution required is 0.5 V for 4 bit R/2R ladder type DAC.*

Solution : $\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f$

Let V_R = 10 V, n = 4 and resolution = 0.5

Example 9.38 : *An 8-bit ADC outputs all 1's when* $V_i = 5.1$ *V. Find its a) Resolution and b) Digital output when* $V_i = 1.28$ *V.*

Solution : a) From equation (1) we have,

$$\text{Resolution} = 2^8 = 256$$

and from equation (2) we have,

$$\text{Resolution} = \frac{5.1\,\text{V}}{2^8 - 1} = \mathbf{20\ mV/LSB}$$

Therefore, we can say that to change output by 1 LSB we have to change input by 20 mV.

b) For 1.28 V analog input, digital output can be calculated as,

$$D = \frac{1.28\,\text{V}}{20\,\text{mV} / \text{LSB}} = \mathbf{64\ LSBs}$$

The binary equivalent of 64 is $0100\ 0000_2$.

Example 9.39 : *Calculate the quantizing error for 12-bit ADC with full scale input voltage 4.095 V.*

Solution : From equation (3) we get

$$Q_E = \frac{4.095}{(2^{12} - 1) \times 2} = \frac{4.095}{(4096 - 1) \times 2} = \mathbf{0.5\ mV}$$

9.37 Basic Conversion Techniques

Analog to digital converter are classified into two general groups based on the conversion techniques. One technique involves comparing a given analog signal with the internally generated reference voltages. This group includes successive approximation, flash, delta modulated (DM), adaptive delta modulated and flash type converters. The another technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. This group includes integrator converters and voltage-to-frequency converters.

In this section we are going to discuss following types of ADCs using various conversion techniques :

1. Single ramp or single slope
2. Dual slope
3. Successive approximation
4. Flash
5. Delta modulation
6. Adaptive delta modulation

9.37.1 Single Slope ADC

It consists of a ramp generator and BCD or binary counters. The Fig. 9.119 shows the single slope ADC.

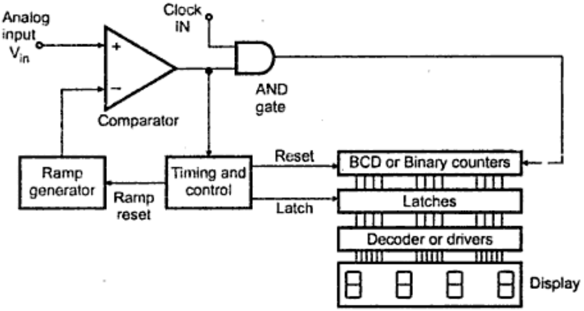


Fig. 9.119 Single slope ADC

At the start, the reset signal is provided to the ramp generator and the counters. Thus counters are resetted to 0's. The analog input voltage V_{in} is applied to the positive terminal of the comparator. As this is more positive than the negative input, the comparator output goes high. The output of ramp generator is applied to the negative terminal of the comparator. The high output of the comparator enables the AND gate which allows clock to reach to the counters and also this high output starts the ramp.

The ramp voltage goes positive until it exceeds the input voltage. When it exceeds V_{in}, comparator output goes low. This disables AND gate which inturn stops the clock to the counters. The control circuitry provides the latch signal which is used to latch the counter data. The reset signal resets the counters to 0's and also resets the ramp generator. The latched data is then displayed using decoder and a display device.

Let us consider the practical example to understand the working. Assume that the clock frequency is 1 MHz. There are four BCD counters and the input V_{in} is 2.000 V.

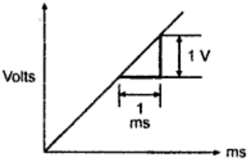


Fig. 9.120

Now let ramp has a slope of 1 V/ms as shown in the Fig. 9.120. As the input is 2.000 V, the ramp will take 2 ms to reach to 2 V and to stop the clock to the counters.

Now how many pulses will reach to the counters during 2 ms ? It can be calculated from the frequency of the clock. The number of pulses reaching to the counter in 2 ms is $\frac{2\text{ms}}{(1/1\text{MHz})}$ = 2000. The comparator output

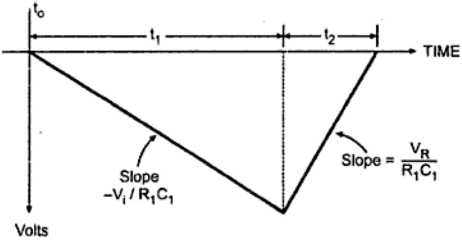


Fig. 9.122 Integrator output voltage

At time t = 0, analog switch S is connected to the analog input voltage V_i, so that the analog input voltage integration begins. The output voltage of the integrator can be given as,

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t V_i \, dt$$

$$= \frac{-V_i t}{R_1 C_1} \qquad \dots (1)$$

where $R_1 C_1$ is the integrator time constant and V_i is assumed constant over the integration time period. At the end of 2^N clock periods MSB of the counter goes high. At a result the output of the flip-flop goes high, which causes analog switch S to be switched from V_i to $-V_R$. At this very same time the binary counter which has gone through its entire count sequence is reset.

The negative input voltage ($-V_R$) connected to the input of integrator causes the integrator output to ramp positive. When integrator output reaches zero, the comparator output voltage goes low, which disables the clock AND gate. This stops the clock pulses reaching the counter, so that the counter will be stopped at a count corresponding to the number of clock pulses in time t_2.

The integrator output ramp down to a voltage V and get back upto 0. Therefore, the charge voltage is equal to discharge voltage and we can write,

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$\therefore \quad V_i t_1 = V_R t_2$$

$$\therefore \quad \boxed{t_2 = \frac{V_i t_1}{V_R}} \qquad \dots (2)$$

The above equation shows that t_2 is directly proportional only to the V_i, since V_R and t_1 are constants. The binary digital output of the counter gives corresponding digital value for time period t_2 and hence it is also directly proportional to input signal V_i.

The actual conversion of analog voltage V_{in} into a digital count occurs during t_2. The control circuit connects the clock to the counter at the beginning of t_2. The clock is disconnected at the end of t_2. Thus the counter contents is digital output. Hence we can write,

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{Second}}\right) t_2 \qquad \ldots(3)$$

But from equation (2) we can write,

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{Second}}\right) t_1 \left(\frac{V_i}{V_R}\right) \qquad \ldots(4)$$

The counter output can then be connected to an appropriate digital display.

The advantages of dual slope ADC are

1. It is highly accurate.
2. Its cost is low.
3. It is immune to temperature caused variations in R_1 and C_1.

The only disadvantage of this ADC is its speed which is low.

Example 9.40 : *For a particular dual slope ADC, t_1 is 83.33 ms and the reference voltage is 100 mV. Calculate t_2 if i) V_i is 100 mV and ii) 200 mV.*

Solution : We know that,

$$t_2 = \left(\frac{V_i}{V_R}\right) t_1$$

i)

$$t_2 = \left(\frac{100}{100}\right)(83.33)$$

$$= \mathbf{83.33\ ms}$$

ii)

$$V_i = 200\text{ mV}$$

$$\therefore \quad t_2 = \left(\frac{200}{100}\right)(83.33)$$

$$= \mathbf{166.6\ ms}$$

Example 9.41 : *Find the digital output of an ADC having t_1 as 83.33 ms and V_R as 100 mV for an input voltage of + 100 mV. The clock frequency is 12 kHz.*

Solution : The digital output is given as,

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{Second}}\right) t_1 \left(\frac{V_i}{V_R}\right)$$

Now $\quad$ Clock frequency $= 12$ kHz

$$\text{i.e.} \quad = 12000 \, \frac{\text{counts}}{\text{second}}$$

$$\therefore \quad \text{Digital output} = 12000 \times 83.33 \times \left(\frac{100}{100}\right) \times 10^{-3}$$

$$= \mathbf{1000\ counts.}$$

9.37.3 Successive Approximation ADC

In this technique, the basic idea is to adjust the DAC's input code such that its output is within ± $\frac{1}{2}$ LSB of the analog input V_i to be A/D converted. The code that achieves this represents the desired ADC output. It uses very efficient code searching strategy called binary search. It completes searching process for n-bit conversion in just n clock periods.

Fig. 9.123 shows the block diagram of successive approximation A/D converter. It consists of a DAC, a comparator, and a successive approximation register (SAR). The external clock input sets the internal timing parameters. The control signal start of conversion (SOC) initiates an A/D conversion process and end of conversion signal is activated when the conversion is completed.

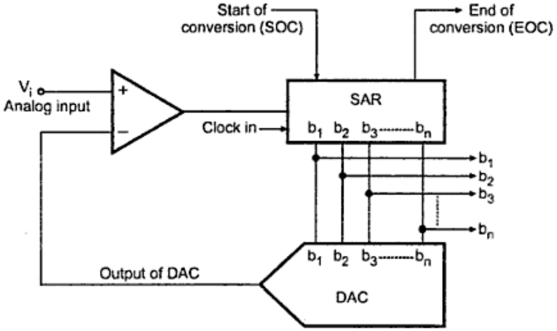

Start of conversion (SOC)
End of conversion (EOC)
V_i
Analog input
+
–
SAR
Clock in
b_1 b_2 b_3 ········ b_n
b_1
b_2
b_3
b_n
Output of DAC
b_1 b_2 b_3 ········ b_n
DAC

Fig. 9.123 Block diagram of successive approximation A/D converter

Operation :

The searching code process in successive approximation method is similar to weighing an unknown material with a balance scale and a set of standard weights. Let us assume that we have 1 kg, 2 kg and 4 kg weights (SAR) plus a balance scale (comparator and DAC). Now we will see the successive approximation analogy for 3-bit ADC.

Refer Fig. 9.123 and 9.124. The analog voltage V_{in} is applied at one input of comparator. On receiving start of conversion signal (SOC) successive approximation register sets 3-bit binary code 100_2 ($b_2 = 1$) as an input of DAC. This is similar process of placing the unknown weight on one platform of the balance and 4 kg weight on the other. The DAC converts the digital word 100 and applies it equivalent analog output at the second input of the comparator. The comparator then compares two voltages just like comparing unknown weight with 4 kg weight with the help of balance scale. If the input voltage is greater than the analog output of DAC, successive approximation register keeps $b_2 = 1$ and makes $b_1 = 1$ (addition of 2 kg weight to have total 6 kg weight) otherwise it resets $b_2 = 0$ and makes $b_1 = 1$ (replacing 2 kg weight). The same process is repeated for b_1 and b_0. The status of b_0, b_1 and b_2 bits gives the digital equivalent of the analog input.

Fig. 9.124 illustrates the process we have just discussed.

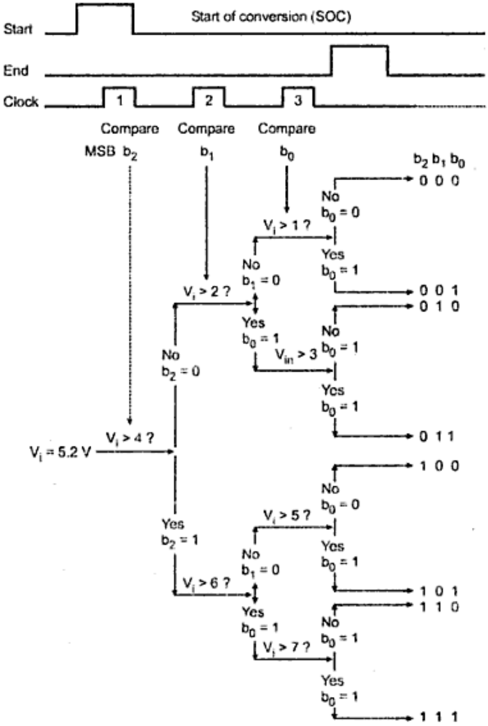

Start
Start of conversion (SOC)
End
Clock
1
2
3
Compare MSB b2
Compare b1
Compare b0
b2 b1 b0
000
No b0 = 0
V1 > 1 ?
Yes b0 = 1
No b1 = 0
V1 > 2 ?
001
010
Yes b0 = 1
No b0 = 1
Vin > 3
No b2 = 0
Yes b0 = 1
V1 > 4 ?
Vi = 5.2 V
011
100
No b0 = 0
V1 > 5 ?
Yes b2 = 1
Yes b0 = 1
No b1 = 0
V1 > 6 ?
101
110
Yes b0 = 1
No b0 = 1
V1 > 7 ?
Yes b0 = 1
111

Fig. 9.124 Illustration of conversion process

The dark lines in the Fig. 9.124 shows setting and resetting actions of bits for input voltage 5.2 V, on the basis of comparison. It can be seen from the Fig. 9.124 that one clock pulse is required for the successive approximation regsiter to compare each bit. However an additional clock pulse is usually required to reset the register prior to performing a conversion.

The time for one analog to digital conversion must depend on both the clock's period T and number of bits n. It is given as,

$$T_C = T(n+1) \qquad \ldots(5)$$

where T_C = Conversion time

T = Clock period

n = Number of bits

Example 9.42 : *An 8 bit successive approximation ADC is driven by a 1 MHz clock. Find its conversion time.*

Solution : $f = 1\text{ MHz}$

$$\therefore \quad T = \frac{1}{f} = \frac{1}{1\times 10^6} = \mathbf{1\ \mu sec}$$

$$n = 8$$

$$\therefore \quad T_C = T(n+1) = 1(8+1) = \mathbf{9\ \mu sec.}$$

9.37.4 Flash ADC

When system designs call for the highest speed available, flash-type A/D converters (ADCs) are likely to be the right choice. They get their names from their ability to do the conversion very rapidly. Flash A/D converters, also known as a simultaneous or parallel comparator ADC, because the fast conversion speed is accomplished by providing $2^n - 1$ comparators and simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

Fig. 9.125 shows 3-bit flash A/D converter. For this ADC, seven $(2^3 - 1)$ comparators are required. As shown in the Fig. 9.125, one input of each comparator is connected to the input signal and other input to the reference voltage level generated by the reference voltage divider. The reference voltage (V_{REF}) is equal to the full scale input signal voltage. The manner in which the flash A/D converter performs a quantization is relatively simple.

The comparators give output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referred above the input signal, remain turned-off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The code resulting from this comparator is converted to a binary code by the encoder.

➽ **Example 9.43 :** *For a particular 8-bit ADC, the conversion time is 9 μs. Find the maximum frequency of an input sine wave that can be digitized.*

Solution : The maximum frequency is given by,

$$f_{max} \approx \frac{1}{2\pi(T_C)2^n} \approx \frac{1}{2\pi\times 9\times 10^{-6}\times 2^8}$$

$$\approx \textbf{69.07 Hz}$$

9.37.5 Comparison between Flash, Dual Slope and Successive Approximation Techniques

The comparison of ADCs is given in the tabular form as below :

<table>
<tr><th>Parameter</th><th colspan="3">Flash</th><th colspan="3">Successive approximation</th><th colspan="3">Dual slope</th></tr>
<tr><td>Speed</td><td colspan="3">Fastest</td><td colspan="3">Fast</td><td colspan="3">Slow</td></tr>
<tr><td>Accuracy</td><td colspan="3">Less</td><td colspan="3">Medium</td><td colspan="3">More</td></tr>
<tr><td>Resolution</td><td colspan="3">Upto 2^8</td><td colspan="3">Upto 2^{16}</td><td colspan="3">2^{16} or even more</td></tr>
<tr><td>Input hold time</td><td colspan="3">Very less</td><td colspan="3">Depend on number of bits. It is more than flash A/D converter.</td><td colspan="3">It is maximum, hence sample and hold circuit is required.</td></tr>
<tr><td>Cost</td><td colspan="3">Very costly</td><td colspan="3">Medium</td><td colspan="3">Less</td></tr>
<tr><td>Applications</td><td colspan="3">High speed fiber optic communication, Digital storage oscilloscope, Imaging and many more where high speed A/D conversion is required.</td><td colspan="3">The successive approximation A/D converter has the disadvantage of requiring D/A converter, but it has the advantage of high speed with excellent resolution. Hence these are most popular and used in data acquisition systems.</td><td colspan="3">These are used when high accuracy and resolution is required and speed is not the important criteria.</td></tr>
<tr><td></td><td>IC</td><td>Resolution</td><td>Conversion rate</td><td>IC</td><td>Resolution</td><td>Conversion rate</td><td>IC</td><td>Resolution</td><td>Conversion rate</td></tr>
<tr><td rowspan="4">ICs</td><td>AD6020KD</td><td>6</td><td>50 MHz</td><td>ADC1103</td><td>8</td><td>1 MHz</td><td>ADC141</td><td>14</td><td>25 Hz</td></tr>
<tr><td>AD9000SD</td><td>6</td><td>75 MHz</td><td>ADC60</td><td>10</td><td>670 kHz</td><td>7109</td><td>12</td><td>30 Hz</td></tr>
<tr><td>TM1070</td><td>7</td><td>15 MHz</td><td>ADC1103</td><td>12</td><td>300 kHz</td><td>ADB1200</td><td>12</td><td>28 Hz</td></tr>
<tr><td>TDC10193</td><td>9</td><td>25 MHz</td><td>ADC72</td><td>16</td><td>20 kHz</td><td>LF13300</td><td>12</td><td>28 Hz</td></tr>
</table>

9.37.6 Counter Type ADC

Principle of operation :

This ADC uses DAC for A to D conversion. The output of the DAC is continuously compared with the analog input to the ADC which is to be converted into digital ouput. When the output of the DAC becomes greater than this analog input, the corresponding digital input to the DAC is noted which represents the analog input to the ADC.

Fig. 9.126 shows the circuit diagram of counter type ADC.

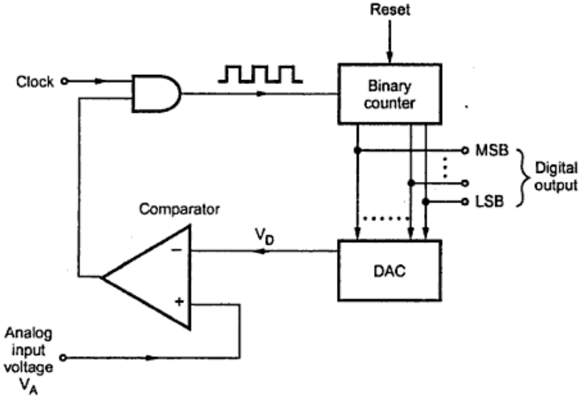


Fig. 9.126

As shown in the Fig. 9.126, the counter type ADC consists of a binary counter, DAC, comparator and AND gate. The operation of the circuit is explained below.

i) Initially, the counter is reset, i.e. its output is set to zero by applying a reset pulse. The output of the counter is given as digital input to DAC. Since input to DAC is zero, its output V_D is zero.

ii) When the analog input voltage V_A is applied to ADC, it becomes greater than V_D. V_A acts as input voltage for non inverting terminal and V_D acts as input voltage for inverting terminal of the comparator. Since V_A is greater than V_D , the comparator output goes high.

iii) For an AND gate, one input is clock pulses and another input is the output of the comparator. Because of the high output of the comparator, the clock pulses are allowed to pass through the AND gate.

iv) The counter starts counting these close pulses. According to the number of clock pulses, the output of the counter goes on increasing. This increases the output of the DAC.

v) The above steps are continued till V_D is less than V_A.

vi) As soon as DAC output V_D becomes greater than V_A, the comparator output goes low. This disables AND gate. So the clock pulses are not allowed to pass through the AND gate. The counting process of the binary counter is stopped.

vii) The output of the binary counter which is in digital form is noted which represents the digital equivalent of the analog input voltage V_A.

viii) For the next A to D conversion, the input voltage to ADC, V_A changes. The binary counter is cleared by applying a second reset pulse and all the above steps are repeated to obtain the digital equivalent of V_A.

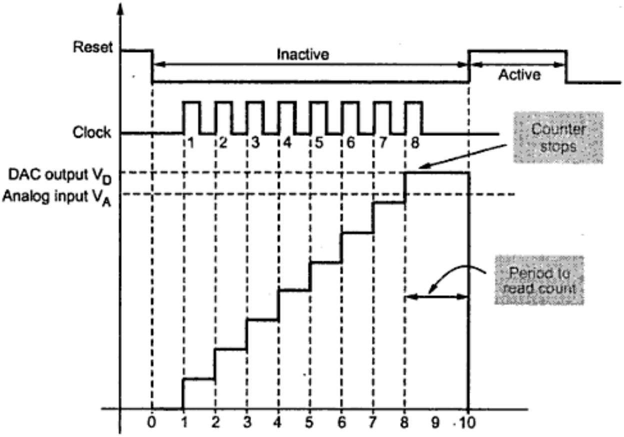


Fig. 9.127 Waveforms for counter type ADC

Disadvantages

- It is necessary to give enough time for DAC conversion and comparator to respond. Therefore, there is a limitation on the clock frequency. As clock frequency is low, the speed of conversion is less.
- Conversion time is not constant. It increases with increase in input voltage. In other words, we can say that conversion time is high at high input voltage.

9.37.7 Delta Modulation (DM)

The delta modulation technique for analog to digital conversion is used in digital communication. In this technique, the analog signal is converted into pulses which can represented by digital data.

The Fig. 9.128 (a) shows the basic circuit for delta modulator. It consists of comparator, one bit quantizer and integrator. The comparator compares the input analog signal m(t) with the feedback signal m′(t), which is the integrated form of the output signal $p_o(t)$. The comparator output produces the difference signal. If the difference signal is positive, it is encoded as a binary 1, whereas if the difference signal is negative, it is encoded as a binary 0. A binary 1 is transmitted as a positive voltage pulse and binary 0 is transmitted as a negative voltage pulse.

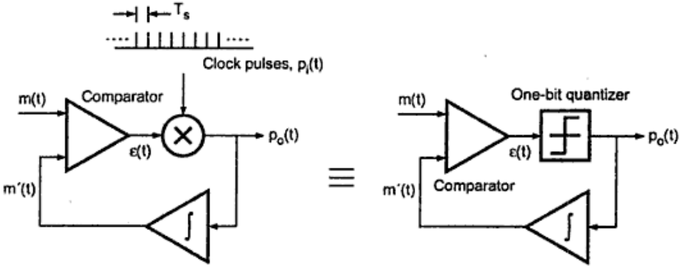


Fig. 9.128 (a) DM transmitter

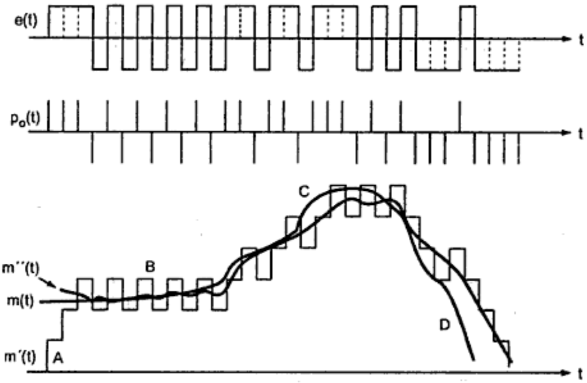


Fig. 9.128 (b) DM waveforms

According to difference signal the positive and negative pulses are generated with the help of multiplier. One input of the multiplier is a difference signal e(t) and the other input of the multiplier is a periodic train of unipolar impulses (very short pulses) $p_i(t)$ at the sampling frequency f_s. Therefore, the output of multiplier is a sequence of impulses $p_o(t)$ whose polarity depends on the difference signal. This is illustrated in Fig. 9.128 (b).

As mentioned earlier, sequence of impulses $p_o(t)$ can be encoded as binary output by encoding positive impulse as a binary 1 and negative impulse as a binary 0.

In the reverse process, the encoded binary data is converted into impulses and then integrated to produce staircase approximation $m'(t)$ as shown in Fig. 9.128 (b). Finally, the analog output $m''(t)$ is generated from the integrator output through the use of a low-pass reconstruction filter.

Advantages of Delta Modulation

1. It is a simple technique.
2. It represents each analog sample by only one bit.

Disadvantages of Delta Modulation

1. **Granular noise :** As shown in the Fig. 9.128 (b), the $m'(t)$ waveform is a staircase approximation to the analog signal m(t). For this staircase waveform, there will be an initial transient period labelled A. When modulator reaches steady state, the staircase waveform **"hunts"** around the analog waveform as shown at B. This hunting produces granular noise. The granular noise occurs when the step size is two large compared to small variations in the input signal. This can be observed at point B. Here, input is slowly increasing but the staircase waveform remains horizontal. The granual noise can be reduced by keeping step size small.
2. **Slope overload distortion :** The slope overload distortion occurs when the rate of change of the analog waveform is too high for the staircase waveform to follow. The slope overload causes a large error between the staircase approximated signal, $m'(t)$ and the original input signal, m(t). At point C and D waveform suffers from slope overload distortion. Since the step size of delta modulator remains fixed, its maximum or minimum slopes occur along straight lines. In case of horizontal line slope overload distortion is minimum, and it is maximum along the vertical line. The slope overload distortion can be minimised by increasing the step size. But increase in step size increases granular noise. To solve this problem the delta modulation process is modified and known as **adaptive delta modulation.**

9.37.8 Adaptive Delta Modulation (ADM)

To overcome the quantization errors due to slope overload and granular noise, the step size is made adaptive to variations in the input signal m (t). Particularly in the steep segment of the input signal m(t), the step size is increased. When the input is varying slowly, the step size is reduced. This method is called Adaptive Delta Modulation. The adaptive modulators can take continuous changes in step size or discrete changes in step size. The Fig. 9.129 shows the circuit for generation of adaptive delta modulated signal. The logic for step size control is added in the diagram. The step size increases or decreases according to certain rule depending on one bit quantizer output. For example if one bit quantizer output is high (1), then step size may be doubled for next sample. If one bit

2. Because of the variable step size, the dynamic range of ADM is wide.
3. Utilization of bandwidth is better than delta modulation.

Review Questions

1. *Draw the circuit diagram of a comparator using IC741 op-amp. Explain its working.*
2. *How to move a trip point in a basic non-inverting comparator?*
3. *Explain how an op-amp can be used as comparator.*
4. *Draw and explain inverting and non-inverting comparator circuits.*
5. *Explain op-amp as a Schmitt trigger.*
6. *What is the most important applications of Schmitt trigger circuit.*
7. *Explain the working of Schmitt trigger.*
8. *Design Schmitt trigger having upper and lower thresholds of 120 mV. Input to this circuit is 1 V peak to peak triangular wave of 100 Hz. Draw the Hysteresis loop.*
9. *Design a Schmitt trigger for UTP = + 0.5 V and LTP = – 0.5 V.*
10. *How to obtain different UPT and LTP levels in a Schmitt trigger ?*
11. *What is a multivibrator circuit ? What is its use ? State its types.*
12. *Draw and explain the operation of monostable multivibrator using op-amp.*
13. *Derive the expression for pulse width of monostable multivibrator.*
14. *Draw and explain the operation of astable multivibrator using op-amp.*
15. *Derive the expression for frequency of oscillations in astable multivibrator.*
16. *Which are the basic elements of IC 555 ?*
17. *How transistorised R-S flip flop circuit works ?*
18. *Draw and explain the basic timing circuit of IC 555. Draw the necessary waveforms.*
19. *Explain the principle of RC timer in IC 555.*
20. *Draw and explain the functional block diagram of IC 555.*
21. *Explain in brief the functions of pins 2, 3, 4, 5, 6 of IC 555.*
22. *Draw and explain block diagram of IC 555.*
23. *Explain the importance of control voltage pin 5 of timer 555.*
24. *Derive the expression for the pulse width of a monostable multivibrator using IC 555.*
25. *State any two applications of monostable multivibrator.*
26. *Determine the output pulse width of the monostable multivibrator using IC 555, if R = 12 kΩ and C = 0.1 μF.* **(Ans. : 1.32 ms)**
27. *A IC 555 timer used as a monostable has R = 20 kΩ and C = 0.01 μF. What is the duration of output pulse ?* **(Ans. : 0.22 ms)**
28. *Estimate the values of timing elements to generate a time delay of 1 ms using IC 555 timer as a monostable multivibrator.*

29. *Describe the monostable mode of operation of IC 555. Does the same circuit work as timer ? Justify. Draw the necessary waveforms and expressions.*
30. *Mention various practical applications of IC - 555 timer. Explain any one monostable application.*
31. *Define duty cycle. Derive the expression for the duty cycle of an astable multivibrator using 555.*
32. *Derive the expression for the frequency of the output of an astable multivibrator.*
33. *How astable mode of 555 can be modified to get a square wave generator ?*
34. *A 555 timer is configured to run in astable mode with* $R_1 = 20\ k\Omega$ *and* $R_2 = 8\ k\Omega$ *and* $C = 0.1\ \mu mF$*. Determine the output frequency and duty cycle.* **(Ans. : 400 Hz, 77.77 %)**
35. *State the applications of astable multivibrator using IC 555.*
36. *Draw and explain astable multivibrator using IC 555. Draw the output and capacitor voltage waveforms. What is the range of duty cycle we can have with astable circuit ?*
37. *Draw the circuit diagram of an astable multivibrator for 50% duty cycle output using IC 555, and explain its operation. Give any two applications of astable multivibrator.*
38. *State the application of astable multivibrator using IC 555 and explain any one.*
39. *List the features of IC 555.*
40. *Which are the two ways of connecting load to IC 555 ?*
41. *What is the difference between A/D and D/A converters ?*
42. *Define the following terms for D/A converters : Resolution, accuracy, monotonicity, and conversion time.*
43. *Explain the binary weighted resistor technique of D/A conversion.*
44. *Explain the R/2R ladder technique of D/A conversion ?*
45. *Explain the advantages of R/2R ladder technique over binary weighted resistor technique.*
46. *List the drawbacks of binary weighted resistor technique of D/A conversion.*
47. *What are different source of errors in DACs ?*
48. *Explain the operation of a 4 bit R-2R type DAC and derive the expression for the output voltage.*
49. *Explain following with reference to DAC :*
    i. Linearity ii. Accuracy iii. Settling time
50. *Obtain an expression for the output voltage of R/2R DAC.*
51. *For the R/2Rladder 4 bit type DAC, find the output voltage and resolution if digital input is 1111. Assume* $V_R = 10\ V$ *and* $R = 10\ k\Omega = R_f$ **(Ans. : 9.375 V, 0.625 V)**
52. *Find out stepsize and analog output when input is 1000 and 1111. Assume* $V_{ref} = +5\ V$
    (Ans. : Stepsize = 0.3125 V, 1000 → 2.5 V, 1111 →4.6875)
53. *List the various specifications of ADC.*
54. *List various A/D conversion techniques.*
55. *What do you mean by quantization error ?*
56. *Explain the digital ramp A/D converter with the help of neat block diagram.*
57. *Explain the successive approximation A/D converter technique with the help of block diagram.*
58. *Explain the operation of flash A/D converter.*

59. *Which is the fastest ADC and why ?*

60. *Explain the dual slope A/D converter technique with the help of block diagram.*

61. *What is Delta modulation ?* **[April-2004, 5 Marks]**

62. *Draw block diagram of delta the modulation circuit.* **[April-2005, 5 Marks]**

63. *Explain ADM.* **[April-2003, April-2004, 6 Marks]**

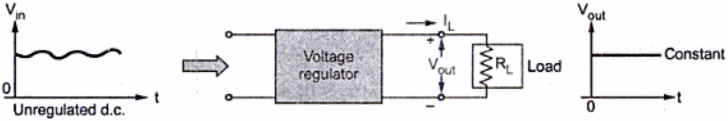
❑❑❑

10

Voltage Regulators

10.1 Introduction

The **voltage** regulator circuit keeps the output voltage constant inspite of changes in the load current or input voltage. Its input is unregulated pulsating d.c. voltage obtained from filter and rectifier. Its output is constant d.c. voltage which is almost ripple free. The basic block diagram of voltage regulator is shown in the Fig. 10.1.

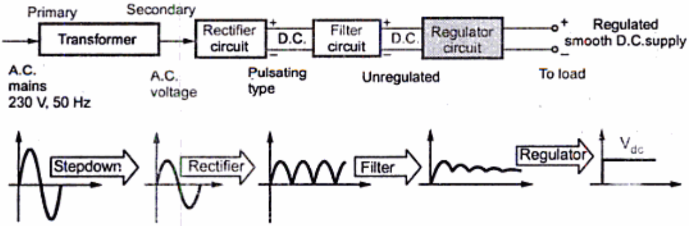


V_{in}
0
t
Unregulated d.c.
Voltage regulator
I_L
+
V_{out}
−
R_L
Load
V_{out}
Constant
0
t

Fig. 10.1 Concept of voltage regulator

10.2 Block Schematic of Regulated Power Supply

A typical d.c. power supply consists of various stages. The Fig. 10.2 shows the block diagram of a typical d.c. power supply consisting of various circuits. The nature of voltages at various points is also shown in the Fig. 10.2.



Primary
Secondary
Transformer
Rectifier circuit
+
D.C.
−
Filter circuit
+
D.C.
−
Regulator circuit
+
−
Regulated smooth D.C.supply
A.C. mains 230 V, 50 Hz
A.C. voltage
Pulsating type
Unregulated
To load
Stepdown
Rectifier
Filter
Regulator
V_{dc}

Fig. 10.2 Block Schematic of regulated power supply with waveforms

The a.c. voltage (230 V, 50 Hz) is connected to the primary of the transformer. The transformer steps down the a.c. voltage, to the level required for the desired d.c. output. Thus, with suitable turns ratio we get desired a.c. secondary voltage. The rectifier circuit converts this a.c. voltage into a **pulsating d.c. voltage**. A pulsating d.c. voltage means a unidirectional voltage containing large varying component called **ripple** in it. The **filter** circuit is used after a rectifier circuit, which reduces the ripple content in the pulsating d.c. and tries to make it smoother. Still then the filter output contains some ripple. This voltage is called **unregulated d.c. voltage**. A circuit used after the filter is a regulator circuit which not only makes the d.c. voltage smooth and almost ripple free but it also keeps the d.c. output voltage constant though input d.c. voltage varies under certain conditions. It keeps the output voltage constant under variable load conditions, as well. The output of a regulator is called **d.c. supply**, to which the load can be connected. Now a days, complete regulator circuits are available in the integrated circuit (IC) form.

Key Point : *Thus a voltage regulator circuit is the one which is designed to keep the output voltage of a power supply nearly constant, under varying input voltage conditions and varying load conditions.*

10.3 Factors Affecting the Load Voltage

The various factors which affect the load voltage in a power supply are,

a) The load current (I_L) : An ideal power supply maintains a constant voltage at its output terminals, inspite of changes in load current. But practically in a power supply without regulator the load voltage decreases as the load current I_L increases. For a practical power supply with regulator load voltage must be constant though load changes from no load condition to full load condition. But with regulator circuit also the load voltage gets affected by the load current in a power supply.

b) The line voltage : The input to the rectifier which is a.c. line voltage decides the level of the output voltage. Hence any change in the line voltage, changes the load voltage and affects the performance of the power supply. Ideally the d.c. output voltage must remain constant irrespective of any changes in the line voltage.

c) The temperature : In a power supply, the rectifier circuit uses the p-n junction diodes. The diode characteristics are temperature sensitive. The other semiconductor devices used in power supplies have their characteristics, temperature dependent. Hence the temperature is an important factor responsible for the changes in the load voltage.

The voltage regulator circuit in a power supply, has to consider these factors and provide constant d.c. output voltage.

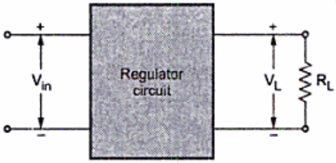
10.4 Power Supply Performance Parameters

The performance of the overall power supply is judged by specifying some parameters, based on the factors discussed above. Let us see in detail the various power supply performance parameters.

10.4.1 Load Regulation

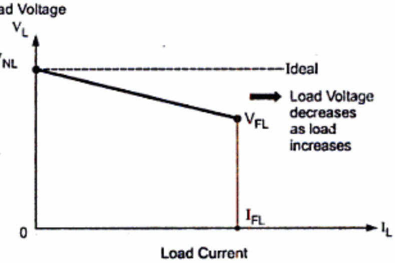
The load regulation is the change in the regulated output voltage when the load current is changed from minimum (no load) to maximum (full load).

Consider the block diagram of regulator circuit shown in the Fig. 10.3.



Block diagram of regulator

Fig. 10.3



Regulation characteristics

Fig. 10.4

The load regulation is denoted as LR and mathematically expressed as,

$$\boxed{LR = V_{NL} - V_{FL}}$$

where V_{NL} = load voltage with no load current

V_{FL} = load voltage with full load current

The load regulation is often expressed as percentage by dividing the LR by full load voltage and multiplying result by 100.

$$\therefore \quad \boxed{\%\ LR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100}$$

The graph of load current against load voltage is called regulation characteristics of a power supply. The ideal value of load regulation is zero. Less the regulation, better is the performance of regulator. The regulation characteristics is shown in the Fig. 10.4.

10.4.2 Line Regulation or Source Regulation

The input to the unregulated power supply i.e. rectifier circuit is 230 V a.c. supply. This line voltage may change, under the different load conditions. This affects the output voltage of rectifier which is V_{in} for a regulator circuit. Hence the characteristics which gives source effect on regulator performance is defined.

The line regulation is also called source regulation and denoted as SR.

The SR is defined as the change in the regulated load voltage for a specified range of line voltage, typically 230 V ± 10 %.

Mathematically it is expressed as,

$$\boxed{SR = V_{HL} - V_{LL}}$$

where V_{HL} = load voltage with high line voltage

V_{LL} = load voltage with low line voltage

The percentage source regulation is defined as,

$$\boxed{\% \; SR = \frac{SR}{V_{nom}} \times 100}$$

where V_{nom} = nominal load voltage

10.4.3 Output Resistance

To understand the effect of output resistance on the load voltage, consider the representation of power supply in terms of no load voltage V_{NL} and output resistance R_{out} as shown in the Fig. 10.5.

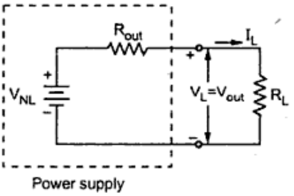


Fig. 10.5 Concept of R_{out}

When no load is connected to the output terminals, the current I_L is zero. Hence load voltage V_L is equal to no load voltage V_{NL}.

But when a certain load resistance R_L is connected then,

$$V_L = V_{out} = V_{NL} - I_L R_{out}$$

Thus ideally for a power supply R_{out} must be zero and V_{out} must be equal to V_{NL}, whatever may be the load current drawn.

Practically the output resistance of a power supply is very small and it can supply different loads with a constant load voltage. For a regulated power supply, the output resistance is in the range of milliohms.

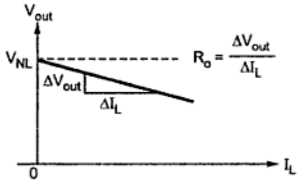


Fig. 10.6 Load regulation characteristics

The value of R_{out} is obtained by finding the slope of a load regulation characteristics. Consider the load regulation characteristics as shown in the Fig. 10.6.

The slope of this characteristics is the output resistance.

Hence mathematically the output resistance can be expressed as,

$$\boxed{R_{out} = \left.\frac{\Delta V_{out}}{\Delta I_L}\right|_{V_{in} \text{ and temperature constant}}}$$

10.4.4 Voltage Stability Factor (S_V)

Another way of specifying the dependence of output voltage on line voltage is defining voltage stability factor denoted as S_V. It is the percentage change in the output voltage which occurs per volt change in the input line voltage, with load current and the temperature are assumed constant. Mathematically it is expressed as,

$$\boxed{S_V = \left.\frac{\Delta V_{out}}{\Delta V_{in}}\right|_{I_L \text{ and temperature constant}}}$$

Smaller the value of this factor better is the performance of power supply.

10.4.5 Temperature Stability Factor (S_T)

As mentioned earlier, the semiconductor devices having temperature dependent characteristics cause change in the output voltage as temperature changes. Thus the temperature stability of power supply will be determined by temperature coefficients of various temperature sensitive semiconductor devices. By selecting low temperature coefficient devices, the output voltage of a power supply can be fairly independent of temperature.

For example, zener diodes having breakdown voltages in the range of 5 to 8 V have very low temperature coefficient and hence are always preferred and used in the power supply circuits.

Mathematically temperature stability factor is expressed as,

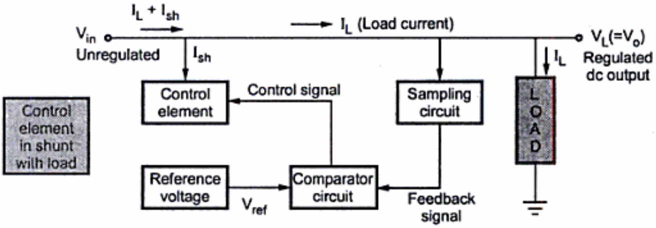
$$\boxed{S_T = \left.\frac{\Delta V_{out}}{\Delta T}\right|_{V_{in} \text{ and } I_L \text{ constant}}}$$

The value of this factor must be as small as possible ideally zero, for a power supply.

Each type, provides a constant d.c. output voltage which is regulated. Let us discuss the functional block diagram and working principle of each of these two types of regulator circuits.

10.6.1 Shunt Voltage Regulator

The heart of any voltage regulator circuit is a control element. If such a control element is connected in shunt with the load, the regulator circuit is called shunt voltage regulator. The Fig. 10.7 shows the block diagram of shunt voltage regulator circuit.



$I_L + I_{sh}$
I_L (Load current)
V_{in}
Unregulated
I_{sh}
$V_L(=V_o)$
I_L
Regulated dc output
Control element in shunt with load
Control element
Control signal
Sampling circuit
LOAD
Reference voltage
V_{ref}
Comparator circuit
Feedback signal

Fig. 10.7 Block diagram of shunt voltage regulator

Operation :

The unregulated input voltage V_{in}, tries to provide the load current. But part of the current is taken by the control element, to maintain the constant voltage across the load. If there is any change in the load voltage, the sampling circuit provides a feedback signal to the comparator circuit. The comparator circuit compares the feedback signal with the reference voltage and generates a control signal which decides the amount of current required to be shunted to keep the load voltage constant. For example, if load voltage increases then comparator circuit decides the control signal based on the feedback information, which draws increased shunt current I_{sh} value. Due to this, the load current I_L decreases and hence the load voltage decreases to its normal. Thus control element maintains the constant output voltage by shunting the current, hence the regulator circuit is called voltage shunt regulator circuit.

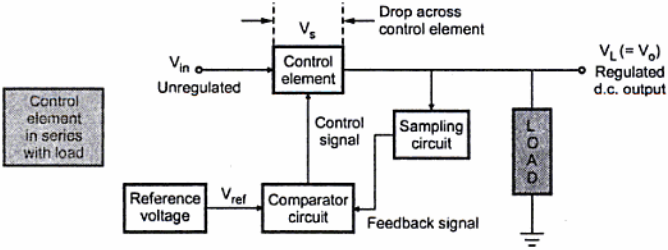
As seen from the block diagram, only part of the load current required to be diverted, passes through the control element. **Thus the control element is low current, high voltage rating component.** The efficiency depends on the load current I_L. Hence shunt regulators are not preferred for varying load conditions.

Process flowchart of shunt regulator is,

If output increases above regulated value	→	Feedback increases	→	Control signal increases	→	Current I_{sh} through control element increases	→	Load current I_L decrease	→	Output voltage decreases to its original value
If output decreases bleow regulated value	→	Feedback decreases	→	Control signal decreases	→	Current I_{sh} thought control element decreaes	→	Load current I_L increaes	→	Output voltage increases to its orignial value

10.6.2 Series Voltage Regulator

If in a voltage regulator circuit, the control element is connected in series with the load, the circuit is called series voltage regulator circuit. The Fig. 10.8 shows the block diagram of series voltage regulator circuit.



Drop across control element
V_s
V_{in}
Unregulated
Control element
$V_L (= V_o)$
Regulated d.c. output
Control element in series with load
Control signal
Sampling circuit
LOAD
Reference voltage
V_{ref}
Comparator circuit
Feedback signal

Fig. 10.8 Block diagram of series voltage regulator

Operation :

The unregulated d.c. voltage is the input to the circuit. The control element, controls the amount of the input voltage, that gets to the output. The sampling circuit provides the necessary feedback signal. The comparator circuit compares the feedback with the reference voltage to generate the appropriate control signal.

For example, if the load voltage tries to increase, the comparator generates a control signal based on the feedback information. This control signal causes the control element to decrease the amount of the output voltage. Thus the output voltage is maintained constant.

Thus, control element which regulates the load voltage, based on the control signal is in series with the load and hence the circuit is called series voltage regulator circuit.

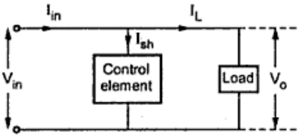
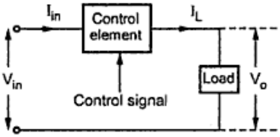
In series regulators, the entire current passes through the control element and hence **control element is high current, low voltage rating component.** As input current and load current are same, the efficiency depends on output voltage. It provides good regulation than shunt regulators. It can be used for fixed voltage as well as variable voltage requirements. To compensate for the drop across the control element, input voltage V_{in} must be at least 2 to 3 V more than output voltage.

Process flowchart of series regulator is,

If output increases above regulated value → Feedback increases → Control signal increases → Voltage across the control element increases → Output voltage decreases back to its original value

If output decreases bleow regulated value → Feedback decreases → Control signal decreases → Voltage across the control element decreases → Output voltage increases back to its orignial value

10.6.3 Comparison of Shunt and Series Regulators

Sr. No.	Shunt Regulator	Series Regulator
1.	1. The control element is in parallel with the load.  I_{in} I_L I_{sh} Control element Load V_{in} V_o	The control element is in series with the load.  I_{in} Control element I_L Load V_{in} V_o Control signal
2.	Only small current passes through the control element, which is required to be diverted to keep output constant.	The entire load current I_L always passes through the control element.
3.	Any change in output voltage is compensated by changing the current I_{sh} through the control element as per the control signal.	Any change in output voltage is compensated by adjusting the voltage across the control element as per the control signal.
4.	The control element is low current, high voltage rating component.	The control element is high current, low voltage rating component.
5.	The regulation is poor.	The regulation is good.
6.	Efficiency depends on the load current.	Efficiency depends on the output voltage.
7.	Not suitable for varying load conditions. Preferred for fixed voltage applications	Preferred for fixed as well as variable voltage applications.

8.	Simple to design.	Complicated to design as compared to shunt regulators.
9.	Examples are : Zener shunt regulator, transistorised shunt regulator etc.	Examples are : Series feedback type regulator, series regulator with preregulator and foldback limiting etc.

Table 10.1

10.7 Shunt Regulator using Op-amp

The op-amp can be used as a voltage comparator. The circuit diagram is shown in the Fig. 10.9. The potential divider formed by the resistances R_1 and R_2, provides the part of the output voltage as a feedback. The op-amp compares this with the reference voltage generated by zener diode. The op-amp provides the control (signal) current to shunt control element which is the transistor Q. The current through the resistance R is thus controlled to drop a voltage across R so that the output voltage is maintained constant.

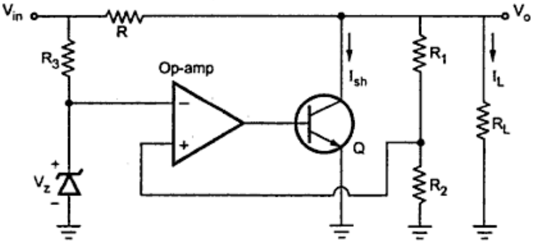


Fig. 10.9 Shunt regulator using op-amp

The shunt regulator is generally suffered with the following limitations :

i) The maximum load current that can be supplied is limited.

ii) A large amount of power is wasted in the zener diode and the series resistance R, in comparison with the load power.

iii) The performance factors like stability factor and the output resistance are not very low, as desired for a good regulator circuit.

10.8 Voltage Follower Regulator using Op-amp

The voltage follower d.c. regulator is nothing but **fixed voltage series regulator using op-amp**. It is shown in the Fig. 10.10.

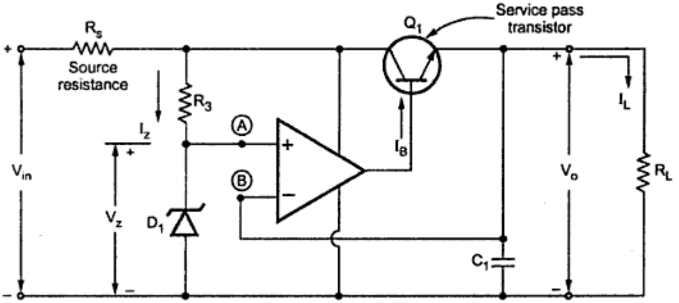


Fig. 10.10 Voltage follower regulator

The op-amp is used as a comparator. The supply of op-amp is derived from input supply terminals. Hence op-amp supply voltages are $+V_{in}$ and ground. The inverting terminal of op-amp is connected to the output terminal.

$$\therefore \qquad V_B = V_o$$

While the voltage of noninverting terminal i.e. node A is zener voltage V_Z, decided by the zener diode D_1.

$$\therefore \qquad V_A = V_Z$$

But due to virtual ground,

$$V_B = V_A$$

$$\text{i.e.} \qquad V_o = V_Z$$

Key Point: Thus the output voltage is constant equal to zener voltage.

The series pass transistor is to supply the additional load current which op-amp can not supply. For large load current, op-amp has to supply only base current of the transistor, I_B.

If load current is less than 25 mA, series pass transistor Q_1 does not play any role and op-amp behaves as a voltage follower.

The C_1 is large capacitor of the order of 50 to 100 μF. The functions of C_1 are,

1. To help to supply fast demands on regulator.
2. To eliminate the possibility of any oscillatory behaviour of the regulator.

Using equation (7) in equation (5), load regulation can be obtained.

While the ripple rejection is,

$$\boxed{RR = 20 \text{ Log } \frac{V_R(\text{out})}{V_R(\text{in})} \text{ dB}} \quad \text{... (8)}$$

Using $V_R(\text{in})$ for ΔV_{in} and $V_R(\text{out})$ for ΔV_o in the equation (3) we get,

$$\boxed{V_R(\text{out}) = \frac{V_R(\text{in}) Z_Z}{R_3}} \quad \text{... (9)}$$

From this, ripple rejection can be obtained.

Example 10.1 : *For a particular voltage follower d.c. regulator $V_{in} = 15 \pm 10$ % with $R_s = 20\ \Omega$. The output voltage is 4.7 V with $R_3 = 330\ \Omega$. The maximum load current is 50 mA. Find*

i) Line regulation ii) Load regulation and iii) Ripple rejection.

The dynamic impedance of zener diode is 7 Ω.

Solution : $Z_Z = 7\ \Omega$, $R_3 = 330\ \Omega$, $V_o = 4.7$ V, $V_{in} = 15$ V

The specified change in V_{in} is 10 %,

$$\therefore \quad \Delta V_{in} = 10 \% \text{ of } V_{in} = 0.1 \times 15 = 1.5 \text{ V}$$

$$\therefore \quad \Delta V_o = \frac{\Delta V_{in} Z_Z}{R_3} = \frac{1.5 \times 7}{330} = 0.03181 \text{ V}$$

$$\therefore \quad \text{Line regulation} = \frac{\Delta V_o \times 100}{V_o} = \frac{0.03181 \times 100}{4.7} = \mathbf{0.677\ \%}$$

For $I_L(\text{max}) = 50$ mA,

$$\Delta V_o = \frac{I_L(\text{max}) R_s Z_Z}{R_3} = \frac{50 \times 10^{-3} \times 20 \times 7}{330} = \mathbf{0.02121\ V}$$

$$\therefore \quad \text{Load regulation} = \frac{\Delta V_o \times 100}{V_o} = \frac{0.02121 \times 100}{4.7} = \mathbf{0.4513\ \%}$$

Now $V_R(\text{out}) = \dfrac{V_R(\text{in}) Z_Z}{R_3}$

$$\therefore \quad \frac{V_R(\text{out})}{V_R(\text{in})} = \frac{Z_Z}{R_3} = \frac{7}{330} = 0.02121$$

$$\therefore \quad RR = 20 \text{ Log } 0.02121 = \mathbf{-33.46\ dB}$$

10.9 Adjustable Output Regulator

The series regulator having fixed output voltage of $V_o = V_Z$ can be converted to adjustable output regulator. This is possible by connecting a potential divider at the output. This is shown in the Fig. 10.11.

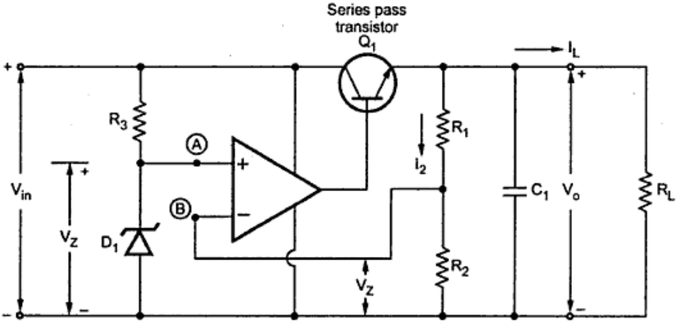


Fig. 10.11 Adjustable output regulator

The basic operation of the circuit is same as voltage follower regulator. The voltage at noninverting terminal is V_Z i.e. $V_A = V_Z$. Due to virtual ground, $V_B = V_A = V_Z$.

Now this V_Z is voltage across R_2 as shown in the Fig. 10.11. If V_{R2} becomes more than V_Z, then this reduces the op-amp output which controls the conduction of transistor Q_1 and finally V_o reduces to such a level which gives $V_{R2} = V_Z$.

There exists a fixed relation between V_o and V_{R2}. From potential divider rule,

$$V_{R2} = V_Z = \frac{V_o R_2}{R_1 + R_2} \qquad \dots (1)$$

The op-amp acts as a comparator i.e. error amplifier. It amplifies the error if any and maintains output at constant level.

From equation (1),

$$\boxed{V_o = \frac{V_Z (R_1 + R_2)}{R_2} = V_Z \left[1 + \frac{R_1}{R_2}\right]} \qquad \dots (2)$$

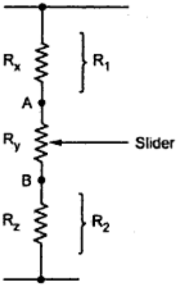


Fig. 10.12

Thus by adjusting proportion of R_1 and R_2, the output voltage can be made adjustable. The proportion of $R_1 - R_2$ can be practically adjusted as shown in the Fig. 10.11.

By adjusting the position of slider, the proportion of $R_1 - R_2$ can be adjusted. When position of slider is at A, $R_1 = R_x$ and $R_2 = R_y + R_z$ while when position of slider is at B, $R_1 = R_x + R_y$ and $R_2 = R_z$.

10.9.1 Performance Parameters

The expression derived for performance parameters for voltage follower constant voltage regulator are applicable for adjustable voltage regulator with a change that the factor by which V_Z gets multiplied appears in all the expresssions.

$$\therefore \quad \boxed{\Delta V_o = \frac{\Delta V_{in} Z_Z}{R_3} \times \left[1 + \frac{R_1}{R_2}\right]} \quad \ldots (3)$$

and

$$\boxed{\Delta V_o = \frac{I_L(\max) R_s Z_Z}{R_3}\left[1 + \frac{R_1}{R_2}\right]} \quad \ldots (4)$$

$$\boxed{V_R(\text{out}) = \frac{V_R(\text{in}) Z_Z}{R_3}\left[1 + \frac{R_1}{R_2}\right]} \quad \ldots (5)$$

Example 10.2 : *Design an op-amp series voltage regulator to meet the following specifications :*

$V_i = (18 \pm 3)$ volts

$V_o = 9$ volts at $I_o = 10$ to 50 mA

Zener available $V_Z = 5.6$ V

$P_{Z\,max} = 0.5$ W

Solution :

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z$$

$$\therefore \quad 9 = \left(1 + \frac{R_1}{R_2}\right) 5.6$$

$$\therefore \quad 1+\frac{R_1}{R_2} = 1.6071$$

$$\therefore \quad \frac{R_1}{R_2} = 0.6071$$

Let $R_1 = \mathbf{10\ k\Omega}$

$$\therefore \quad R_2 = \mathbf{16.47\ k\Omega}$$

Minimum zener current is say 5 mA, which is same as current through R_3.

$$\therefore \quad I_{Z\,min} = \frac{V_{in\,(min)} - V_Z}{R_3}$$

$$\therefore \quad 5\times 10^{-3} = \frac{[18-3]-5.6}{R_3}$$

$$\therefore \quad R_3 = \mathbf{1.88\ k\Omega}$$

For $V_{max} = 18 + 3 = 21$ V we get,

$$I_Z = \frac{21-5.6}{1.88\times 10^{3}} = 8.19\ mA$$

$$\therefore \quad P_D = I_Z \times V_Z = 8.19\times 10^{-3}\times 5.6 = 0.045\ W$$

Thus $P_D < P_{Z\,max}$

Thus the designed elements are

$$R_1 = \mathbf{10\ k\Omega}$$

$$R_2 = \mathbf{16.47\ k\Omega}$$

$$R_3 = \mathbf{1.88\ k\Omega}$$

Assume β of the series transistor as 30.

$$\therefore \quad I_B = \frac{I_E}{\beta+1} = \frac{I_{o\,max}}{\beta+1}$$

$$\therefore \quad I_B = \frac{50}{31} = 1.61\ mA$$

The op-amp must be capable of supplying this current. The op-amp 741 has output current rating of 25 mA. Hence op-amp 741 can be used.

$$\therefore \qquad \% \text{ Load regulation} = \frac{\Delta V_o \text{ for given } \Delta I_L (\text{max}) \times 100}{V_o}$$

$$= \frac{2.504 \times 10^{-3} \times 100}{18} = \mathbf{0.0139\%}$$

And $$V_R(\text{out}) = \frac{V_R(\text{in}) Z_Z}{R_3}\left[1 + \frac{R_1}{R_2}\right]$$

$$\therefore \qquad \frac{V_R(\text{out})}{V_R(\text{in})} = \frac{7}{1.8 \times 10^3}\left[1 + \frac{10}{16.4}\right] = 6.26 \times 10^{-3}$$

$$\therefore \qquad RR = 20 \text{ Log } \frac{V_R(\text{out})}{V_R(\text{in})} = \mathbf{-44.068 \text{ dB}}$$

10.10 Precision Voltage Regulator

The limitation of voltage follower regulator is that the zener circuit is connected to the supply side. Thus any changes in V_{in} directly affects the zener voltage and hence the output voltage.

The circuit in which zener circuit is connected to the output side, is called precision voltage regulator and is shown in the Fig. 10.14.

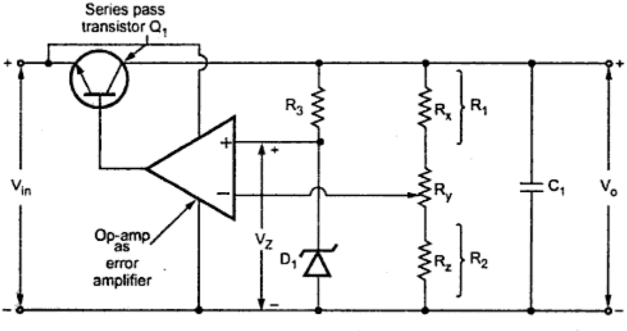


Fig. 10.14 Precision voltage regulator

Except the change in position of zener circuit from input to output, there is no change in the circuit as compared to adjustable voltage regulator circuit.

Now to keep base of Q_1 positive, op-amp output must be more positive than regulated output voltage V_o. But if $+V_{CC}$ of op-amp is connected to V_o, it is not possible hence $+V_{CC}$ terminal of op-amp is connected to positive of V_{in} as shown in the Fig. 10.13.

Now if I_L required is large then,

$$I_{B1} = \frac{I_L}{\beta_1}$$

and

$$I_{B2} = \frac{I_{B1}}{\beta_2} = \frac{I_L}{\beta_1 \beta_2} \quad \text{... (2)}$$

Thus the total current op-amp has to supply reduces by the factor $\frac{1}{\beta_1 \beta_2}$ which it can easily supply.

If the load current is zero, then I_{B1} is very low and hence $I_{E2} = I_{B1}$ is low, Q_2 may not be operating satisfactorily. To avoid this, resistance R_4 is connected to emitter of Q_2 as shown in the Fig. 10.15. Its value is given by,

$$\boxed{R_4 = \frac{V_o + V_{BE1}}{I_{E2}(\text{min})}}$$

10.11 Limitations of Discrete Regulators

The limitations of discrete regulators are,

1. The voltage gets affected by various factors such as temperature, line changes etc.
2. Less reliable than integrated circuit regulators.
3. All the protection circuits are to be added externally, which makes circuit bulkier and heavier.
4. More number of components hence costlier.
5. Flexibility is less.

10.12 Advantages of IC Voltage Regulators

The various advantages of IC voltage regulators are,

1. Easy to use.
2. It greatly simplifies power supply design.
3. Due to mass production, low in cost.
4. IC voltage regulators are versatile.
5. Conveniently used for local regulation.
6. These are provided with features like built in protection, programmable output, current/voltage boosting, internal short circuit current limiting etc.

ii) Load Regulation : As defined earlier, it is the change in output voltage over a given range of load currents i.e. from full load to no load. It is usually expressed in millivolts or as a percentage of output voltage.

iii) Ripple Rejection : It indicates regulator's ability to reject ripple voltage present in the input. It is defined as the ratio of the r.m.s. input ripple voltage to the r.m.s. output ripple voltage. It is expressed in decibels (dB).

iv) Dropout Voltage : It is the minimum voltage that must exist between input and output terminals. As mentioned earlier, it is the difference between input voltage V_{in} and output voltage V_o. For most of the regulators it is 2 to 3 V.

v) Output Resistance (R_o) : It is the rate of change of output voltage with respect to the output current. It should be as small as possible.

vi) Maximum Input Voltage ($V_{in\ max}$) : This is the maximum input voltage that can be applied to the regulator safely.

vii) Maximum Power Dissipation (P_{Dmax}) : This is the maximum power which regulator can dissipate without damage. The actual power dissipated is approximately equal to the voltage drop between the input and the output terminals multiplied by the current through the regulator. For many regulators it is internally limited.

viii) Quiescent Current (I_Q) : It is also called as standby current. This is the supply current drawn by the regulator without any load. It can also be defined as the current that must flow from the ground terminal of the regulator to operate satisfactorily.

ix) Rated Output Current (I_o) : It is the maximum value of the output current above which current limiting occurs.

x) Output Noise Voltage : It indicates the tendency of the output voltage to fluctuate above its prescribed d.c. value, over a specified frequency range.

xi) Maximum Operating Junction Temperature : It is the maximum value of junction temperature above which thermal shutdown occurs.

Out of these parameters maximum input voltage, maximum power dissipation, maximum operating junction temperature etc. are called as absolute maximum ratings of IC regulator, while other ratings are called as electrical characteristics of IC regulator.

10.14.3 IC Series of Three Terminal Fixed Voltage Regulators

The popular IC series of three terminal regulators is µA78XX and µA79XX. The series µA 78XX is the series of three terminal **positive** voltage regulators while µA79XX is the series of three terminal **negative** voltage regulators. The last two digits denoted as XX, indicate the output voltage rating of the IC.

10.14.6 Adjustable Regulator using 78XX Series

Though IC 78XX series regulators have fixed value of the regulated output voltage, by connecting two resistances externally, an adjustable output voltage can be obtained.

The typical connection of 78XX IC regulator to obtain variable output voltage is shown in the Fig. 10.22.

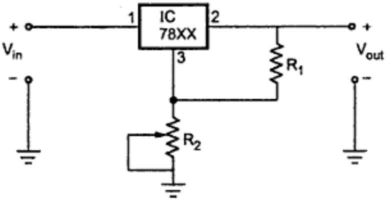


Fig. 10.22 Adjustable regulator using IC 78XX

$$\boxed{V_{out} = V_{reg}\left[1+\frac{R_2}{R_1}\right]}$$

where V_{reg} = Regulated fixed voltage of IC

By varying R_2, variable output voltage can be obtained.

10.14.7 Applications of IC 78XX and 79XX

These ICs are regulator ICs and are basically used to provide constant d.c. voltages to various components in complex electronic circuits.

The IC 7805 is typically used to provide constant 5 V supply to the digital circuits.

The IC 7812 and 7912 are used to provide dual supply of ± 12 V to operational amplifiers used in the electronic circuits.

10.14.8 Datasheet Specifications of IC 7805

The Table 10.3 gives the absolute maximum ratings of the 7805 IC regulator.

Absolute maximum ratings of 7805 voltage regulator	
Input voltage (5 V through 18 V) 24 V)	35 V 40 V
Internal Power dissipation	Internally Limited
Storage Temperature Range	– 65 °C to + 150 °C
Operating junction Temperature range	
µA 7800	– 55 °C to + 150 °C
µA 7800 C	0 °C to + 125 °C

Table 10.3

Example 10.4 : *Calculate the output voltage of the adjustable regulator shown in the Fig. 10.23.*

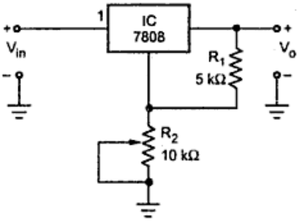


Fig. 10.23

If R_2 is varied from 1 kΩ to 10 kΩ find the range of output voltage.

Solution : $R_1 = 5$ kΩ, $R_2 = 10$ kΩ

The IC is 7808 i.e. $V_{reg} = +8V$

$$\therefore \quad V_{out} = V_{reg}\left[1+\frac{R_2}{R_1}\right] = 8\left[1+\frac{10}{5}\right]$$

$$= 8\times 3 = \mathbf{24\ V}$$

Now $R_2 = 1$ kΩ then,

$$V_{out} = 8\left[1+\frac{1}{5}\right] = \mathbf{9.6\ V}$$

Thus the V_{out} can be varied from 9.6 V to 24 V, by varying R_2 from 1 kΩ to 10 kΩ.

10.14.9 Boosting Regulator Output Current

For limiting the cost and size, if output current as high as 10 A is required then it is convenient to boost a regulator output current, which is of less capacity, with the help of external circuit.

The three terminal regulators can be boosted by connecting an external pass transistor in parallel with the regulator itself. Due to this the maximum output current of 78XX regulator which is 1A,

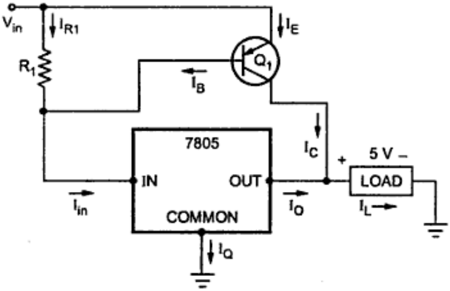


Fig. 10.24 Current Boosting of regulator

used. The Fig. 10.27 shows the functional diagram of LM 317 along with the capacitors and the protecting diodes.

Key Point: *The diodes are necessary if output voltage is higher than 25 V.*

➠ **Example 10.7 :** *Determine the regulated output voltage for the LM 317 voltage regulator shown in the Fig. 10.28.*

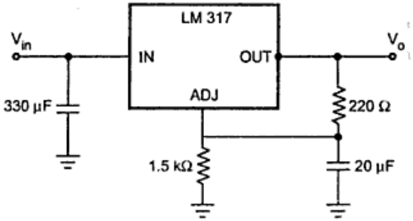


Fig. 10.28

Solution : The resistances used are,

$$R_1 = 220\ \Omega \text{ and } R_2 = 1.5\ \text{k}\Omega$$

while for LM 317, $I_{ADJ} = 100\ \mu A$

$$\therefore \quad V_o = 1.25\left[1+\frac{R_2}{R_1}\right]+I_{ADJ}\,R_2$$

$$= 1.25\left(1+\frac{1.5\times10^3}{220}\right)+100\times10^{-6}\times1.5\times10^3$$

$$= \mathbf{9.92\ V}$$

➠ **Example 10.8 :** *Find the range in which output voltage can be varied with the help of LM 317 regulator using $R_1 = 820\ \Omega$ and R_2 as 10 kΩ potentiometer.*

Solution : For LM 317, the current $I_{ADJ} = 100\ \mu A$

When R_2 is minimum i.e. $R_2 = 0$ then,

$$V_o = 1.25\left[1+\frac{R_2}{R_1}\right]+I_{ADJ}\,R_2 = 1.25\ V$$

When R_2 is maximum, i.e. $R_2 = 10\ \text{k}\Omega$ then

$$V_o = 1.25\left(1+\frac{10\times10^3}{820}\right)+100\times10^{-6}\times10\times10^3 = 17.49\ V$$

Thus the output voltage can be varied in the range **1.25 V to 17.49 V**

10.16 Basic Switching Regulator

The operating principle of switching regulators is completely different than that of linear regulators. The switching regulators are also called as switched mode regulators. Such a switching regulator requires an external transistor and a choke. The series pass transistor in such a regulator is used as a controlled switch and is operated in cut-off region or saturation region. Hence the power transmitted across such a transistor is in the form of discrete pulses rather than a steady flow of current.

When the transistor is operated in the cut-off region, there is no current and dissipates no power. While when it is operated in the saturation region, a negligible voltage drop appears across it and hence dissipates very small power, providing maximum current to load. In any case, the power dissipated in the transistor is very small. Almost the entire power gets transmitted to the load. Hence the efficiency of the switching regulators is always very high.

Key Point: *The pulse width modulation is the basic principle of the switching regulators. The average value of repetitive pulse waveform is proportional to the area under the waveform.*

So switching regulators use the fact that if duty cycle of the pulse waveform is varied, the average value of the voltage also changes proportionally.

Key Point: *The duty cycle of the pulse waveform is the ratio of the on time* t_{on} *to the period T of the pulse waveform.*

Mathematically it can be expressed as,

$$\text{duty cycle } \delta = \frac{t_{on}}{t_{on} + t_{off}} \qquad \dots (1)$$

$$\therefore \quad \boxed{\delta = \frac{t_{on}}{T} = t_{on}\, f} \qquad \dots (2)$$

where t_{on} = on time of pulse

t_{off} = off time of pulse

T = time period $= t_{on} + t_{off} = \frac{1}{f}$

This basic pulse width is shown in the Fig. 10.29.

It has to satisfy the requirements as :

i) It has to supply required power and the losses associated with the regulator.

ii) It must be high to satisfy the minimum requirements of the regulator.

iii) It must be large to supply sufficient dynamic range of line and load changes.

The switch is generally a transistor. The pulse generator output makes it on and off. The pulse generator produces a required pulse waveform. The most effective range of pulse waveform frequency is 20 kHz. The typical operating frequency range is 10 to 50 kHz. The filter F_1 may be RC, RL or RLC. Most commonly used filter is RLC. It converts the pulse waveforms obtained from the switch into a d.c. output voltage.

10.17 Block Diagram of SMPS

The Fig. 10.31 shows the functional block diagram of basic switching voltage regulator, which uses transistor Q_1 as a switch.

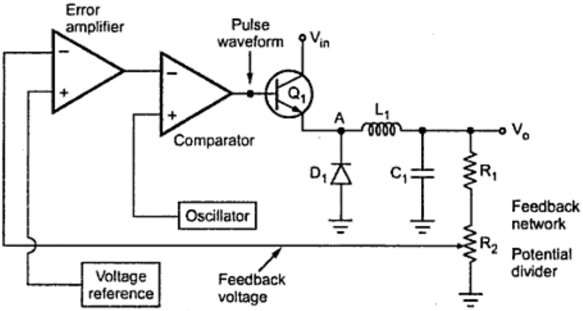


Fig. 10.31 Functional block diagram of switching regulator

The part $R_2/R_1 + R_2$ of the output is fedback to the inverting input of error amplifier. It is compared with the reference voltage. The difference is amplified and given to the comparator inverting terminal.

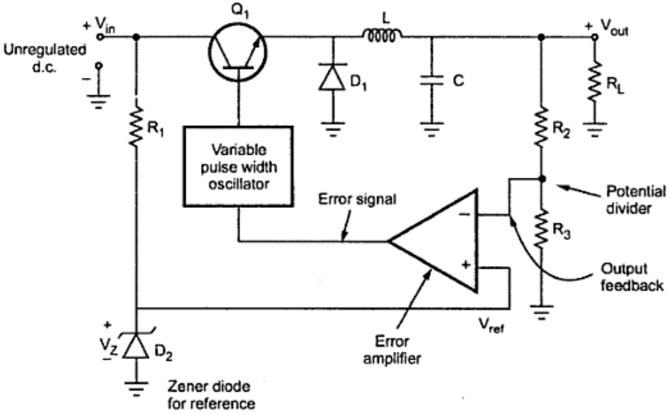
The oscillator generates a triangular waveform at a fixed frequency. It is applied to the non-inverting terminal of the comparator. The output of the comparator is high when the triangular voltage waveform is above the level of the error amplifier output. Due to this the transistor Q_1 remains in cut-off state. **Thus the output of the comparator is nothing but a required pulse waveform.**

The period of this pulse waveform is same as that of oscillator output say T. The duty cycle is denoted as $\delta = t_{on}/T$ or t_{on} f as mentioned earlier. This duty cycle is controlled by the difference between the feedback voltage and the reference voltage.

10.19 Step Down Switching Regulator (Buck)

The Fig. 10.32 shows the basic circuit of step down switching regulator, which is also called buck type switching regulator.

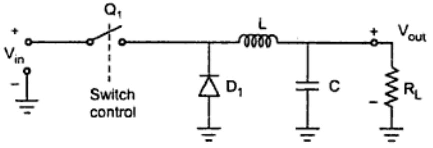
It uses an inductor L and series transistor Q_1 which acts as a switch. The reference for error amplifier is provided by zener voltage V_Z. The output is fed back to error amplifier through potential divider. The pulse width oscillator controls the operation of Q_1 as on or off, depending on the load requirements.



Q1
+ Vin
Unregulated d.c.
L
+ Vout
D1
C
RL
R1
Variable pulse width oscillator
R2
Potential divider
Error signal
R3
Output feedback
Vref
+
VZ
D2
Error amplifier
Zener diode for reference

Fig. 10.32 Step down switching regulator

Consider an equivalent circuit of the regulator as shown in the Fig. 10.33. In this circuit, Q_1 is shown as a switch as it does the function of a switch.



Q1
+
Vin
-
Switch control
L
D1
C
+ Vout
RL
-

Fig. 10.33 Equivalent circuit

The transistor Q_1 is used for switching the input voltage for the required period of time, which is dependent on load current requirement. The L-C filter averages the switched voltage.

The Fig. 10.35 shows the waveform of capacitor voltages for $t_{on} > t_{off}$ and $t_{on} < t_{off}$.

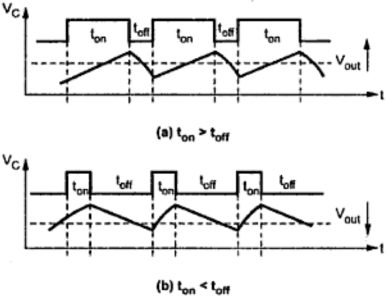

V_C
t_on
t_off
V_out
t
(a) t_on > t_off
V_C
t_on
t_off
V_out
t
(b) t_on < t_off

Fig. 10.35 Variation in V_{out} based on duty cycle

The waveforms for step down switching regulator are shown in the Fig 10.36.

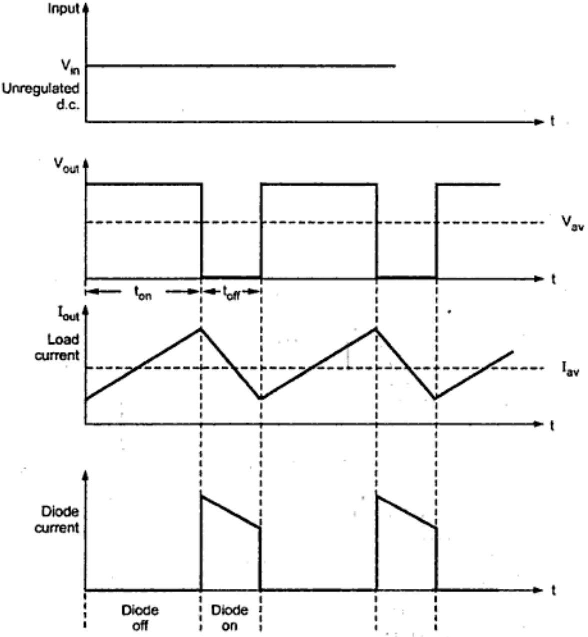

Input
V_in
Unregulated d.c.
t
V_out
V_av
t
t_on
t_off
I_out
Load current
I_av
t
Diode current
t
Diode off
Diode on

Fig. 10.36 Waveforms for step down switching regulator

The transistor Q_1 works as an on/off switch. When Q_1 is driven into saturation, V_{CE} is very very small and it acts as short circuit. When Q_1 is driven into cut-off, it is off and it acts as an open circuit. Let us study these two cases in detail.

Case 1 : Let Q_1 is ON i.e. driven to saturation.

When Q_1 is ON, V_{CE} is denoted as V_{CE}(sat) and the voltage across L suddenly becomes [V_{in} – V_{CE}(sat)] as shown in the Fig. 10.38 (a). This expands the magnetic field around the inductor very quickly. This voltage across L can be obtained by applying KVL to V_{in}, L, Q_1 and V_{in} closed path.

During the ON time (t_{on}) of Q_1, the voltage across the inductor starts decreasing exponentially from its initial maximum value [V_{in} – V_{CE}(sat)].

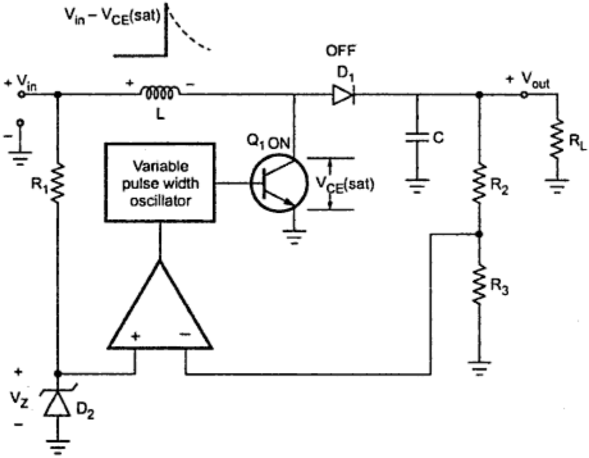


Fig. 10.38 (a) Step up type when Q_1 is ON

Key Point: *The longer the on time of Q_1, the smaller will be the voltage across L.*

Case 2 : Let Q_1 is switched OFF i.e. cut-off region. When Q_1 is OFF, the magnetic field of the inductor L collapses and its polarity gets reversed. This is because an inductor current can not change instantly. Thus value of V_L attained after exponential decrease when Q_1 is ON, now gets reversed as shown in the Fig. 10.38 (b). Due to reversal of polairty, it gets added to V_{in}.

Trace the path V_{in}, L, D_1, C and V_{in}. The diode D_1 is forward biased due to reversed V_L and **capacitor C now charges to V_{in} + V_L. The output voltage is voltage across**

10.20.2 Disadvantages

The disadvantages of boost regulator are :

1. It provides single output.
2. The duty cycle is limited to 50% to avoid the continuous current mode. If regulator enters the continuous current mode, it stops regulating the output. Thus for a minimum input voltage range, maximum duty cycle is limited.
3. Due to restricted duty cycle, the peak collector current is very high. This limits its output power rating.
4. No isolation between input and output. Any surge or transient in input can reach to output directly.

10.21 Voltage Inverter Type Switching Regulator (Buck-Boost)

This type of switching regulator produces an output voltage having polarity opposite to that of the input voltage. This is also called **buck boost type switching regulator.** The Fig. 10.40 shows voltage inverter type switching regulator.

The elements are again identical to buck and boost type regulators but their connections are different. The basic action remains same. Any change in output produces error which gets amplified by op-amp error amplifier. This controls the on/off periods of Q_1 to regulate the output, through variable pulse width oscillator.

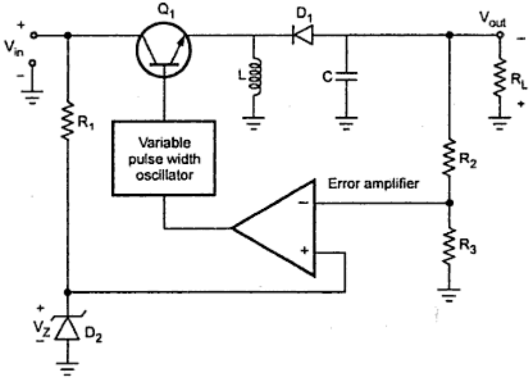


Fig. 10.40 Voltage inverter type switching regulator

Let us analyse two cases.

Case 1 : Let Q_1 is switched ON.

The Q_1 goes into saturation and the voltage across it drops to V_{CE}(sat) which is about 0.3 V. Due to this voltage across inductor suddenly rises to [V_{in} – V_{CE}(sat)] and magnetic

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